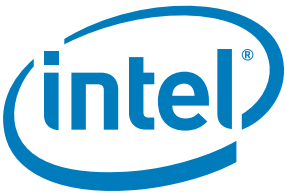


Intel® Core™ Duo Processor and Intel® Core™ Solo Processor on 65 nm Process

Datasheet

January 2007

Document Number: 309221-006

Contents

Figures

Tables

Revision History

Revision	Description	Date
-001	Initial Release	January 2006
-002	• Added references to ULV processor throughout the document • Replaced references to the terminology Deep C4 voltage with Intel® Enhanced Deeper Sleep Voltage throughout the document. • Replaced references to Enhanced Low Power states with CxE Low Power States • Section 3.10 — Included Table 10 Voltage and Current Specifications for Intel Core Solo Processor ULV — Included Figure 5 Active VCC and ICC Load Line for Intel Core Solo Processor ULV — Included Figure 6 Deeper Sleep VCC and ICC Load Line for Intel Core Solo Processor ULV • Chapter 5 — Included Table 24 Power Specifications for the Intel Core Solo Processor ULV (Ultra Low Voltage)	April 2006
-003	• Added Intel® Core™ Duo Processor T2300E and Intel® Core™ Solo Processor T1400 specifications.	May 2006
-004	• Added references to Intel Core Duo Processor, Ultra Low Voltage (ULV) throughout the document • CxE low power states now also referred to as Extended Low Power States • Section 3.10 — Updated Table 6 - Added Icc spec for T2700 — Included Table 9 Voltage and Current Specifications Intel Core Duo Processor, Ultra Low Voltage (ULV) • Chapter 5 — Updated Table 20 - Added TDP for T2700 — Included Table 23 - Power Specification for Intel Core Duo Processor Ultra Low Voltage (ULV)	June 2006
-005	• In Chapter 3: — Added L2500 processor specifications to Table 8. — Added U2400 processor specifications to Table 9. • In Chapter 5: — Added L2500 processor power specifications to Table 22. — Added U2400 processor power specifications to Table 23.	September 2006
-006	• In Chapter 3: — Added U1500 processor specifications to Table 10. • In Chapter 5: — Added U1500 processor power specifications to Table 24.	January 2007

§

1 Introduction

The Intel® Core™ Duo processor and the Intel® Core™ Solo processor are built on Intel's next generation 65 nanometer process technology with copper interconnect. The Intel Core Solo processor refers to a single core processor and the Intel Core Duo processor refers to a dual core processor. This document provides specifications for all Intel Core Duo processor and Intel Core Solo processor in standard voltage (SV), low voltage (LV) and ultra low voltage (ULV) products.

Note: All instances of the "processor" in this document refer to the Intel Core Duo processor and Intel Core Solo processor with 2-MB L2 cache, unless specified otherwise.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.

The following list provides some of the key features on this processor:

- First dual core processor for mobile
- Supports Intel® Architecture with Dynamic Execution
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache
- On-die, 2-MB second level cache with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3)
- The Intel Core Duo processor and Intel Core Solo processor standard voltage and low voltage processors are offered at 667-MHz FSB
- The Intel Core Duo processor and Intel Core Solo processor ultra low voltage are offered at 533-MHz FSB
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Digital thermal sensor (DTS)
- The Intel Core Duo processor and Intel Core Solo processor standard voltage are offered in both the Micro-FCPGA and the Micro-FCBGA packages
- Intel Core Duo processor low voltage is offered only in the Micro-FCBGA package
- The Intel Core Duo processor and Intel Core Solo processor ultra low voltage are offered only in Micro-FCBGA package
- Execute Disable Bit support for enhanced security
- Intel® Virtualization Technology
- Intel® Enhanced Deeper Sleep and Dynamic Cache Sizing

The processor maintains support for MMX™ technology, Streaming SIMD instructions, and full compatibility with IA-32 software. The processor features on-die, 32-KB, Level 1 instruction and data caches and a 2-MB level 2 cache with Advanced Transfer Cache Architecture. The processor's Data Prefetch Logic speculatively fetches data to the L2 cache before the L1 cache requests occurs, resulting in reduced bus cycle penalties. The processor includes the Data Cache Unit Streamer which enhances the performance of the L2 prefetcher by requesting L1 warm-ups earlier. In addition, the Writer Order Buffer depth is enhanced to help with the write-back latency performance.

In addition to supporting the existing Streaming SIMD Extensions 2 (SSE2), there are 13 new instructions which extend the capabilities of Intel processor technology further. These new instructions are called Streaming SIMD Extensions 3 (SSE3). 3D graphics and other entertainment applications, such as gaming, will have the opportunity to take advantage of these new instructions as platforms with the processor and SSE3 become available in the market place.

The processor's FSB utilizes a split-transaction, deferred reply protocol. The FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock. The 4X data bus can deliver data four times per bus clock and is referred as "quad-pumped" or 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and the 2X address bus provide a data bus bandwidth of up to 5.33 GB/second. The FSB uses Advanced Gunning Transceiver Logic (AGTL+) signaling technology, a variant of GTL+ signaling technology with low power enhancements.

The processor features Enhanced Intel SpeedStep Technology, which enables real-time dynamic switching between multiple voltage and frequency points. The processor features the Auto Halt, Stop Grant, Deep Sleep, and Deeper Sleep low power C-states.

The processor utilizes socketable Micro Flip-Chip Pin Grid Array (Micro-FCPGA) and surface mount Micro Flip-Chip Ball Grid Array (Micro-FCBGA) package technology. The Micro-FCPGA package plugs into a 479-hole, surface-mount, Zero Insertion Force (ZIF) socket, which is referred to as the mPGA479M socket.

The processor supports the Execute Disable Bit capability. This feature, combined with a support operating system, allows memory to be marked as executable or non executable. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® Architecture Software Developer's Manual* for more detailed information.

Intel Virtualization Technology is a set of hardware enhancements to Intel server and client systems that combined with the appropriate software, will enable enhanced virtualization robustness and performance for both enterprise and consumer uses. Intel Virtualization Technology forms the foundation of Intel technologies focused on improved virtualization, safer computing, and system stability. For client systems, Intel Virtualization Technology's hardware-based isolation helps provide the foundation for highly available and more secure client virtualization partitions.

1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined.
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document. Chipset references in this document are to the Mobile Intel® 945 Express Chipset family unless specified otherwise.

Document	Document Number
Intel® Core™ Duo Processor and Intel® Core™ Solo Processor on 65 nm Process Specification Update	309222
Mobile Intel® 945 Express Chipset Family Datasheet	309219
Mobile Intel® 945 Express Chipset Family Specification Update	309220
Intel® I/O Controller Hub 7 (ICH7) Family Datasheet	307013
Intel® I/O Controller Hub 7 (ICH7) Family Specification Update	307014
Intel® Architecture Software Developer's Manual	
Volume 1 Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669
AP-485, Intel® Processor Identification and CPUID Instruction Application Note	241618

§

2 Low Power Features

2.1 Clock Control and Low Power States

The Intel Core Duo processor and Intel Core Solo processor support low power states both at the individual core level and the package level for optimal power management. A core may independently enter the C1/AutoHALT, C1/MWAIT, C2, C3, and C4 low power states. Refer to Figure 2 for a visual representation of the core low power states for the Intel Core Duo processor and Intel Core Solo processor. When both cores coincide in a common core low power state, the central power management logic ensures the Intel Core Duo processor enters the respective package low power state by initiating a P_LVLx (P_LVL2, P_LVL3, and P_LVL4) I/O read to the Mobile Intel 945 Express Chipset family. Package low power states include Normal, Stop Grant, Stop Grant Snoop, Sleep, Deep Sleep, and Deeper Sleep. Refer Figure 1 for a visual representation of the package low-power states for the Intel Core Duo processor and Intel Core Solo processor and to Table 1 for a mapping of core low power states to package low power states.

The processor implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR.

When software running on a core requests the C4 state, that core enters the core C4 state, which is identical to the core C3 state. When both cores have requested C4 then the Intel Core Duo processor will enter the Deeper Sleep state.

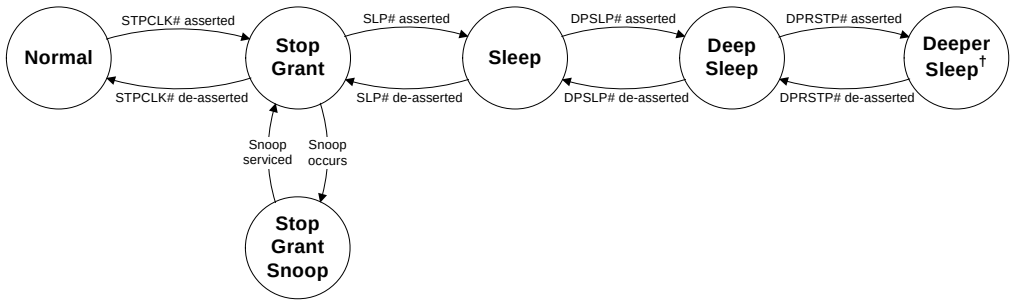
If a core encounters a chipset break event while STPCLK# is asserted, then it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that individual cores should return to the C0 state and the Intel Core Duo processor should return to the Normal state. Same mechanism is also applicable for the Intel Core Solo processor.

Table 1. Coordination of Core-Level Low Power States at the Package Level

Resolved Package State		Single Core	Dual Core: Core1 State				
			C0	C1[1]	C2	C3	C4
Core0 / Functional Core State	C0	Normal	Normal	Normal	Normal	Normal	Normal
	C1†	Normal	Normal	Normal	Normal	Normal	Normal
	C2	Stop Grant	Normal	Normal	Stop Grant	Stop Grant	Stop Grant
	C3	Deep Sleep	Normal	Normal	Stop Grant	Deep Sleep	Deep Sleep
	C4	Deeper Sleep	Normal	Normal	Stop Grant	Deep Sleep	Deeper Sleep / Intel® Enhanced Deeper Sleep

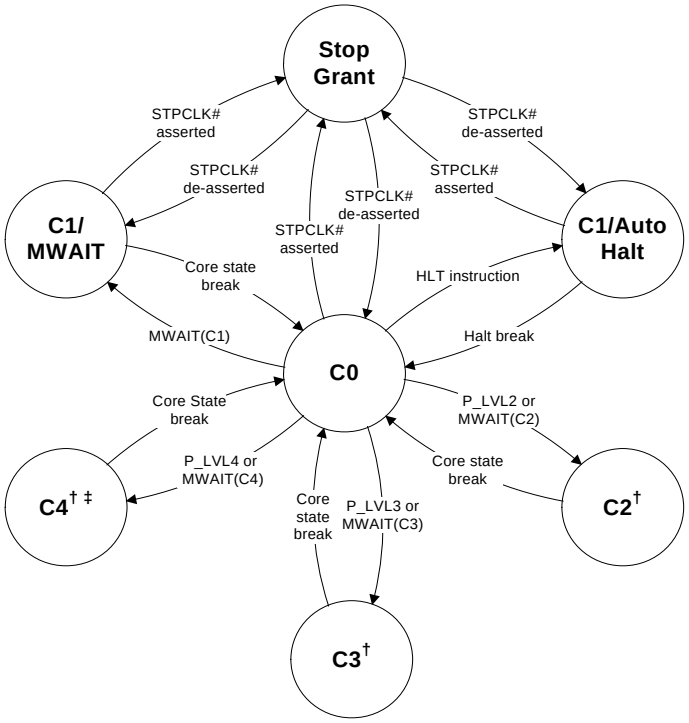
NOTE:
1. AutoHALT or MWAIT/C1.

Figure 1. Package-Level Low Power States



† — Deeper Sleep includes the Deeper Sleep and the Intel Enhanced Deeper Sleep state.

Figure 2. Core Low Power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no effect if a core is in C2, C3, or C4.
‡ — Core C4 state supports the package level Intel Enhanced Deeper sleepstate.

2.1.1 Core Low-Power States

2.1.1.1 C0 State

This is the normal operating state for the Intel Core Duo processor and Intel Core Solo processor.

2.1.1.2 C1/AutoHALT Powerdown State

C1/AutoHALT is a low power state entered when the processor core executes the HALT instruction. The processor core will transition to the C0 state upon the occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel® Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate an STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Powerdown state, the dual core processor will process bus snoops and snoops from the other core, and the single core processor will process only the bus snoops. The processor core will enter a snoopable sub-state (not shown in Figure 2) to process the snoop and then return to the AutoHALT Powerdown state.

2.1.1.3 C1/MWAIT Powerdown State

MWAIT is a low power state entered when the processor core executes the MWAIT instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that there is an additional event that can cause the processor core to return to the C0 state: the Monitor event. See the *Intel® Architecture Software Developer's Manual, Volumes 2A/2B: Instruction Set Reference,* for more information.

2.1.1.4 Core C2 State

Individual cores of the Intel Core Duo processor and Intel Core Solo processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in C2 state, the dual core processor will process bus snoops and snoops from the other core, and the single core processor will process only the bus snoops. The processor core will enter a snoopable sub-state (not shown in Figure 2) to process the snoop and then return to the C2 state.

2.1.1.5 Core C3 State

Core C3 state is a very low power state the processor core can enter while maintaining context. Individual cores of the Intel Core Duo processor and Intel Core Solo processor can enter the C3 state by initiating a P_LVL3 I/O read to the P_BLK or an MWAIT(C3) instruction. Before entering the C3 state, the processor core flushes the contents of its L1 caches into the processor's L2 cache. Except for the caches, the processor core maintains all its architectural state in the C3 state. The Monitor remains armed if it is configured. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed the processor keeps the core in the C3 state when the processor detects a snoop on the FSB or when the other core of the dual core processor accesses cacheable memory. The processor core will transition to the C0 state upon the occurrence of a Monitor event, SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor core to immediately initialize itself.

2.1.1.6 Core C4 State

Individual cores of the Intel Core Duo processor and Intel Core Solo processor can enter the C4 state by initiating a P_LVL4 I/O read to the P_BLK or an MWAIT(C4) instruction. The processor core behavior in the C4 state is identical to the behavior in the C3 state. The only difference is that if both processor cores are in C4, then the central power management logic will request that the entire dual core processor enter the Deeper Sleep package low power state (see Section 2.1.2.5). The single core processor would be put into the Deeper Sleep State in C4 state if the low power state coordination logic is enabled.

To enable the package level Intel Enhanced Deeper Sleep Low Voltage, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the software programmable MSR.

2.1.2 Package Low Power States

The package level low power states are applicable for the Intel Core Duo processor as well as the Intel Core Solo processor. The package level low power states are described in Section 2.1.2.1 through Section Section 2.1.2.6.

2.1.2.1 Normal State

This is the normal operating state for the processor. The processor enters the Normal state when at least one of its cores is in the C0, C1/AutoHALT, or C1/MWAIT state.

2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted, each core of the Intel Core Duo processor and Intel Core Solo processor enters the Stop-Grant state within 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Processor cores that are already in the C2, C3, or C4 state remain in their current low-power state. When the STPCLK# pin is deasserted, each core returns to its previous core low power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system the STPCLK#, SLP#, DPSLP#, and DPRSTP# pins must be deasserted more than 450 µs prior to RESET# deassertion. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted ten or more bus clocks after the deassertion of SLP#.

While in Stop-Grant state, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT# and LINT[1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire dual core processor should return to the Normal state.

A transition to the Stop Grant Snoop state will occur when the processor detects a snoop on the FSB (see Section 2.1.2.3). A transition to the Sleep state (see Section 2.1.2.4) will occur with the assertion of the SLP# signal.

2.1.2.3 Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor will return to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

2.1.2.4 Sleep State

The Sleep state is a low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin. (See Section 2.1.2.5.) While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.

2.1.2.5 Deep Sleep State

Deep Sleep state is a very low power state the processor can enter while maintaining context. Deep Sleep state is entered by asserting the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. BCLK stop/restart timings on appropriate chipset-based platforms with the CK410M clock chip are as follows:

- Deep Sleep entry: the system clock chip may stop/tristate BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- Deep Sleep exit: the system clock chip must drive BCLK to differential DC levels within 2-3 ns of DPSLP# deassertion and start toggling BCLK within 10 BCLK periods.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be re-started after DPSLP# deassertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.1.2.6 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but reduces core voltage to one of two lower levels. One lower core voltage level is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. The other lower core voltage level, the lowest possible in the processor, is achieved by entering the Intel Enhanced Deeper Sleep state of Deeper Sleep state. The Intel Enhanced Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep only when the L2 cache has been completely shut down. Refer to Section 2.1.2.6.1 and Section 2.1.2.6.2 for further details on reducing the L2 cache and entering Intel Enhanced Deeper Sleep state.

In response to entering Deeper Sleep, the processor will drive the VID code corresponding to the Deeper Sleep core voltage on the VID[6:0] pins.

Exit from the Deeper Sleep state or Intel Enhanced Deeper Sleep state is initiated by DPRSTP# deassertion when either core requests a core state other than C4 or either core requests a processor performance state other than the lowest operating point.

2.1.2.6.1 Intel Enhanced Deeper Sleep State

Intel Enhanced Deeper Sleep state is a sub-state of Deeper Sleep that extends power saving capabilities by allowing the processor to further reduce core voltage once the L2 cache has been reduced to zero ways and completely shut down. The following events occur when the processor enters Intel Enhanced Deeper Sleep state:

- The last core entering C4 issues a P_LVL4 I/O read or an MWAIT(C4) instruction and then progressively reduces the L2 cache to zero.
- The processor drives the VID code corresponding to the Intel Enhanced Deeper Sleep state core voltage on the VID[6:0] pins.

2.1.2.6.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following conditions:

- The second core is already in C4 and the Intel Enhanced Deeper Sleep state is enabled (as specified in Section 2.1.2.6.1).
- The C0 timer, which tracks continuous residency in the Normal package state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The FSB speed to processor core speed ratio is below the predefined L2 shrink threshold.

If the FSB speed to processor core speed ratio is above the predefined L2 shrink threshold, then L2 cache expansion will be requested. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.

Upon STPCLK# deassertion, the first core exiting the Intel Enhanced Deeper Sleep state will expand the L2 cache to 2 ways and invalidate previously disabled cache ways. If the L2 cache reduction conditions stated above still exist when the last core returns to C4 and the package enters Intel Enhanced Deeper Sleep state, then the L2 will be shrunk to zero again. If a core requests a processor performance state resulting in a higher ratio than the predefined L2 shrink threshold, the C0 timer expires, or the second core (not the one currently entering the interrupt routine) requests the C1, C2, or C3 states, then the whole L2 will be expanded when the next INTR event would occur.

L2 cache shrink prevention may be enabled as needed on occasion through an MWAIT(C4) sub-state field. If shrink prevention is enabled, then the processor does not enter the Intel Enhanced Deeper Sleep state since the L2 cache remains valid and in full size.

2.2 Enhanced Intel SpeedStep® Technology

Intel Core Duo processor and Intel Core Solo processor feature Enhanced Intel SpeedStep Technology. Following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage/frequency operating points provide optimal performance at the lowest power.
- Voltage/Frequency selection is software controlled by writing to processor MSR's (Model Specific Registers).
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure glitch free transitions.
- Low transition latency and large number of transitions possible per second.
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition

  - The bus protocol (BNR# mechanism) is used to block snooping
- Improved Intel® Thermal Monitor mode.
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency/ voltage specified in a software programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency/voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.
- Enhanced thermal management features.
  - Digital thermal sensor and thermal interrupts
  - TM1 in addition to TM2 in case of non successful TM2 transition.
  - dual core thermal management synchronization.

Each core in the Intel Core Duo processor implements an independent MSR for controlling Enhanced Intel SpeedStep Technology, but both cores must operate at the same frequency and voltage. The processor has performance state coordination logic to resolve frequency and voltage requests from the two cores into a single frequency and voltage request for the package as a whole. If both cores request the same frequency and voltage then the Intel Core Duo processor will transition to the requested common frequency and voltage. If the two cores have different frequency and voltage requests then the Intel Core Duo processor will take the highest of the two frequencies and voltages as the resolved request and transition to that frequency and voltage.

2.3 Extended Low Power States

The Extended low power states (C1E, C2E, C3E, C4E) optimize for power by forcibly reducing the performance state of the processor when it enters a package low power state. Instead of directly transitioning into the package low power states, the extended low power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the package low power state, control will be returned to software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in the package low power states.

The processor implements two software interfaces for requesting extended low power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring a software programmable MSR bit to automatically promote package low power states to extended low power states.

Note: C2E and C4E must be enabled via the BIOS for the processor to remain within specification.

Enhanced Intel SpeedStep Technology transitions are multistep processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low power states since processor clocks are not active in these states. C4E is an exception to this rule when the Hard C4E configuration is enabled in a software programmable MSR bit. This C4E low power state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency. The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state

entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

2.4 FSB Low Power Enhancements

The processor incorporates FSB low power enhancements:

- Dynamic FSB Power Down
- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On Die Termination disabling
- Low VCCP (I/O termination voltage)

The Intel Core Duo processor and Intel Core Solo processor incorporate the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in chipset address and control input buffers when the processor deasserts its BR0# pin. The On Die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.5 Processor Power Status Indicator (PSI#) Signal

The Intel Core Duo processor and Intel Core Solo processor incorporate the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve intermediate and light load efficiency of the voltage regulator, resulting in platform power savings and improved battery life. The algorithm that the Intel Core Duo processor and Intel Core Solo processor use for determining when to assert PSI# is different from the algorithm used in previous Intel® Pentium® M processors.

§

3 Electrical Specifications

3.1 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. Please contact your Intel representative for more details. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.2 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the Intel Core Duo processor and Intel Core Solo processors' core frequency is a multiple of the BCLK[1:0] frequency. The processor uses a differential clocking implementation.

3.3 Voltage Identification

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of power supply voltages. The VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A 1 in this refers to a high-voltage level and a 0 refers to low-voltage level.

Table 2. Voltage Identification Definition (Sheet 1 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125

Table 2. Voltage Identification Definition (Sheet 2 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375

Table 2. Voltage Identification Definition (Sheet 3 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625

Table 2. Voltage Identification Definition (Sheet 4 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125

3.4 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor.

3.5 Signal Terminations and Unused Pins

All RSVD (RESERVED) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

The TEST1 pin must have a stuffing option connection to V_{SS}. The TEST2 pin must have a 51 Ω ±5%, pull-down resistor to V_{SS}.

3.6 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the Mobile Intel 945 Express Chipset family on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 3:

Table 3. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	L	RESERVED
L	L	H	133 MHz
L	H	L	RESERVED
L	H	H	166 MHz

3.7 FSB Signal Groups

In order to simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependant upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 4 identifies which signals are common clock, source synchronous, and asynchronous.

Table 4. FSB Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, DPWR#, PREQ#, RESET#, RS[2:0]#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[3:0]#[3], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#[3]
AGTL+ Source Synchronous I/O	Synchronous to Assoc. Strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[31:17]#</td><td>ADSTB[1]#</td></tr><tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
CMOS Input	Asynchronous	A20M#, DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Open Drain Output	Asynchronous	FERR#, IERR#, THERMTRIP#
Open Drain I/O	Asynchronous	PROCHOT#[4]
CMOS Output	Asynchronous	PSI#, VID[6:0], BSEL[2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0]
Power/Other		COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, V_{CC}, V_{CCA}, V_{CCP}, $V_{CCSENSE}$, V_{SS}, $V_{SSSENSE}$

NOTES:
1. Refer to Table 17 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. BPM[2:1]# and PRDY# are AGTL+ output only signals.
4. PROCHOT# signal type is open drain output and CMOS input.

3.8 CMOS Signals

CMOS input signals are shown in Table 4. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for at least three BCLKs in order for the processor to recognize them. See Section 3.10 for the DC specifications for the CMOS signal groups.

3.9 Maximum Ratings

Table 5 specifies absolute maximum and minimum ratings. Only within specified operation limits, can functionality and long-term reliability be expected.

At condition outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from electro static discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 5. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor Storage Temperature	-40	85	°C	2
V_{CC}	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.6	V	1
$V_{inAGTL+}$	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.3	1.6	V	1, 2
$V_{inAsynch\_CMOS}$	CMOS Buffer DC iNput Voltage with Respect to V_{SS}	-0.3	1.6	V	1, 2

NOTES:
1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

3.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Table 4 for the pin signal definitions and signal pin assignments. Most of the signals on the FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 12. DC specifications for the CMOS group are listed in Table 13.

Table 6 through Table 14 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at Tjunction = 100°C. Care should be taken to read all notes associated with each parameter.

Table 6. Voltage and Current Specifications for Intel Core Duo Processor SV (Standard Voltage) (Sheet 1 of 2)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		1.1625		1.3	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.7625		1.0	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up			1.20		V	2, 8
V_{CCP}	AGTL+ Termination Voltage		0.997	1.05	1.102	V	2
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep Voltage		0.55		0.85	V	1, 2, 12
V_{CCDC4}	V_{CC} at Intel Enhanced Deeper Sleep Voltage		0.50		0.80	V	1, 2
I_{CCDES}	I_{CC} for Intel® Core™ Duo Processor SV Recommended Design Target				36	A	5
I_{CC}	I_{CC} for Intel Core Duo Processor SV						
	Processor Number	Core Frequency/Voltage					
	T2700	2.33 GHz and HFM V_{CC}			34	A	3,12,13
	T2600	2.16 GHz and HFM V_{CC}			34		
	T2500	2.00 GHz and HFM V_{CC}			34		
	T2400	1.83 GHz and HFM V_{CC}			34		
	T2300	1.66 GHz and HFM V_{CC}			34		
	T2300E	1.66 GHz and HFM V_{CC}			34		
	N/A	1 GHz and LFM V_{CC}			15.5		
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM				 12.5 23.3	A	3,4
I_{SLP}	I_{CC} Sleep LFM HFM				 12.4 23.2	A	3,4

Table 6. Voltage and Current Specifications for Intel Core Duo Processor SV (Standard Voltage) (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DSLP}	I_{CC} Deep Sleep LFM HFM			 11.8 20.9	 A	 3, 4
I_{DPRSLP}	I_{CC} Deeper Sleep			7.6	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep			6.7	A	4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at CPU Package Pin			600	A/µs	6, 7
I_{CCA}	I_{CC} for V_{CCA} Supply			120	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable			6.0 2.5	A A	10 9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or C1E).
2. The voltage specifications are assumed to be measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. The I_{CCDES}(max) specification of 36 A comprehends only Intel Core Duo processor SV HFM frequencies. Platforms should be designed to 44 A to be compatible with next generation processor.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. V_{CC}, boot tolerance is shown in Figure 3.
9. This is a steady-state I_{CCP} current specification, which is applicable when both V_{CCP} and V_{CC} core are high.
10. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC} core is low.
11. Specified at the nominal V_{CC}.
12. If a given Operating Systems C-State model is not based on the use of MWAIT or I/O Redirection, the processor Deeper Sleep VID will be same as LFM VID.
13. T2300E does not support Intel Virtualization Technology.

Table 7. Voltage and Current Specifications for Intel Core Solo Processor SV (Standard Voltage)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		1.1625		1.3	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.7625		1.0	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up			1.20		V	2, 8
V_{CCP}	AGTL+ Termination Voltage		0.997	1.05	1.102	V	2
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep Voltage		0.55		0.85	V	1, 2, 12
V_{CCDC4}	V_{CC} at Intel Enhanced Deeper Sleep Voltage		0.50		0.80	V	1, 2
I_{CCDES}	I_{CC} for Intel® Core™ Solo Processor SV				36	A	5
I_{CC}	I_{CC} for Intel Core Solo Processor SV						
	Processor Number	Core Frequency/Voltage					
	T1400 T1300 N/A	1.83 GHz and HFM V_{CC} 1.66 GHz and HFM V_{CC} 1 GHz and LFM V_{CC}			34 15.5	A	3,11
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM				 12.5 23.3	A	3,4
I_{SLP}	I_{CC} Sleep LFM HFM				 12.4 23.2	A	3,4
I_{DSLP}	I_{CC} Deep Sleep LFM HFM				 11.8 20.9	A	3,4
I_{DPRSLP}	I_{CC} Deeper Sleep				7.6	A	3,4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep				6.7	A	4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at CPU Package Pin				600	A/µs	6, 7
I_{CCA}	I_{CC} for V_{CCA} Supply				120	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before Vcc Stable I_{CC} for V_{CCP} Supply after Vcc Stable				6.0 2.5	A A	10 9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or C1E).
2. The voltage specifications are assumed to be measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. The I_{CCDES}(max) specification of 36 A comprehends only Intel Core Solo processor SV HFM frequencies.

6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. V_{CC}, boot tolerance is shown in Figure 3.
9. This is a steady-state Iccp current specification, which is applicable when both V_{CCP} and Vcc core are high.
10. This is a power-up peak current specification, which is applicable when V_{CCP} is high and Vcc core is low.
11. Specified at the nominal V_{CC}.
12. If a given Operating System C-State model is not based on the use of MWAIT or I/O Redirection, the processor Deeper Sleep VID will be same as LFM VID.

Table 8. Voltage and Current Specifications for Intel Core Duo Processor LV (Low Voltage)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		1.0000		1.2125	V	1, 2, 3
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.7625		1.0000	V	1, 2, 3
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up			1.20		V	2, 8
V_{CCP}	AGTL+ Termination Voltage		0.997	1.05	1.102	V	2
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep Voltage		0.55		0.85	V	1, 2, 12
V_{CCDC4}	V_{CC} at Intel® Enhanced Deeper Sleep Voltage		0.50		0.80	V	1, 2
I_{CCDES}	I_{CC} for Intel® Core™ Duo Processor LV				19	A	5
I_{CC}	Icc for Intel Core Duo Processor LV						
	Processor Number	Core Frequency/Voltage					
	L2500 L2400 L2300 N/A	1.83 GHz and HFM V_{CC} 1.66 GHz and HFM V_{CC} 1.50 GHz and HFM V_{CC} 1 GHz and LFM V_{CC}			19 19 19 15.5	A	3,11
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM				 12.5 13.5	A	3,4
I_{SLP}	I_{CC} Sleep LFM HFM				 12.4 13.3	A	3,4
I_{DSLP}	I_{CC} Deep Sleep LFM HFM				 11.8 12.0	A	3,4
I_{DPRSLP}	I_{CC} Deeper Sleep				7.6	A	3,4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep				6.7	A	4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at CPU Package Pin				600	A/µs	6, 7
I_{CCA}	I_{CC} for V_{CCA} Supply				120	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable				6.0 2.5	A A	10 9

NOTES:
1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or C1E).
2. The voltage specifications are assumed to be measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. The I_{CCDES}(max) specification of 19 A comprehends only Intel Core Duo processor LV HFM frequencies.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. V_{CC}, boot tolerance is shown in Figure 3.
9. This is a steady-state Iccp current specification, which is applicable when both V_{CCP} and V_{CC} core are high.
10. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC} core is low.
11. Specified at the nominal V_{CC}.
12. If a given Operating System C-State model is not based on the use of MWAIT or I/O Redirection, the processor Deeper Sleep VID will be same as LFM VID.

Table 9. Voltage and Current Specifications Intel Core Duo Processor Ultra Low Voltage (ULV) (Sheet 1 of 2)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		0.85		1.1	V	1, 2
V_{CCLFM}	V_{CC}at Lowest Frequency Mode (LFM)		0.8		1.0	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up			1.20		V	2, 7, 9
V_{CCP}	AGTL+ Termination Voltage		0.997	1.05	1.102	V	2
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep voltage		0.55		0.85	V	1, 2, 13
V_{CCDC4}	V_{CC} at Intel® Enhanced Deeper Sleep Voltage		0.5		0.8	V	
I_{CCDES}	I_{CC} for Intel® Core™ Duo Processor ULV				14	A	5
I_{CC}	Icc for Intel Core Duo Processor ULV						
	Processor Number	Core Frequency/Voltage					
	U2500 U2400 N/A	1.20 GHz and HFM V_{CC} 1.06 GHz and HFM V_{CC} 800 MHz and LFM V_{CC}			13.9 13.9 10.5	A	3, 12
$I_{AH,}$ I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM				 5.4 6.4	A	3,4
I_{SLP}	I_{CC} Sleep LFM HFM				 5.3 6.3	A	3,4
I_{DSLP}	I_{CC} Deep Sleep LFM HFM				 4.8 5.4	A	3,4
I_{DPRSLP}	I_{CC} Deeper Sleep				3.6	A	4

Table 9. Voltage and Current Specifications Intel Core Duo Processor Ultra Low Voltage (ULV) (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DC4}	I_{CCC} Intel Enhanced Deeper Sleep			3.3	A	4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at CPU Package Pin			600	A/µs	6, 8
I_{CCA}	I_{CC} for V_{CCA} Supply			120	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} supply after V_{CC} Stable			6.0 2.5	A A	11 10

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep technology, or C1E).
2. The voltage specifications are assumed to be measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. The I_{CCDES}(max) specification of 14A comprehends Intel Core Duo processor ultra low voltage HFM frequencies.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Reserved.
8. Measured at the bulk capacitors on the motherboard.
9. V_{CC}, boot tolerance is shown in Figure 3.
10. This is a steady-state Iccp current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
11. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
12. Specified at the nominal V_{CC}.
13. If a given Operating System C-State model is not based on the use of MWAIT or I/O Redirection, the processor Deeper Sleep VID will be same as LFM VID.

Table 10. Voltage and Current Specifications for Intel Core Solo Processor ULV (Ultra Low Voltage) (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)	0.85		1.1	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)	0.8		1.0	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		1.20		V	2, 8
V_{CCP}	AGTL+ Termination Voltage	0.997	1.05	1.102	V	2
V_{CCA}	PLL Supply Voltage	1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep Voltage	0.55		0.85	V	1, 2, 12
V_{CCDC4}	V_{CC} at Intel Enhanced Deeper Sleep Voltage	0.50		0.80	V	1, 2
I_{CCDES}	I_{CC} for Intel® Core™ Solo Processor ULV			8	A	5

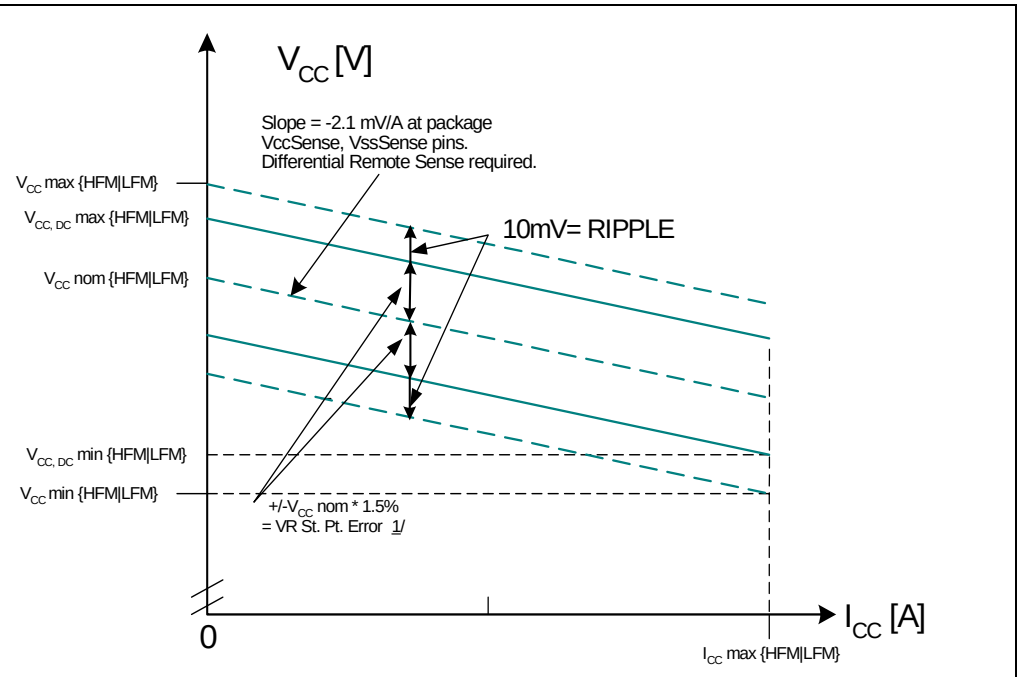
Table 10. Voltage and Current Specifications for Intel Core Solo Processor ULV (Ultra Low Voltage) (Sheet 2 of 2)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
I_{CC}	I_{CC} for Intel Core Solo Processor ULV						
	Processor Number	Core Frequency/Voltage					
	U1500 U1400 U1300 N/A	1.33 GHz and HFM V_{CC} 1.20 GHz and HFM V_{CC} 1.06 GHz and HFM V_{CC} 800 MHz and LFM V_{CC}			8 8 8 6.4	A	3,11
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM				 3.9 4.6	A	3,4
I_{SLP}	I_{CC} Sleep LFM HFM				 3.8 4.5	A	3,4
I_{DSLP}	I_{CC} Deep Sleep LFM HFM				 3.3 3.6	A	3,4
I_{DPRSLP}	I_{CC} Deeper Sleep				2.4	A	3,4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep				2.3	A	4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at CPU Package Pin				600	A/µs	6, 7
I_{CCA}	I_{CC} for V_{CCA} Supply				120	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable				6.0 2.5	A A	10 9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or C1E).
2. The voltage specifications are assumed to be measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. This specification comprehends Intel Core Duo processor ULV processor HFM frequencies.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. Vcc, boot tolerance is shown in Figure 5.
9. This is a steady-state I_{CCP} current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
11. Specified at the nominal V_{CC}.
12. If a given Operating System C-State model is not based on the use of MWAIT or I/O Redirection, the processor Deeper Sleep VID will be same as LFM VID.

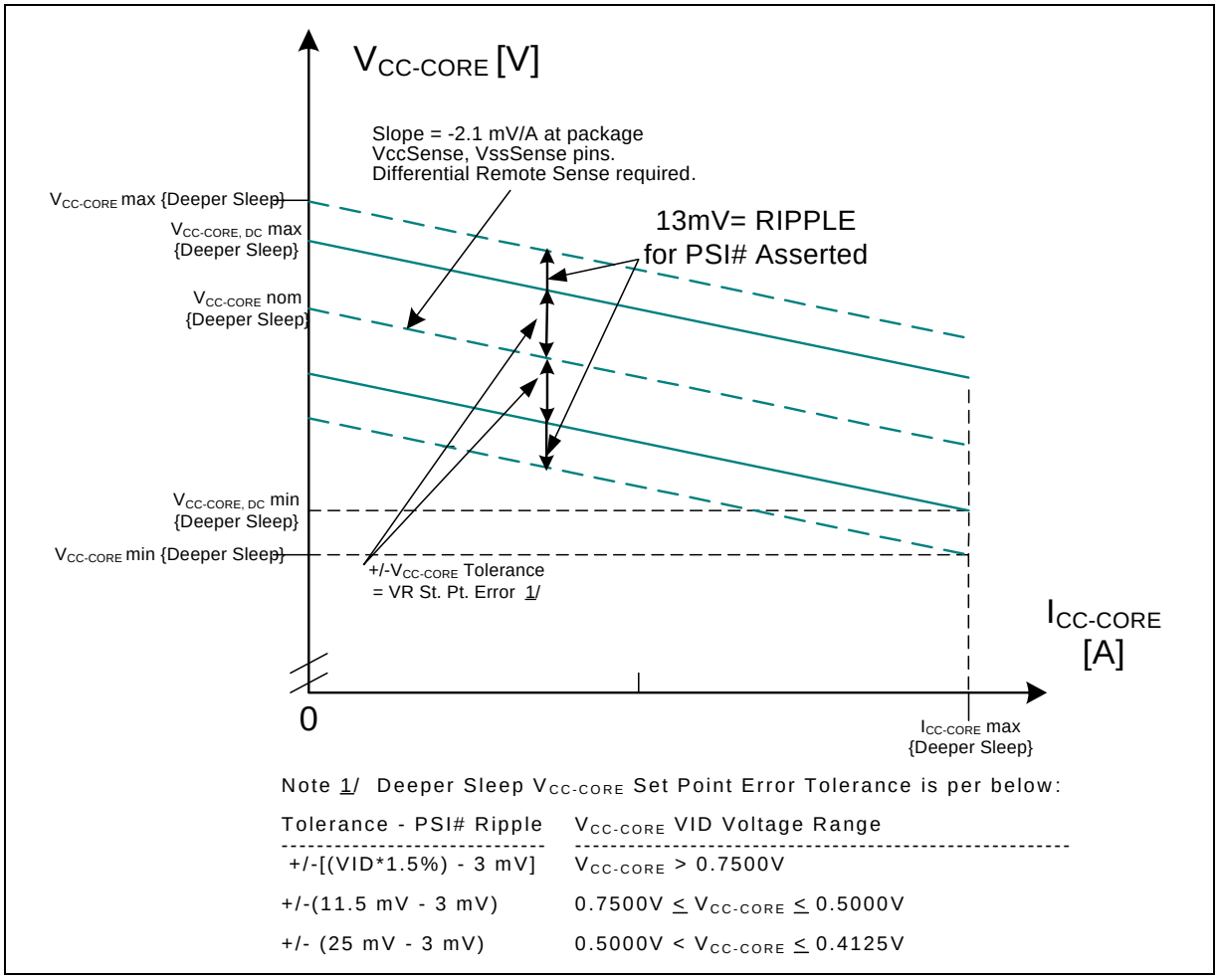
Figure 3. Active V_{CC} and I_{CC} Loadline for Intel Core Duo Processor (SV, LV & ULV) and Intel Core Solo Processor SV



Note 1/ V_{CC} Set Point Error Tolerance is per below:

Tolerance	V_{CC} Active Mode VID Code Range
+/-1.5%	V_{CC} > 0.7500V (VID 0111100).
+/-11.5mV	$V_{CC} \leq$ 0.7500V (VID 0111100)

Figure 4. Deeper Sleep V_{CC} and I_{CC} Loadline for Intel Core Duo Processor (SV, LV & ULV) and Intel Core Solo Processor SV

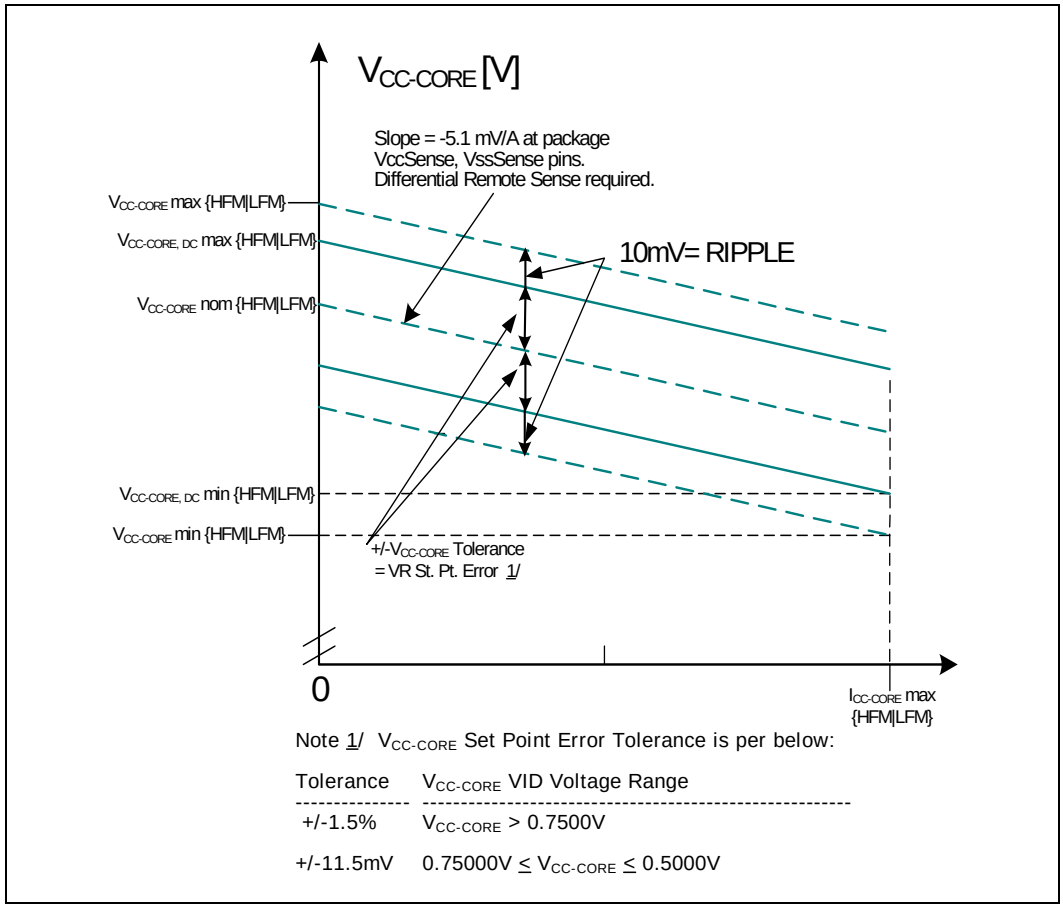


Note 1/ Deeper Sleep $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance - PSI# Ripple	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-[(VID*1.5%) - 3 mV]	$V_{CC\text{-}CORE} > 0.7500V$
+/-(11.5 mV - 3 mV)	$0.7500V \leq V_{CC\text{-}CORE} \leq 0.5000V$
+/- (25 mV - 3 mV)	$0.5000V < V_{CC\text{-}CORE} \leq 0.4125V$

NOTE: For low voltage, if PSI# is not asserted, then the 13-mV ripple allowance becomes 10 mV.

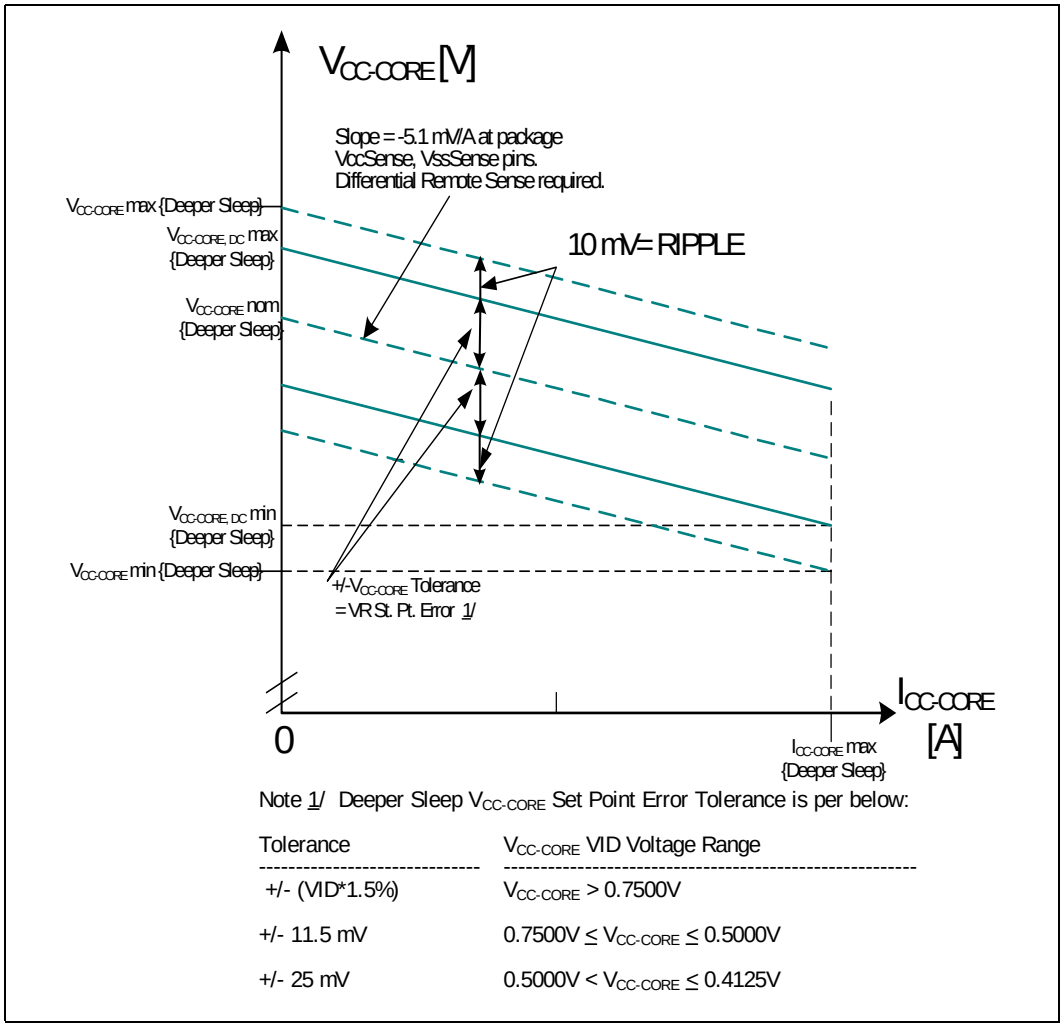
Figure 5. Active V_{CC} and I_{CC} Loadline for Intel Core Solo Processor ULV



Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-1.5%	$V_{CC\text{-}CORE} > 0.7500V$
+/-11.5mV	$0.75000V \leq V_{CC\text{-}CORE} \leq 0.5000V$

Figure 6. Deeper Sleep V_{CC} and I_{CC} Loadline for Intel Core Solo Processor ULV



Note 1/ Deeper Sleep $V_{CC-CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC-CORE}$ VID Voltage Range
+/- (VID*1.5%)	$V_{CC-CORE} > 0.7500V$
+/- 11.5 mV	$0.7500V \leq V_{CC-CORE} \leq 0.5000V$
+/- 25 mV	$0.5000V < V_{CC-CORE} \leq 0.4125V$

Table 11. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage		0		V	
V_{IH}	Input High Voltage	0.660	0.710	0.85	V	
V_{CROSS}	Crossing Voltage	0.25	0.35	0.55	V	2
ΔV_{CROSS}	Range of Crossing Points			0.14	V	6
V_{TH}	Threshold Region	V_{CROSS} -0.100		V_{CROSS}+0.100	V	3
I_{LI}	Input Leakage Current			± 100	µA	4
Cpad	Pad Capacitance	0.95	1.2	1.45	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. Threshold Region is defined as a region entered about the crossing voltage in which the differential receiver switches. It includes input threshold hysteresis.
4. For Vin between 0 V and V_{IH}.
5. Cpad includes die capacitance only. No package parasitics are included.
6. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.

Table 12. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	0.997	1.05	1.102	V	
GTLREF	Reference Voltage		2/3 V_{CCP}		V	6
V_{IH}	Input High Voltage	GTLREF+0.1		V_{CCP}+0.1	V	3,6
V_{IL}	Input Low Voltage	-0.1	0	GTLREF-0.1	V	2,4
V_{OH}	Output High Voltage		V_{CCP}			6
R_{TT}	Termination Resistance	50	55	61	Ω	7,10
R_{ON}	Buffer on Resistance	22.3	25.5	28.7	Ω	5
I_{LI}	Input Leakage Current			± 100	µA	8
Cpad	Pad Capacitance	1.8	2.3	2.75	pF	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance.
6. GTLREF should be generated from V_{CCP} with a 1% tolerance resistor divider. Tolerance of resistor divider decides the tolerance of GTLREF. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver.
8. Specified with on die R_{TT} and R_{ON} are turned off.
9. Cpad includes die capacitance only. No package parasitics are included.
10. This spec applies to all AGTL+ signals except for PREQ#. R_{TT} for PREQ# is between 1.5 kΩ to 6.0 kΩ.

Table 13. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.0	1.05	1.10	V	
V_{IL}	Input Low Voltage CMOS	-0.1	0.0	0.33	V	2, 3
V_{IH}	Input High Voltage	0.7	1.05	1.20	V	2
V_{OL}	Output Low Voltage	-0.1	0	0.11	V	2
V_{OH}	Output High Voltage	0.9	V_{CCP}	1.20	V	2
I_{OL}	Output Low Current	1.3		4.1	mA	4
I_{OH}	Output High Current	1.3		4.1	mA	5
I_{LI}	Input Leakage Current			±100	µA	6
Cpad1	Pad Capacitance	1.8	2.3	2.75	pF	7
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45	pF	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Reserved.
4. Measured at $0.1*V_{CCP}$.
5. Measured at $0.9*V_{CCP}$.
6. For Vin between 0 V and V_{CCP}. Measured when the driver is tristated.
7. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#,PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 14. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	1.0	1.05	1.10	V	3
V_{OL}	Output Low Voltage	0		0.20	V	
I_{OL}	Output Low Current	11.40		50	mA	2
I_{Leak}	Output Leakage Current			±200	µA	4
Cpad	Pad Capacitance	1.8	2.3	2.75	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at $0.2*V_{CCP}$.
3. V_{OH} is determined by value of the external pullup resistor to V_{CCP}. Please contact your Intel representative for details.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

§

4 Package Mechanical Specifications and Pin Information

4.1 Package Mechanical Specifications

The Intel Core Duo processor and Intel Core Solo processor are available in 478-pin Micro-FCPGA and 479-ball Micro-FCBGA packages. The package mechanical dimensions are shown in Figure 7 through Figure 10. Table 15 (two sheets) shows a top-view of package pin-out with their functionalities.

Warning: The Micro-FCBGA package incorporates land-side capacitors. The land-side capacitors are electrically conductive, care should be taken to avoid contacting the capacitors with other electrically conductive materials on the motherboard. Doing so may short the capacitors, and possibly damage the device or render it inactive.

4.1.1 Package Mechanical Drawings

Different views showing all pertinent dimensions of the Micro-FCPGA package are shown in Figure 7 and continued in Figure 8. Views and pertinent dimensions for Micro-FCBGA package are shown in Figure 9 and continued in Figure 10.

Figure 7. Micro-FCPGA Processor Package Drawing (Sheet 1 of 2)

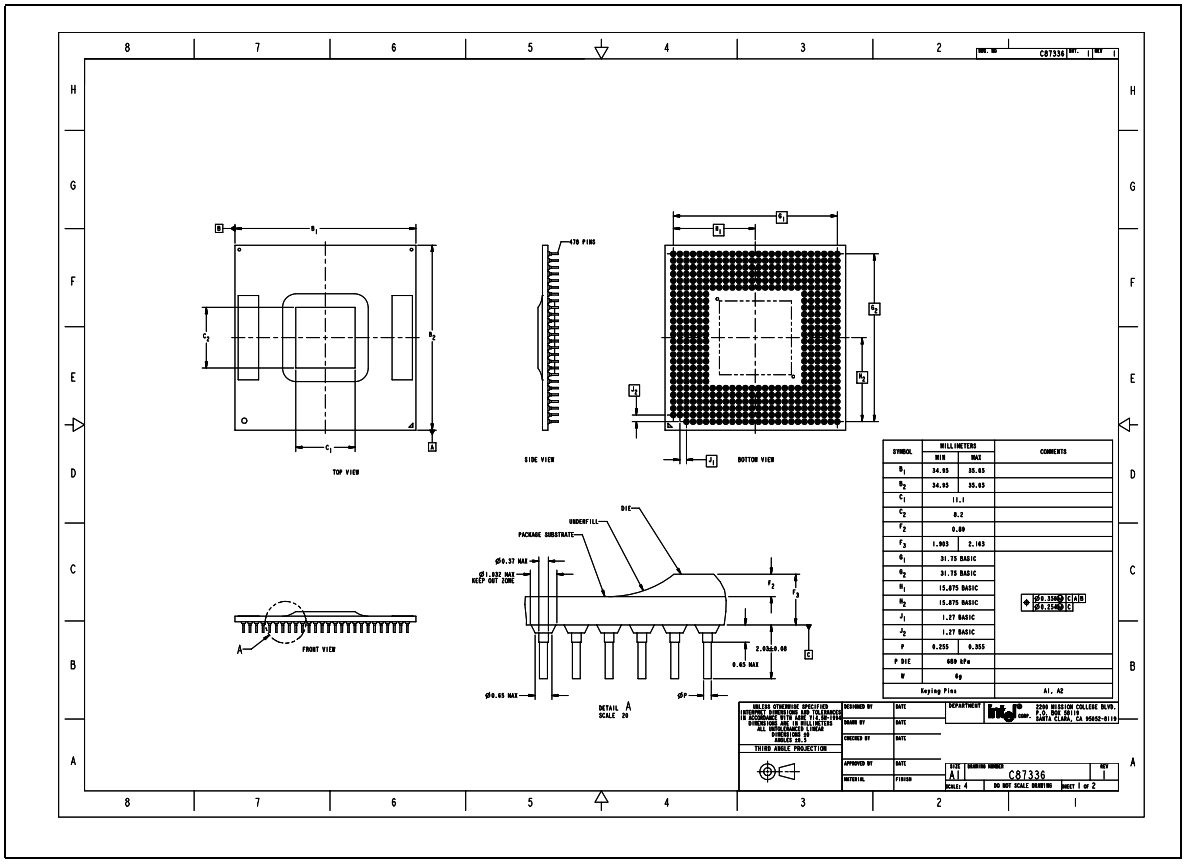


Figure 8. Micro-FCPGA Processor Package Drawing (Sheet 2 of 2)

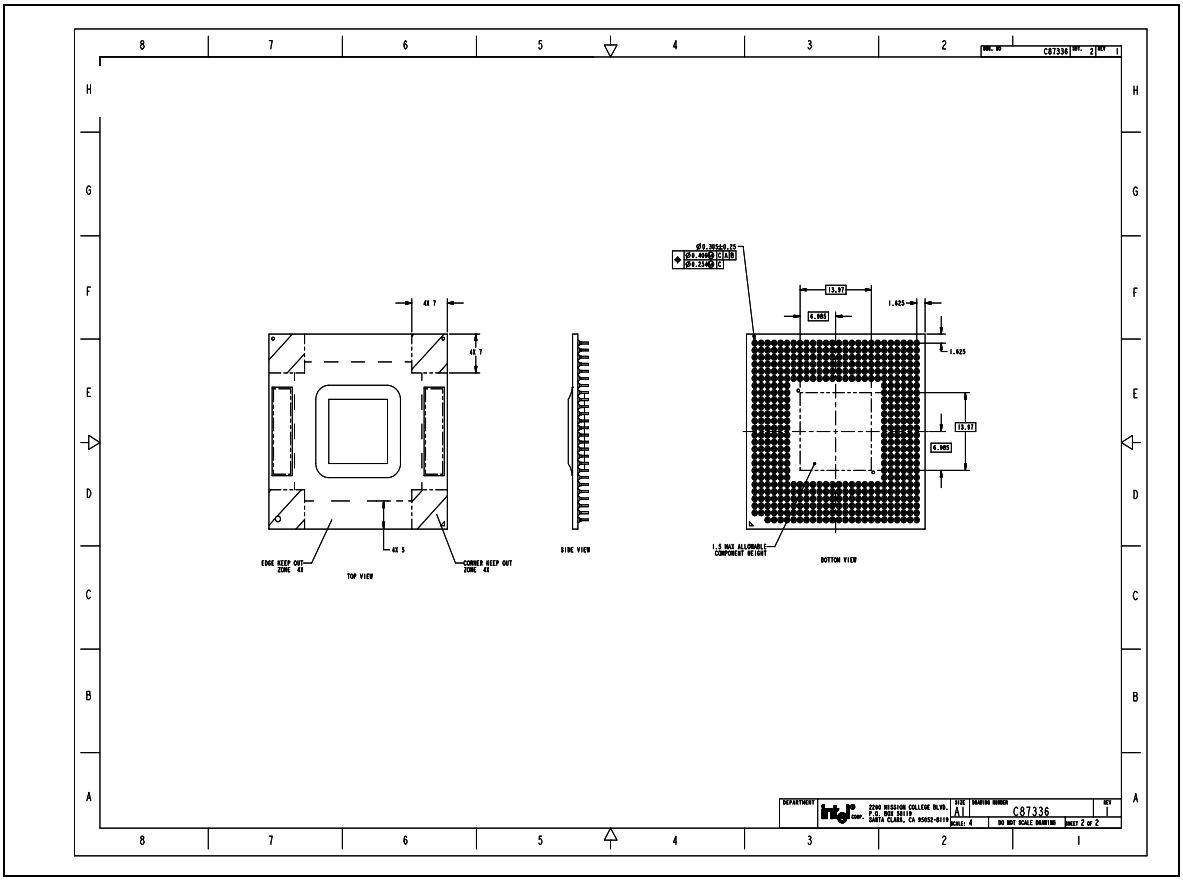


Figure 9. Micro-FCBGA Processor Package Drawing (Sheet 1 of 2)

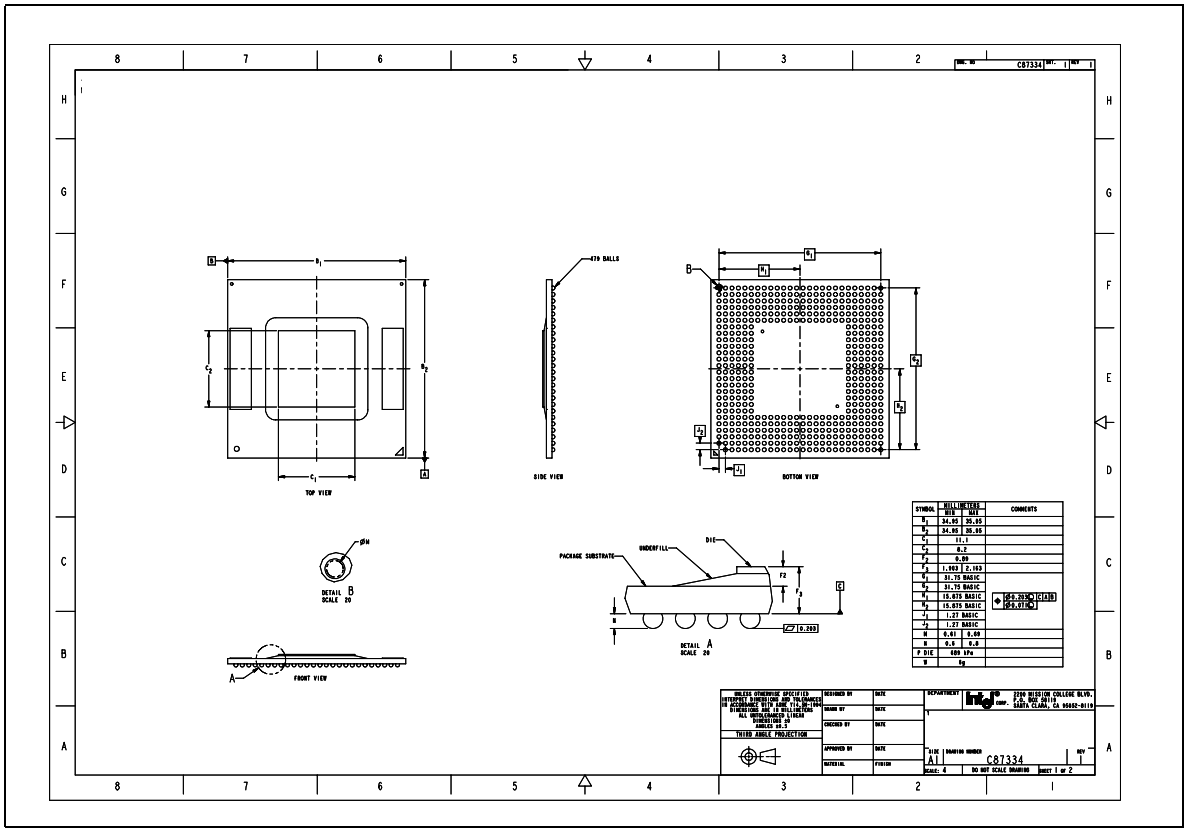
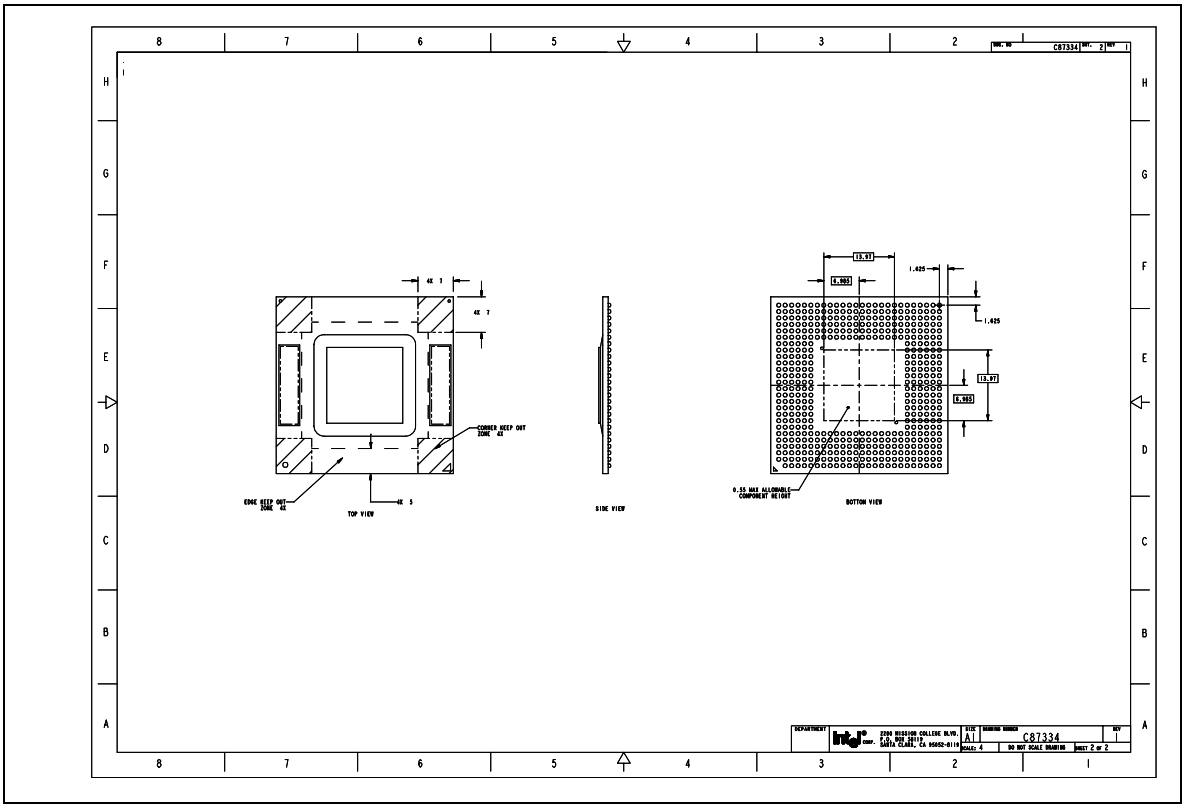


Figure 10. Micro-FCBGA Processor Package Drawing (Sheet 2 of 2)



4.1.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted in the keep-out areas. The location and quantity of the capacitors may change, but will remain within the component keep-in. See Figure 7 and Figure 9 for keep-out zones.

4.1.3 Package Loading Specifications

Maximum mechanical package loading specifications are given in Figure 7 and Figure 9. These specifications are static compressive loading in the direction normal to the processor. This maximum load limit should not be exceeded during shipping conditions, standard use condition, or by thermal solution. In addition, there are additional load limitations against transient bend, shock, and tensile loading. These limitations are more platform specific, and should be obtained by contacting your field support. Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution.

4.1.4 Processor Mass Specifications

The typical mass of the processor is given in Figure 7 and Figure 9. This mass includes all the components that are included in the package.

4.2 Processor Pinout and Pin List

Table 15 shows the top view pinout of the processor. The pin list arranged in two different formats is shown in the following pages.

Table 15. The Coordinates of the Processor Pins as Viewed from the Top of the Package (Sheet 1 of 2)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A			SMI#	VSS	FERR#	A20M#	VCC	VSS	VCC	VCC	VSS	VCC	VCC	A
B	RESET#	RSVD	INIT#	LINT1	DPSLP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	B
C	RSVD	VSS	RSVD	IGNNE#	VSS	LINT0	THERMTRIP#	VSS	VCC	VCC	VSS	VCC	VCC	C
D	VSS	RSVD	RSVD	VSS	STPCLK#	PWRGOOD	SLP#	VSS	VCC	VCC	VSS	VCC	VSS	D
E	DBSY#	BNR#	VSS	HITM#	DPRSTP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	E
F	BR0#	VSS	RS[0]#	RS[1]#	VSS	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VSS	F
G	VSS	TRDY#	RS[2]#	VSS	BPRI#	HIT#								G
H	ADS#	REQ[1]#	VSS	LOCK#	DEFER#	VSS								H
J	A[9]#	VSS	REQ[3]#	A[3]#	VSS	VCCP								J
K	VSS	REQ[2]#	REQ[0]#	VSS	A[6]#	VCCP								K
L	A[13]#	ADSTB[0]#	VSS	A[4]#	REQ[4]#	VSS								L
M	A[7]#	VSS	A[5]#	RSVD	VSS	VCCP								M
N	VSS	A[8]#	A[10]#	VSS	RSVD	VCCP								N
P	A[15]#	A[12]#	VSS	A[14]#	A[11]#	VSS								P
R	A[16]#	VSS	A[19]#	A[24]#	VSS	VCCP								R
T	VSS	RSVD	A[26]#	VSS	A[25]#	VCCP								T
U	COMP[2]	A[23]#	VSS	A[21]#	A[18]#	VSS								U
V	COMP[3]	VSS	RSVD	ADSTB[1]#	VSS	VCCP								V
W	VSS	A[30]#	A[27]#	VSS	A[28]#	A[20]#								W
Y	A[31]#	A[17]#	VSS	A[29]#	A[22]#	VSS								Y
AA	RSVD	VSS	RSVD	RSVD	VSS	TDI	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AA
AB	VSS	RSVD	TDO	VSS	TMS	TRST#	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AB
AC	PREQ#	PRDY#	VSS	BPM[3]#	TCK	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AC
AD	BPM[2]#	VSS	BPM[1]#	BPM[0]#	VSS	VID[0]	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AD
AE	VSS	VID[6]	VID[4]	VSS	VID[2]	PSI#	VSS SENSE	VSS	VCC	VCC	VSS	VCC	VCC	AE
AF	RSVD	VID[5]	VSS	VID[3]	VID[1]	VSS	VCC SENSE	VSS	VCC	VCC	VSS	VCC	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Table 16. The Coordinates of the Processor Pins as Viewed from the Top of the Package (Sheet 2 of 2)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VCC	VSS	VCC	VCC	VSS	VCC	BCLK[1]	BCLK[0]	VSS	THRMDA	THRMDC	VSS	A
B	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	BSEL[0]	BSEL[1]	VSS	RSVD	VCCA	B
C	VSS	VCC	VSS	VCC	VCC	VSS	DBR#	BSEL[2]	VSS	RSVD	RSVD	VSS	TEST1	C
D	VCC	VCC	VSS	VCC	VCC	VSS	IERR#	PROC HOT#	RSVD	VSS	DPWR#	TEST2	VSS	D
E	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[0]#	D[7]#	VSS	D[6]#	D[2]#	E
F	VCC	VCC	VSS	VCC	VCC	VSS	VCC	DRDY#	VSS	D[4]#	D[1]#	VSS	D[13]#	F
G								VCCP	DSTBP[0]#	VSS	D[9]#	D[5]#	VSS	G
H								VSS	D[3]#	DSTBN[0]#	VSS	D[15]#	D[12]#	H
J								VCCP	VSS	D[11]#	D[10]#	VSS	DINV[0]#	J
K								VCCP	D[14]#	VSS	D[8]#	D[17]#	VSS	K
L								VSS	D[21]#	D[22]#	VSS	D[20]#	D[29]#	L
M								VCCP	VSS	D[23]#	DSTBN[1]#	VSS	DINV[1]#	M
N								VCCP	D[16]#	VSS	D[31]#	DSTBP[1]#	VSS	N
P								VSS	D[25]#	D[26]#	VSS	D[24]#	D[18]#	P
R								VCCP	VSS	D[19]#	D[28]#	VSS	COMP[0]	R
T								VCCP	RSVD	VSS	D[27]#	D[30]#	VSS	T
U								VSS	D[39]#	D[37]#	VSS	D[38]#	COMP[1]	U
V								VCCP	VSS	DINV[2]#	D[34]#	VSS	D[35]#	V
W								VCCP	D[41]#	VSS	DSTBN[2]#	D[36]#	VSS	W
Y								VSS	D[45]#	D[42]#	VSS	DSTBP[2]#	D[44]#	Y
AA	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[51]#	VSS	D[32]#	D[47]#	VSS	D[43]#	AA
AB	VCC	VCC	VSS	VCC	VCC	VSS	VCC	D[52]#	D[50]#	VSS	D[33]#	D[40]#	VSS	AB
AC	VSS	VCC	VSS	VCC	VCC	VSS	DINV[3]#	VSS	D[48]#	D[49]#	VSS	D[53]#	D[46]#	AC
AD	VCC	VCC	VSS	VCC	VCC	VSS	D[54]#	D[59]#	VSS	DSTBN[3]#	D[57]#	VSS	GTLREF	AD
AE	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[58]#	D[55]#	VSS	DSTBP[3]#	D[60]#	VSS	AE
AF	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[62]#	D[56]#	VSS	D[61]#	D[63]#	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

4.3 Alphabetical Signals Reference

Table 17. Signal Description (Sheet 1 of 9)

Name	Type	Description
A[31:3]#	Input/ Output	A[31:3]# (Address) define a 2^{32}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel® Core™ Duo processor and the Intel® Core™ Solo processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[31:17]# — ADSTB[1]#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Table 17. Signal Description (Sheet 2 of 9)

Name	Type	Description
BPM[2:1]# BPM[3,0]#	Output Input/ Output	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all processor FSB agents.This includes debug or performance monitoring tools. Please contact your Intel representative for more detailed information.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and the Mobile Intel® 945 Express Chipset family (High Priority Agent).
BSEL[2:0]	Output	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The processor operates at 667-MHz or 533-MHz system bus frequency (166-MHz or 133-MHz BCLK[1:0] frequency, respectively).
COMP[3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Please contact your Intel representative for more implementation details.

Table 17. Signal Description (Sheet 3 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN# / DSTBP#</th><th>DINV#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/ Output agent. This signal must connect the appropriate pins of both FSB agents.</td></tr>
</table>

Table 17. Signal Description (Sheet 4 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DINV[3:0]#</td><td>Input/ Output</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment to Data Bus<table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DINV[3]#</td><td>D[63:48]#</td></tr><tr><td>DINV[2]#</td><td>D[47:32]#</td></tr><tr><td>DINV[1]#</td><td>D[31:16]#</td></tr><tr><td>DINV[0]#</td><td>D[15:0]#</td></tr></table></td></tr>
<tr><td>DPRSTP#</td><td>Input</td><td>DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the Intel® ICH7M chipset.</td></tr>
<tr><td>DPSLP#</td><td>Input</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSLP# must be deasserted. DPSLP# is driven by the ICH7M chipset.</td></tr>
<tr><td>DPWR#</td><td>Input</td><td>DPWR# is a control signal from the Mobile Intel 945 Express Chipset family used to reduce power on the processor data bus input buffers.</td></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr></table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr></table></td></tr>
</table>

Table 17. Signal Description (Sheet 5 of 9)

Name	Type	Description
FERR#/PBE#	Output	FERR# (Floating-point Error)PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® Architecture Software Developer's Manual* and *AP-485*, *Intel® Processor Identification and CPUID Instruction Application Note*. For termination requirements please contact your Intel representative.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Please contact your Intel representative for more information regarding GTLREF implementation.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. For termination requirements please contact your Intel representative.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction.

Table 17. Signal Description (Sheet 6 of 9)

Name	Type	Description
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST). For termination requirements please contact your Intel representative.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/ INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness. Please contact your Intel representative for more implementation details.
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor. Please contact your Intel representative for more implementation details.

Table 17. Signal Description (Sheet 7 of 9)

Name	Type	Description
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. By default PROCHOT# is configured as an output only. Bidirectional PROCHOT# must be enabled via the BIOS. For termination requirements please contact your Intel representative. This signal may require voltage translation on the motherboard. Please contact your Intel representative for more details.
PSI#	Output	Processor Power Status Indicator signal. This signal is asserted when the processor is in a normal state (HFM and LFM) and lower state (Deep Sleep and Deeper Sleep). Please contact your Intel representative for more details on the PSI# signal.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. For termination requirements please contact your Intel representative.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. For termination requirements please contact your Intel representative and implementation details. There is a 55 Ω (nominal) on die pull-up resistor on this signal.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved /No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please contact your Intel representative for more details.

Table 17. Signal Description (Sheet 8 of 9)

Name	Type	Description
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port). Please contact your Intel representative for termination requirements and implementation details.
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. Please contact your Intel representative for termination requirements and implementation details.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. Please contact your Intel representative for termination requirements and implementation details.
TEST1	Input	TEST1 must have a stuffing option of separate pull-down resistor to V_{SS}. Please contact your Intel representative for more detailed information.
TEST2	Input	TEST2 must have a 51 Ω ±5% pull-down resistor to V_{SS}. Please contact your Intel representative for more details.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.

Table 17. Signal Description (Sheet 9 of 9)

Name	Type	Description
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. For termination requirements please contact your Intel representative.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. Please contact your Intel representative for termination requirements and implementation details.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents. Please contact your Intel representative for termination requirements and implementation details.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Please contact your Intel representative for termination requirements and implementation details.
V_{CC}	Input	Processor core power supply.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLL's. Please contact your Intel representative for complete implementation details.
V_{CCP}	Input	Processor I/O Power Supply.
$V_{CCSENSE}$	Output	$V_{CCSENSE}$ together with $V_{SSSENSE}$ are voltage feedback signals to IMVP6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense voltage near the silicon with little noise. Please contact your Intel Representative for more information regarding termination and routing recommendations.
VID[6:0]	Output	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Core Duo processor and Intel Core Solo processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ together with $V_{CCSENSE}$ are voltage feedback signals to Intel® MVP6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense ground near the silicon with little noise. Please contact your Intel Representative for more information regarding termination and routing recommendations.

§

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A[3]#	J4	Source Synch	Input/ Output
A[4]#	L4	Source Synch	Input/ Output
A[5]#	M3	Source Synch	Input/ Output
A[6]#	K5	Source Synch	Input/ Output
A[7]#	M1	Source Synch	Input/ Output
A[8]#	N2	Source Synch	Input/ Output
A[9]#	J1	Source Synch	Input/ Output
A[10]#	N3	Source Synch	Input/ Output
A[11]#	P5	Source Synch	Input/ Output
A[12]#	P2	Source Synch	Input/ Output
A[13]#	L1	Source Synch	Input/ Output
A[14]#	P4	Source Synch	Input/ Output
A[15]#	P1	Source Synch	Input/ Output
A[16]#	R1	Source Synch	Input/ Output
A[17]#	Y2	Source Synch	Input/ Output
A[18]#	U5	Source Synch	Input/ Output
A[19]#	R3	Source Synch	Input/ Output
A[20]#	W6	Source Synch	Input/ Output
A[21]#	U4	Source Synch	Input/ Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A[22]#	Y5	Source Synch	Input/ Output
A[23]#	U2	Source Synch	Input/ Output
A[24]#	R4	Source Synch	Input/ Output
A[25]#	T5	Source Synch	Input/ Output
A[26]#	T3	Source Synch	Input/ Output
A[27]#	W3	Source Synch	Input/ Output
A[28]#	W5	Source Synch	Input/ Output
A[29]#	Y4	Source Synch	Input/ Output
A[30]#	W2	Source Synch	Input/ Output
A[31]#	Y1	Source Synch	Input/ Output
A20M#	A6	CMOS	Input
ADS#	H1	Common Clock	Input/ Output
ADSTB[0]#	L2	Source Synch	Input/ Output
ADSTB[1]#	V4	Source Synch	Input/ Output
BCLK[0]	A22	Bus Clock	Input
BCLK[1]	A21	Bus Clock	Input
BNR#	E2	Common Clock	Input/ Output
BPM[0]#	AD4	Common Clock	Input/ Output
BPM[1]#	AD3	Common Clock	Output
BPM[2]#	AD1	Common Clock	Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
BPM[3]#	AC4	Common Clock	Input/ Output
BPRI#	G5	Common Clock	Input
BR0#	F1	Common Clock	Input/ Output
BSEL[0]	B22	CMOS	Output
BSEL[1]	B23	CMOS	Output
BSEL[2]	C21	CMOS	Output
COMP[0]	R26	Power/Other	Input/ Output
COMP[1]	U26	Power/Other	Input/ Output
COMP[2]	U1	Power/Other	Input/ Output
COMP[3]	V1	Power/Other	Input/ Output
D[0]#	E22	Source Synch	Input/ Output
D[1]#	F24	Source Synch	Input/ Output
D[2]#	E26	Source Synch	Input/ Output
D[3]#	H22	Source Synch	Input/ Output
D[4]#	F23	Source Synch	Input/ Output
D[5]#	G25	Source Synch	Input/ Output
D[6]#	E25	Source Synch	Input/ Output
D[7]#	E23	Source Synch	Input/ Output
D[8]#	K24	Source Synch	Input/ Output
D[9]#	G24	Source Synch	Input/ Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D[10]#	J24	Source Synch	Input/ Output
D[11]#	J23	Source Synch	Input/ Output
D[12]#	H26	Source Synch	Input/ Output
D[13]#	F26	Source Synch	Input/ Output
D[14]#	K22	Source Synch	Input/ Output
D[15]#	H25	Source Synch	Input/ Output
D[16]#	N22	Source Synch	Input/ Output
D[17]#	K25	Source Synch	Input/ Output
D[18]#	P26	Source Synch	Input/ Output
D[19]#	R23	Source Synch	Input/ Output
D[20]#	L25	Source Synch	Input/ Output
D[21]#	L22	Source Synch	Input/ Output
D[22]#	L23	Source Synch	Input/ Output
D[23]#	M23	Source Synch	Input/ Output
D[24]#	P25	Source Synch	Input/ Output
D[25]#	P22	Source Synch	Input/ Output
D[26]#	P23	Source Synch	Input/ Output
D[27]#	T24	Source Synch	Input/ Output
D[28]#	R24	Source Synch	Input/ Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D[29]#	L26	Source Synch	Input/ Output
D[30]#	T25	Source Synch	Input/ Output
D[31]#	N24	Source Synch	Input/ Output
D[32]#	AA23	Source Synch	Input/ Output
D[33]#	AB24	Source Synch	Input/ Output
D[34]#	V24	Source Synch	Input/ Output
D[35]#	V26	Source Synch	Input/ Output
D[36]#	W25	Source Synch	Input/ Output
D[37]#	U23	Source Synch	Input/ Output
D[38]#	U25	Source Synch	Input/ Output
D[39]#	U22	Source Synch	Input/ Output
D[40]#	AB25	Source Synch	Input/ Output
D[41]#	W22	Source Synch	Input/ Output
D[42]#	Y23	Source Synch	Input/ Output
D[43]#	AA26	Source Synch	Input/ Output
D[44]#	Y26	Source Synch	Input/ Output
D[45]#	Y22	Source Synch	Input/ Output
D[46]#	AC26	Source Synch	Input/ Output
D[47]#	AA24	Source Synch	Input/ Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D[48]#	AC22	Source Synch	Input/ Output
D[49]#	AC23	Source Synch	Input/ Output
D[50]#	AB22	Source Synch	Input/ Output
D[51]#	AA21	Source Synch	Input/ Output
D[52]#	AB21	Source Synch	Input/ Output
D[53]#	AC25	Source Synch	Input/ Output
D[54]#	AD20	Source Synch	Input/ Output
D[55]#	AE22	Source Synch	Input/ Output
D[56]#	AF23	Source Synch	Input/ Output
D[57]#	AD24	Source Synch	Input/ Output
D[58]#	AE21	Source Synch	Input/ Output
D[59]#	AD21	Source Synch	Input/ Output
D[60]#	AE25	Source Synch	Input/ Output
D[61]#	AF25	Source Synch	Input/ Output
D[62]#	AF22	Source Synch	Input/ Output
D[63]#	AF26	Source Synch	Input/ Output
DBR#	C20	CMOS	Output
DBSY#	E1	Common Clock	Input/ Output
DEFER#	H5	Common Clock	Input
DINV[0]#	J26	Source Synch	Input/ Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
DINV[1]#	M26	Source Synch	Input/ Output
DINV[2]#	V23	Source Synch	Input/ Output
DINV[3]#	AC20	Source Synch	Input/ Output
DPRSTP#	E5	CMOS	Input
DPSLP#	B5	CMOS	Input
DPWR#	D24	Common Clock	Input
DRDY#	F21	Common Clock	Input/ Output
DSTBN[0]#	H23	Source Synch	Input/ Output
DSTBN[1]#	M24	Source Synch	Input/ Output
DSTBN[2]#	W24	Source Synch	Input/ Output
DSTBN[3]#	AD23	Source Synch	Input/ Output
DSTBP[0]#	G22	Source Synch	Input/ Output
DSTBP[1]#	N25	Source Synch	Input/ Output
DSTBP[2]#	Y25	Source Synch	Input/ Output
DSTBP[3]#	AE24	Source Synch	Input/ Output
FERR#	A5	Open Drain	Output
GTLREF	AD26	Power/Other	Input
HIT#	G6	Common Clock	Input/ Output
HITM#	E4	Common Clock	Input/ Output
IERR#	D20	Open Drain	Output
IGNNE#	C4	CMOS	Input
INIT#	B3	CMOS	Input

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
LINT0	C6	CMOS	Input
LINT1	B4	CMOS	Input
LOCK#	H4	Common Clock	Input/ Output
PRDY#	AC2	Common Clock	Output
PREQ#	AC1	Common Clock	Input
PROCHOT#	D21	Open Drain	Input/ Output
PSI#	AE6	CMOS	Output
PWRGOOD	D6	CMOS	Input
REQ[0]#	K3	Source Synch	Input/ Output
REQ[1]#	H2	Source Synch	Input/ Output
REQ[2]#	K2	Source Synch	Input/ Output
REQ[3]#	J3	Source Synch	Input/ Output
REQ[4]#	L5	Source Synch	Input/ Output
RESET#	B1	Common Clock	Input
RS[0]#	F3	Common Clock	Input
RS[1]#	F4	Common Clock	Input
RS[2]#	G3	Common Clock	Input
RSVD	D2	Reserved	
RSVD	F6	Reserved	
RSVD	D3	Reserved	
RSVD	C1	Reserved	
RSVD	AF1	Reserved	
RSVD	D22	Reserved	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
RSVD	C23	Reserved	
RSVD	C24	Reserved	
RSVD	AA1	Reserved	
RSVD	AA4	Reserved	
RSVD	AB2	Reserved	
RSVD	AA3	Reserved	
RSVD	M4	Reserved	
RSVD	N5	Reserved	
RSVD	T2	Reserved	
RSVD	V3	Reserved	
RSVD	B2	Reserved	
RSVD	C3	Reserved	
RSVD	T22	Reserved	
RSVD	B25	Reserved	
SLP#	D7	CMOS	Input
SMI#	A3	CMOS	Input
STPCLK#	D5	CMOS	Input
TCK	AC5	CMOS	Input
TDI	AA6	CMOS	Input
TDO	AB3	Open Drain	Output
TEST1	C26	Test	
TEST2	D25	Test	
THERMDA	A24	Power/Other	
THERMDC	A25	Power/Other	
THERMTRIP#	C7	Open Drain	Output
TMS	AB5	CMOS	Input
TRDY#	G2	Common Clock	Input
TRST#	AB6	CMOS	Input
VCC	AB20	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AA20	Power/Other	
VCC	AF20	Power/Other	
VCC	AE20	Power/Other	
VCC	AB18	Power/Other	
VCC	AB17	Power/Other	
VCC	AA18	Power/Other	
VCC	AA17	Power/Other	
VCC	AD18	Power/Other	
VCC	AD17	Power/Other	
VCC	AC18	Power/Other	
VCC	AC17	Power/Other	
VCC	AF18	Power/Other	
VCC	AF17	Power/Other	
VCC	AE18	Power/Other	
VCC	AE17	Power/Other	
VCC	AB15	Power/Other	
VCC	AA15	Power/Other	
VCC	AD15	Power/Other	
VCC	AC15	Power/Other	
VCC	AF15	Power/Other	
VCC	AE15	Power/Other	
VCC	AB14	Power/Other	
VCC	AA13	Power/Other	
VCC	AD14	Power/Other	
VCC	AC13	Power/Other	
VCC	AF14	Power/Other	
VCC	AE13	Power/Other	
VCC	AB12	Power/Other	
VCC	AA12	Power/Other	
VCC	AD12	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AC12	Power/Other	
VCC	AF12	Power/Other	
VCC	AE12	Power/Other	
VCC	AB10	Power/Other	
VCC	AB9	Power/Other	
VCC	AA10	Power/Other	
VCC	AA9	Power/Other	
VCC	AD10	Power/Other	
VCC	AD9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC9	Power/Other	
VCC	AF10	Power/Other	
VCC	AF9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE9	Power/Other	
VCC	AB7	Power/Other	
VCC	AA7	Power/Other	
VCC	AD7	Power/Other	
VCC	AC7	Power/Other	
VCC	B20	Power/Other	
VCC	A20	Power/Other	
VCC	F20	Power/Other	
VCC	E20	Power/Other	
VCC	B18	Power/Other	
VCC	B17	Power/Other	
VCC	A18	Power/Other	
VCC	A17	Power/Other	
VCC	D18	Power/Other	
VCC	D17	Power/Other	
VCC	C18	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	C17	Power/Other	
VCC	F18	Power/Other	
VCC	F17	Power/Other	
VCC	E18	Power/Other	
VCC	E17	Power/Other	
VCC	B15	Power/Other	
VCC	A15	Power/Other	
VCC	D15	Power/Other	
VCC	C15	Power/Other	
VCC	F15	Power/Other	
VCC	E15	Power/Other	
VCC	B14	Power/Other	
VCC	A13	Power/Other	
VCC	D14	Power/Other	
VCC	C13	Power/Other	
VCC	F14	Power/Other	
VCC	E13	Power/Other	
VCC	B12	Power/Other	
VCC	A12	Power/Other	
VCC	D12	Power/Other	
VCC	C12	Power/Other	
VCC	F12	Power/Other	
VCC	E12	Power/Other	
VCC	B10	Power/Other	
VCC	B9	Power/Other	
VCC	A10	Power/Other	
VCC	A9	Power/Other	
VCC	D10	Power/Other	
VCC	D9	Power/Other	
VCC	C10	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	C9	Power/Other	
VCC	F10	Power/Other	
VCC	F9	Power/Other	
VCC	E10	Power/Other	
VCC	E9	Power/Other	
VCC	B7	Power/Other	
VCC	A7	Power/Other	
VCC	F7	Power/Other	
VCC	E7	Power/Other	
VCCA	B26	Power/Other	
VCCP	K6	Power/Other	
VCCP	J6	Power/Other	
VCCP	M6	Power/Other	
VCCP	N6	Power/Other	
VCCP	T6	Power/Other	
VCCP	R6	Power/Other	
VCCP	K21	Power/Other	
VCCP	J21	Power/Other	
VCCP	M21	Power/Other	
VCCP	N21	Power/Other	
VCCP	T21	Power/Other	
VCCP	R21	Power/Other	
VCCP	V21	Power/Other	
VCCP	W21	Power/Other	
VCCP	V6	Power/Other	
VCCP	G21	Power/Other	
VCCSENSE	AF7	Power/Other	
VID[0]	AD6	CMOS	Output
VID[1]	AF5	CMOS	Output
VID[2]	AE5	CMOS	Output

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VID[3]	AF4	CMOS	Output
VID[4]	AE3	CMOS	Output
VID[5]	AF2	CMOS	Output
VID[6]	AE2	CMOS	Output
VSS	AB26	Power/Other	
VSS	AA25	Power/Other	
VSS	AD25	Power/Other	
VSS	AE26	Power/Other	
VSS	AB23	Power/Other	
VSS	AC24	Power/Other	
VSS	AF24	Power/Other	
VSS	AE23	Power/Other	
VSS	AA22	Power/Other	
VSS	AD22	Power/Other	
VSS	AC21	Power/Other	
VSS	AF21	Power/Other	
VSS	AB19	Power/Other	
VSS	AA19	Power/Other	
VSS	AD19	Power/Other	
VSS	AC19	Power/Other	
VSS	AF19	Power/Other	
VSS	AE19	Power/Other	
VSS	AB16	Power/Other	
VSS	AA16	Power/Other	
VSS	AD16	Power/Other	
VSS	AC16	Power/Other	
VSS	AF16	Power/Other	
VSS	AE16	Power/Other	
VSS	AB13	Power/Other	
VSS	AA14	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AD13	Power/Other	
VSS	AC14	Power/Other	
VSS	AF13	Power/Other	
VSS	AE14	Power/Other	
VSS	AB11	Power/Other	
VSS	AA11	Power/Other	
VSS	AD11	Power/Other	
VSS	AC11	Power/Other	
VSS	AF11	Power/Other	
VSS	AE11	Power/Other	
VSS	AB8	Power/Other	
VSS	AA8	Power/Other	
VSS	AD8	Power/Other	
VSS	AC8	Power/Other	
VSS	AF8	Power/Other	
VSS	AE8	Power/Other	
VSS	AA5	Power/Other	
VSS	AD5	Power/Other	
VSS	AC6	Power/Other	
VSS	AF6	Power/Other	
VSS	AB4	Power/Other	
VSS	AC3	Power/Other	
VSS	AF3	Power/Other	
VSS	AE4	Power/Other	
VSS	AB1	Power/Other	
VSS	AA2	Power/Other	
VSS	AD2	Power/Other	
VSS	AE1	Power/Other	
VSS	B6	Power/Other	
VSS	C5	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	F5	Power/Other	
VSS	E6	Power/Other	
VSS	H6	Power/Other	
VSS	J5	Power/Other	
VSS	M5	Power/Other	
VSS	L6	Power/Other	
VSS	P6	Power/Other	
VSS	R5	Power/Other	
VSS	V5	Power/Other	
VSS	U6	Power/Other	
VSS	Y6	Power/Other	
VSS	A4	Power/Other	
VSS	D4	Power/Other	
VSS	E3	Power/Other	
VSS	H3	Power/Other	
VSS	G4	Power/Other	
VSS	K4	Power/Other	
VSS	L3	Power/Other	
VSS	P3	Power/Other	
VSS	N4	Power/Other	
VSS	T4	Power/Other	
VSS	U3	Power/Other	
VSS	Y3	Power/Other	
VSS	W4	Power/Other	
VSS	D1	Power/Other	
VSS	C2	Power/Other	
VSS	F2	Power/Other	
VSS	G1	Power/Other	
VSS	K1	Power/Other	
VSS	J2	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	M2	Power/Other	
VSS	N1	Power/Other	
VSS	T1	Power/Other	
VSS	R2	Power/Other	
VSS	V2	Power/Other	
VSS	W1	Power/Other	
VSS	A26	Power/Other	
VSS	D26	Power/Other	
VSS	C25	Power/Other	
VSS	F25	Power/Other	
VSS	B24	Power/Other	
VSS	A23	Power/Other	
VSS	D23	Power/Other	
VSS	E24	Power/Other	
VSS	B21	Power/Other	
VSS	C22	Power/Other	
VSS	F22	Power/Other	
VSS	E21	Power/Other	
VSS	B19	Power/Other	
VSS	A19	Power/Other	
VSS	D19	Power/Other	
VSS	C19	Power/Other	
VSS	F19	Power/Other	
VSS	E19	Power/Other	
VSS	B16	Power/Other	
VSS	A16	Power/Other	
VSS	D16	Power/Other	
VSS	C16	Power/Other	
VSS	F16	Power/Other	
VSS	E16	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	B13	Power/Other	
VSS	A14	Power/Other	
VSS	D13	Power/Other	
VSS	C14	Power/Other	
VSS	F13	Power/Other	
VSS	E14	Power/Other	
VSS	B11	Power/Other	
VSS	A11	Power/Other	
VSS	D11	Power/Other	
VSS	C11	Power/Other	
VSS	F11	Power/Other	
VSS	E11	Power/Other	
VSS	B8	Power/Other	
VSS	A8	Power/Other	
VSS	D8	Power/Other	
VSS	C8	Power/Other	
VSS	F8	Power/Other	
VSS	E8	Power/Other	
VSS	G26	Power/Other	
VSS	K26	Power/Other	
VSS	J25	Power/Other	
VSS	M25	Power/Other	
VSS	N26	Power/Other	
VSS	T26	Power/Other	
VSS	R25	Power/Other	
VSS	V25	Power/Other	
VSS	W26	Power/Other	
VSS	H24	Power/Other	
VSS	G23	Power/Other	
VSS	K23	Power/Other	

Table 18. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	L24	Power/Other	
VSS	P24	Power/Other	
VSS	N23	Power/Other	
VSS	T23	Power/Other	
VSS	U24	Power/Other	
VSS	Y24	Power/Other	
VSS	W23	Power/Other	
VSS	H21	Power/Other	
VSS	J22	Power/Other	
VSS	M22	Power/Other	
VSS	L21	Power/Other	
VSS	P21	Power/Other	
VSS	R22	Power/Other	
VSS	V22	Power/Other	
VSS	U21	Power/Other	
VSS	Y21	Power/Other	
VSSSENSE	AE7	Power/Other	Output

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A3	SMI#	CMOS	Input
A4	VSS	Power/Other	
A5	FERR#	Open Drain	Output
A6	A20M#	CMOS	Input
A7	VCC	Power/Other	
A8	VSS	Power/Other	
A9	VCC	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VCC	Power/Other	
A14	VSS	Power/Other	
A15	VCC	Power/Other	
A16	VSS	Power/Other	
A17	VCC	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	BCLK[1]	Bus Clock	Input
A22	BCLK[0]	Bus Clock	Input
A23	VSS	Power/Other	
A24	THERMDA	Power/Other	
A25	THERMDC	Power/Other	
A26	VSS	Power/Other	
AA1	RSVD	Reserved	
AA2	VSS	Power/Other	
AA3	RSVD	Reserved	
AA4	RSVD	Reserved	
AA5	VSS	Power/Other	
AA6	TDI	CMOS	Input

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AA7	VCC	Power/Other	
AA8	VSS	Power/other	
AA9	VCC	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VCC	Power/Other	
AA14	VSS	Power/Other	
AA15	VCC	Power/Other	
AA16	VSS	Power/Other	
AA17	VCC	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	VCC	Power/Other	
AA21	D[51]#	Source Synch	Input/ Output
AA22	VSS	Power/Other	
AA23	D[32]#	Source Synch	Input/ Output
AA24	D[47]#	Source Synch	Input/ Output
AA25	VSS	Power/Other	
AA26	D[43]#	Source Synch	Input/ Output
AB1	VSS	Power/Other	
AB2	RSVD	Reserved	
AB3	TDO	Open Drain	Output
AB4	VSS	Power/Other	
AB5	TMS	CMOS	Input
AB6	TRST#	CMOS	Input
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AB9	VCC	Power/Other	
AB10	VCC	Power/Other	
AB11	VSS	Power/Other	
AB12	VCC	Power/Other	
AB13	VSS	Power/Other	
AB14	VCC	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VCC	Power/Other	
AB19	VSS	Power/Other	
AB20	VCC	Power/Other	
AB21	D[52]#	Source Synch	Input/ Output
AB22	D[50]#	Source Synch	Input/ Output
AB23	VSS	Power/Other	
AB24	D[33]#	Source Synch	Input/ Output
AB25	D[40]#	Source Synch	Input/ Output
AB26	VSS	Power/Other	
AC1	PREQ#	Common Clock	Input
AC2	PRDY#	Common Clock	Output
AC3	VSS	Power/Other	
AC4	BPM[3]#	Common Clock	Input/ Output
AC5	TCK	CMOS	Input
AC6	VSS	Power/Other	
AC7	VCC	Power/Other	
AC8	VSS	Power/Other	
AC9	VCC	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VCC	Power/Other	
AC14	VSS	Power/Other	
AC15	VCC	Power/Other	
AC16	VSS	Power/Other	
AC17	VCC	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	DINV[3]#	Source Synch	Input/ Output
AC21	VSS	Power/Other	
AC22	D[48]#	Source Synch	Input/ Output
AC23	D[49]#	Source Synch	Input/ Output
AC24	VSS	Power/Other	
AC25	D[53]#	Source Synch	Input/ Output
AC26	D[46]#	Source Synch	Input/ Output
AD1	BPM[2]#	Common Clock	Output
AD2	VSS	Power/Other	
AD3	BPM[1]#	Common Clock	Output
AD4	BPM[0]#	Common Clock	Input/ Output
AD5	VSS	Power/Other	
AD6	VID[0]	CMOS	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AD10	VCC	Power/Other	
AD11	VSS	Power/Other	
AD12	VCC	Power/Other	
AD13	VSS	Power/Other	
AD14	VCC	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VCC	Power/Other	
AD19	VSS	Power/Other	
AD20	D[54]#	Source Synch	Input/ Output
AD21	D[59]#	Source Synch	Input/ Output
AD22	VSS	Power/Other	
AD23	DSTBN[3] #	Source Synch	Input/ Output
AD24	D[57]#	Source Synch	Input/ Output
AD25	VSS	Power/Other	
AD26	GTLREF	Power/Other	Input
AE1	VSS	Power/Other	
AE2	VID[6]	CMOS	Output
AE3	VID[4]	CMOS	Output
AE4	VSS	Power/Other	
AE5	VID[2]	CMOS	Output
AE6	PSI#	CMOS	Output
AE7	VSSSENSE	Power/Other	Output
AE8	VSS	Power/Other	
AE9	VCC	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AE12	VCC	Power/Other	
AE13	VCC	Power/Other	
AE14	VSS	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VCC	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	D[58]#	Source Synch	Input/ Output
AE22	D[55]#	Source Synch	Input/ Output
AE23	VSS	Power/Other	
AE24	DSTBP[3] #	Source Synch	Input/ Output
AE25	D[60]#	Source Synch	Input/ Output
AE26	VSS	Power/Other	
AF1	RSVD	Reserved	
AF2	VID[5]	CMOS	Output
AF3	VSS	Power/Other	
AF4	VID[3]	CMOS	Output
AF5	VID[1]	CMOS	Output
AF6	VSS	Power/Other	
AF7	VCCSENSE	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VCC	Power/Other	
AF11	VSS	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AF14	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VCC	Power/Other	
AF19	VSS	Power/Other	
AF20	VCC	Power/Other	
AF21	VSS	Power/Other	
AF22	D[62]#	Source Synch	Input/ Output
AF23	D[56]#	Source Synch	Input/ Output
AF24	VSS	Power/Other	
AF25	D[61]#	Source Synch	Input/ Output
AF26	D[63]#	Source Synch	Input/ Output
B1	RESET#	Common Clock	Input
B2	RSVD	Reserved	
B3	INIT#	CMOS	Input
B4	LINT1	CMOS	Input
B5	DPSLP#	CMOS	Input
B6	VSS	Power/Other	
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VCC	Power/Other	
B11	VSS	Power/Other	
B12	VCC	Power/Other	
B13	VSS	Power/Other	
B14	VCC	Power/Other	
B15	VCC	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VCC	Power/Other	
B19	VSS	Power/Other	
B20	VCC	Power/Other	
B21	VSS	Power/Other	
B22	BSEL[0]	CMOS	Output
B23	BSEL[1]	CMOS	Output
B24	VSS	Power/Other	
B25	RSVD	Reserved	
B26	VCCA	Power/Other	
C1	RSVD	Reserved	
C2	VSS	Power/Other	
C3	RSVD	Reserved	
C4	IGNNE#	CMOS	Input
C5	VSS	Power/Other	
C6	LINT0	CMOS	Input
C7	THERMTRIP#	Open Drain	Output
C8	VSS	Power/Other	
C9	VCC	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VCC	Power/Other	
C14	VSS	Power/Other	
C15	VCC	Power/Other	
C16	VSS	Power/Other	
C17	VCC	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
C20	DBR#	CMOS	Output
C21	BSEL[2]	CMOS	Output
C22	VSS	Power/Other	
C23	RSVD	Reserved	
C24	RSVD	Reserved	
C25	VSS	Power/Other	
C26	TEST1	Test	
D1	VSS	Power/Other	
D2	RSVD	Reserved	
D3	RSVD	Reserved	
D4	VSS	Power/Other	
D5	STPCLK#	CMOS	Input
D6	PWRGOOD	CMOS	Input
D7	SLP#	CMOS	Input
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VCC	Power/Other	
D11	VSS	Power/Other	
D12	VCC	Power/Other	
D13	VSS	Power/Other	
D14	VCC	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VCC	Power/Other	
D19	VSS	Power/Other	
D20	IERR#	Open Drain	Output
D21	PROCHOT #	Open Drain	Input/ Output
D22	RSVD	Reserved	
D23	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
D24	DPWR#	Common Clock	Input
D25	TEST2	Test	
D26	VSS	Power/Other	
E1	DBSY#	Common Clock	Input/ Output
E2	BNR#	Common Clock	Input/ Output
E3	VSS	Power/Other	
E4	HITM#	Common Clock	Input/ Output
E5	DPRSTP#	CMOS	Input
E6	VSS	Power/Other	
E7	VCC	Power/Other	
E8	VSS	Power/Other	
E9	VCC	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VCC	Power/Other	
E14	VSS	Power/Other	
E15	VCC	Power/Other	
E16	VSS	Power/Other	
E17	VCC	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	VSS	Power/Other	
E22	D[0]#	Source Synch	Input/ Output
E23	D[7]#	Source Synch	Input/ Output
E24	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
E25	D[6]#	Source Synch	Input/ Output
E26	D[2]#	Source Synch	Input/ Output
F1	BR0#	Common Clock	Input/ Output
F2	VSS	Power/Other	
F3	RS[0]#	Common Clock	Input
F4	RS[1]#	Common Clock	Input
F5	VSS	Power/Other	
F6	RSVD	Reserved	
F7	VCC	Power/Other	
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VCC	Power/Other	
F11	VSS	Power/Other	
F12	VCC	Power/Other	
F13	VSS	Power/Other	
F14	VCC	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VCC	Power/Other	
F19	VSS	Power/Other	
F20	VCC	Power/Other	
F21	DRDY#	Common Clock	Input/ Output
F22	VSS	Power/Other	
F23	D[4]#	Source Synch	Input/ Output
F24	D[1]#	Source Synch	Input/ Output

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
F25	VSS	Power/Other	
F26	D[13]#	Source Synch	Input/ Output
G1	VSS	Power/Other	
G2	TRDY#	Common Clock	Input
G3	RS[2]#	Common Clock	Input
G4	VSS	Power/Other	
G5	BPRI#	Common Clock	Input
G6	HIT#	Common Clock	Input/ Output
G21	VCCP	Power/Other	
G22	DSTBP[0]#	Source Synch	Input/ Output
G23	VSS	Power/Other	
G24	D[9]#	Source Synch	Input/ Output
G25	D[5]#	Source Synch	Input/ Output
G26	VSS	Power/Other	
H1	ADS#	Common Clock	Input/ Output
H2	REQ[1]#	Source Synch	Input/ Output
H3	VSS	Power/Other	
H4	LOCK#	Common Clock	Input/ Output
H5	DEFER#	Common Clock	Input
H6	VSS	Power/Other	
H21	VSS	Power/Other	
H22	D[3]#	Source Synch	Input/ Output
H23	DSTBN[0]#	Source Synch	Input/ Output

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
H24	VSS	Power/Other	
H25	D[15]#	Source Synch	Input/ Output
H26	D[12]#	Source Synch	Input/ Output
J1	A[9]#	Source Synch	Input/ Output
J2	VSS	Power/Other	
J3	REQ[3]#	Source Synch	Input/ Output
J4	A[3]#	Source Synch	Input/ Output
J5	VSS	Power/Other	
J6	VCCP	Power/Other	
J21	VCCP	Power/Other	
J22	VSS	Power/Other	
J23	D[11]#	Source Synch	Input/ Output
J24	D[10]#	Source Synch	Input/ Output
J25	VSS	Power/Other	
J26	DINV[0]#	Source Synch	Input/ Output
K1	VSS	Power/Other	
K2	REQ[2]#	Source Synch	Input/ Output
K3	REQ[0]#	Source Synch	Input/ Output
K4	VSS	Power/Other	
K5	A[6]#	Source Synch	Input/ Output
K6	VCCP	Power/Other	
K21	VCCP	Power/Other	
K22	D[14]#	Source Synch	Input/ Output
K23	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
K24	D[8]#	Source Synch	Input/ Output
K25	D[17]#	Source Synch	Input/ Output
K26	VSS	Power/Other	
L1	A[13]#	Source Synch	Input/ Output
L2	ADSTB[0]#	Source Synch	Input/ Output
L3	VSS	Power/Other	
L4	A[4]#	Source Synch	Input/ Output
L5	REQ[4]#	Source Synch	Input/ Output
L6	VSS	Power/Other	
L21	VSS	Power/Other	
L22	D[21]#	Source Synch	Input/ Output
L23	D[22]#	Source Synch	Input/ Output
L24	VSS	Power/Other	
L25	D[20]#	Source Synch	Input/ Output
L26	D[29]#	Source Synch	Input/ Output
M1	A[7]#	Source Synch	Input/ Output
M2	VSS	Power/Other	
M3	A[5]#	Source Synch	Input/ Output
M4	RSVD	Reserved	
M5	VSS	Power/Other	
M6	VCCP	Power/Other	
M21	VCCP	Power/Other	
M22	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
M23	D[23]#	Source Synch	Input/ Output
M24	DSTBN[1] #	Source Synch	Input/ Output
M25	VSS	Power/Other	
M26	DINV[1]#	Source Synch	Input/ Output
N1	VSS	Power/Other	
N2	A[8]#	Source Synch	Input/ Output
N3	A[10]#	Source Synch	Input/ Output
N4	VSS	Power/Other	
N5	RSVD	Reserved	
N6	VCCP	Power/Other	
N21	VCCP	Power/Other	
N22	D[16]#	Source Synch	Input/ Output
N23	VSS	Power/Other	
N24	D[31]#	Source Synch	Input/ Output
N25	DSTBP[1] #	Source Synch	Input/ Output
N26	VSS	Power/Other	
P1	A[15]#	Source Synch	Input/ Output
P2	A[12]#	Source Synch	Input/ Output
P3	VSS	Power/Other	
P4	A[14]#	Source Synch	Input/ Output
P5	A[11]#	Source Synch	Input/ Output
P6	VSS	Power/Other	
P21	VSS	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
P22	D[25]#	Source Synch	Input/ Output
P23	D[26]#	Source Synch	Input/ Output
P24	VSS	Power/Other	
P25	D[24]#	Source Synch	Input/ Output
P26	D[18]#	Source Synch	Input/ Output
R1	A[16]#	Source Synch	Input/ Output
R2	VSS	Power/Other	
R3	A[19]#	Source Synch	Input/ Output
R4	A[24]#	Source Synch	Input/ Output
R5	VSS	Power/Other	
R6	VCCP	Power/Other	
R21	VCCP	Power/Other	
R22	VSS	Power/Other	
R23	D[19]#	Source Synch	Input/ Output
R24	D[28]#	Source Synch	Input/ Output
R25	VSS	Power/Other	
R26	COMP[0]	Power/Other	Input/ Output
T1	VSS	Power/Other	
T2	RSVD	Reserved	
T3	A[26]#	Source Synch	Input/ Output
T4	VSS	Power/Other	
T5	A[25]#	Source Synch	Input/ Output
T6	VCCP	Power/Other	
T21	VCCP	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
T22	RSVD	Reserved	
T23	VSS	Power/Other	
T24	D[27]#	Source Synch	Input/ Output
T25	D[30]#	Source Synch	Input/ Output
T26	VSS	Power/Other	
U1	COMP[2]	Power/Other	Input/ Output
U2	A[23]#	Source Synch	Input/ Output
U3	VSS	Power/Other	
U4	A[21]#	Source Synch	Input/ Output
U5	A[18]#	Source Synch	Input/ Output
U6	VSS	Power/Other	
U21	VSS	Power/Other	
U22	D[39]#	Source Synch	Input/ Output
U23	D[37]#	Source Synch	Input/ Output
U24	VSS	Power/Other	
U25	D[38]#	Source Synch	Input/ Output
U26	COMP[1]	Power/Other	Input/ Output
V1	COMP[3]	Power/Other	Input/ Output
V2	VSS	Power/Other	
V3	RSVD	Reserved	
V4	ADSTB[1]#	Source Synch	Input/ Output
V5	VSS	Power/Other	
V6	VCCP	Power/Other	
V21	VCCP	Power/Other	

Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
V22	VSS	Power/Other	
V23	DINV[2]#	Source Synch	Input/ Output
V24	D[34]#	Source Synch	Input/ Output
V25	VSS	Power/Other	
V26	D[35]#	Source Synch	Input/ Output
W1	VSS	Power/Other	
W2	A[30]#	Source Synch	Input/ Output
W3	A[27]#	Source Synch	Input/ Output
W4	VSS	Power/Other	
W5	A[28]#	Source Synch	Input/ Output
W6	A[20]#	Source Synch	Input/ Output
W21	VCCP	Power/Other	
W22	D[41]#	Source Synch	Input/ Output
W23	VSS	Power/Other	
W24	DSTBN[2]#	Source Synch	Input/ Output
W25	D[36]#	Source Synch	Input/ Output
W26	VSS	Power/Other	
Y1	A[31]#	Source Synch	Input/ Output
Y2	A[17]#	Source Synch	Input/ Output
Y3	VSS	Power/Other	
Y4	A[29]#	Source Synch	Input/ Output
Y5	A[22]#	Source Synch	Input/ Output
Y6	VSS	Power/Other	

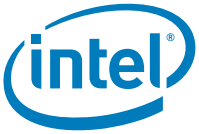


Table 19. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
Y21	VSS	Power/Other	
Y22	D[45]#	Source Synch	Input/ Output
Y23	D[42]#	Source Synch	Input/ Output
Y24	VSS	Power/Other	
Y25	DSTBP[2] #	Source Synch	Input/ Output
Y26	D[44]#	Source Synch	Input/ Output

5 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1. Any attempt to operate that processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsinks or heat exchangers attached to the processor exposed die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a processor fan ducted to a heat exchanger that is thermally coupled to the processor via a heat pipe or direct die attachment. A secondary fan or air from the processor fan may also be used to cool other platform components or to lower the internal ambient temperature within the system.

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 20 to Table 22. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The maximum junction temperature is defined by an activation of the processor Intel Thermal Monitor. Refer to Section 5.1.3 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 20 to Table 22. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.1.3. In all cases, the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 20. Power Specifications for the Intel Core Duo Processor SV (Standard Voltage)

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power	Unit	Notes
TDP	T2700 T2600 T2500 T2400 T2300 T2300E N/A	2.33 GHz & HFM V_{CC} 2.16 GHz & HFM V_{CC} 2.00 GHz & HFM V_{CC} 1.83 GHz & HFM V_{CC} 1.66 GHz & HFM V_{CC} 1.66 GHz & HFM V_{CC} 1.00 GHz & LFM V_{CC}	31 31 31 31 31 31 13.1	W	At 100°C Notes 1, 4, 5

Symbol	Parameter	Min	Typ	Max	Unit	Notes
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}			 15.8 4.8	W	At 50°C Note 2
P_{SLP}	Sleep Power at HFM V_{CC} at LFM V_{CC}			 15.5 4.7	W	At 50°C Note 2
P_{DSLP}	Deep Sleep Power at HFM V_{CC} at LFM V_{CC}			 10.5 3.4	W	At 35°C Note 2
P_{DPRSLP}	Deeper Sleep Power			2.2	W	At 35°C Note 2
P_{DC4}	Intel® Enhanced Deeper Sleep Power			1.8	W	At 35°C Note 2
T_J	Junction Temperature	0		100	°C	Notes 3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specification.
5. T2300E does not support Intel Virtualization Technology.

Table 21. Power Specifications for the Intel Core Solo Processor SV (Standard Voltage)

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	T1400 T1300 N/A	1.83 GHz & HFM V_{CC} 1.66 GHz & HFM V_{CC} 1.00 GHz & LFM V_{CC}	27 27 13.1			W	At 100°C Notes 1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}				15.8 4.8	W	At 50°C Note 2
P_{SLP}	Sleep Power at HFM V_{CC} at LFM V_{CC}				15.5 4.7	W	At 50°C Note 2
P_{DSLP}	Deep Sleep Power at HFM V_{CC} at LFM V_{CC}				10.5 3.4	W	At 35°C Note 2
P_{DPRSLP}	Deeper Sleep Power				2.2	W	At 35°C Note 2
P_{DC4}	Intel® Enhanced Deeper Sleep Power				1.8	W	At 35°C Note 2
T_J	Junction Temperature		0		100	°C	Notes 3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specification.

Table 22. Power Specifications for the Intel Core Duo Processor LV (Low Voltage)

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	L2500 L2400 L2300 N/A	1.83 GHz & HFM V_{CC} 1.66 GHz & HFM V_{CC} 1.50 GHz & HFM V_{CC} 1.00 GHz & LFM V_{CC}	15 15 15 13.1			W	At 100°C Notes 1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}				6.0 4.8	W	At 50°C Note 2
P_{SLP}	Sleep Power at HFM V_{CC} at LFM V_{CC}				5.8 4.7	W	At 50°C Note 2
P_{DSLP}	Deep Sleep Power at HFM V_{CC} at LFM V_{CC}				5.7 3.4	W	At 35°C Note 2
P_{DPRSLP}	Deeper Sleep Power				2.2	W	At 35°C Note 2
P_{DC4}	Intel® Enhanced Deeper Sleep Power				1.8	W	At 35°C Note 2
T_J	Junction Temperature		0		100	°C	Notes 3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specification.

Table 23. Power Specifications for the Intel Core Duo Processor, Ultra Low Voltage (ULV)

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	U2500 U2400 N/A	1.20 GHz & HFM V_{CC} 1.06 GHz & HFM V_{CC} 800 MHz & LFM V_{CC}		9 9 7.5		W	At 100°C Notes1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}				3.7 2.6	W	At 50°C Note 2
P_{SLP}	Sleep Power at HFM V_{CC} at LFM V_{CC}				3.6 2.5	W	At 50°C Note 2
P_{DSLP}	Deep Sleep Power at HFM V_{CC} at LFM V_{CC}				2.2 1.8	W	At 35°C Note 2
P_{DPRSLP}	Deeper Sleep Power				1.3	W	At 35°C Note 2
P_{DC4}	Intel® Enhanced Deeper Sleep Power				1.1	W	At 35°C Note 2
T_J	Junction Temperature		0		100	°C	Notes 3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specification.

Table 24. Power Specifications for the Intel Core Solo Processor ULV (Ultra Low Voltage)

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	U1500 U1400 U1300	1.33 GHz and HFM V_{CC} 1.20 GHz and HFM V_{CC}1.06 GHz and LFM V_{CC} 800 MHz and LFM V_{CC}	5.5 5.5 5.5 5			W	At 100°C Notes 1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}				3.0 2.2	W	At 50°C Note 2
P_{SLP}	Sleep Power at HFM V_{CC} at LFM V_{CC}				2.9 2.1	W	At 50°C Note 2
P_{DSLP}	Deep Sleep Power at HFM V_{CC} at LFM V_{CC}				1.5 1.2	W	At 35°C Note 2
P_{DPRSLP}	Deeper Sleep Power				0.7	W	At 35°C Note 2
P_{DC4}	Intel® Enhanced Deeper Sleep Power				0.6	W	At 35°C Note 2
T_J	Junction Temperature		0		100	°C	Notes 3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specification.

5.1 Thermal Specifications

The processor incorporates three methods of monitoring die temperature, the digital thermal sensor (DTS), Intel Thermal Monitor and the thermal diode. The Intel Thermal Monitor (detailed in Section 5.1.3) must be used to determine when the maximum specified processor junction temperature has been reached.

5.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal diode, with its collector shorted to Ground. The thermal diode, can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard, or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor Model Specific Register (MSR) and applied. See Section 5.1.2 for more details. Please see Section 5.1.3 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

Note: The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals, will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode-based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the processor Model Specific Register (MSR).

Table 25, Table 26, Table 27, and Table 28 provide the diode interface and specifications. Two different sets of diode parameters are listed in Table 26 and Table 27. The Diode Model parameters (Table 26) apply to traditional thermal sensors that use the Diode Equation to determine the processor temperature. Transistor Model parameters (Table 27) have been added to support thermal sensors that use the transistor equation method. The Transistor Model may provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Please contact your external thermal sensor supplier for their recommendation. This thermal diode is separate from the Intel Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Intel Thermal Monitor.

Table 25. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	A24	Thermal diode anode
THERMDC	A25	Thermal diode cathode

Table 26. Thermal Diode Parameters using Diode Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	-	200	µA	1
n	Diode Ideality Factor	1.000	1.009	1.050	-	2, 3, 4
R_T	Series Resistance	2.79	4.52	6.24	Ω	2, 3, 5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. Characterized across a temperature range of 50 - 100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

   $$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the junction temperature. R_T, as defined, includes the lands of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

   $$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$

   where T_{error} = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

Table 27. Thermal Diode Parameters using Transistor Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	-	200	µA	1, 2
I_E	Emitter Current	5		200	µA	
n_Q	Transistor Ideality	0.997	1.001	1.005	-	3, 4, 5
Beta		0.3		0.760		3, 4
R_T	Series Resistance	2.79	4.52	6.24	Ω	3, 6

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Same as I_{FW} in Table 25.
3. Characterized across a temperature range of 50 - 100°C.
4. Not 100% tested. Specified by design characterization.
5. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

   $$I_C = I_S * (e^{qV_{BE}/n_Q kT} - 1)$$

   Where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
6. The series resistance, R_T, provided in the Diode Model Table (Table 26) can be used for more accurate readings as needed.

When calculating a temperature based on thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although some are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 25. In most temperature sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode the ideality value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processors diode ideality deviates from that of n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} X (1 - n_{actual}/n_{trim})$$

Where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

5.1.2 Thermal Diode Offset

In order to improve the accuracy of diode based temperature measurements, a temperature offset value (specified as Toffset) will be programmed into a processor Model Specific Register (MSR) which will contain thermal diode characterization data. During manufacturing each processors thermal diode will be evaluated for its behavior relative to a theoretical diode. Using the equation above, the temperature error created by the difference between n_{trim} and the actual ideality of the particular processor will be calculated.

If the n_{trim} value used to calculate Toffset differs from the n_{trim} value used in a temperature sensing device, the $T_{error(nf)}$ may not be accurate. If desired, the Toffset can be adjusted by calculating n_{actual} and then recalculating the offset using the actual n_{trim} as defined in the temperature sensor manufacturers' datasheet.

The n_{trim} used to calculate the Diode Correction Toffset are listed in the table below

Table 28. Thermal Diode n_{trim} and Diode Correction Toffset

Symbol	Parameter	Value
n_{trim}	Diode ideality used to calculate Toffset	1.01

5.1.3 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: Automatic mode and on-demand mode. If both modes are activated, Automatic mode takes precedence.

Note: The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications.

There are two automatic modes called Intel Thermal Monitor 1 (TM1) and Intel Thermal Monitor 2 (TM2). These modes are selected by writing values to the Model Specific Registers (MSRs) of the processor. After Automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

Likewise, when Intel Thermal Monitor 2 is enabled, and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep Technology transition to a lower operating point. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep Technology transition to the last requested operating point.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled in the auto-throttle MSR, TM2 will take precedence over TM1. However, if TM2 is not sufficient to cool the processor below the maximum operating temperature then TM1 will also activate to help cool down the processor. Intel recommends Intel Thermal Monitor 1 and Intel Thermal Monitor 2 be enabled on the Intel Core Duo processor and Intel Core Solo processor.

If a processor load-based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when an Intel Thermal Monitor 2 period is active, there are two possible results:

1. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **higher** than the Intel Thermal Monitor 2 transition-based target frequency, the processor load-based transition will be deferred until the Intel Thermal Monitor 2 event has been completed.
2. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **lower** than the Intel Thermal Monitor 2 transition-based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep Technology target frequency point.

When Intel Thermal Monitor 1 is enabled while a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately, independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however,

if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

Note: PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low power states (internal clocks stopped), hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

5.1.4 Digital Thermal Sensor (DTS)

The processor also contains an on-die DTS that can be read via a MSR (no I/O interface). In a dual core implementation of the Intel Core Duo processor, each core will have a unique DTS whose temperature is accessible via processor MSR. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Intel Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (C0 state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below $T_{J,max}$. Over temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the digital thermal sensor MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not guaranteed once the activation of the Out of Spec status bit is set.

The DTS relative temperature readout corresponds to the Intel Thermal Monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached the TM1 or TM2 hardware thermal control mechanism will activate. The DTS and TM1/TM2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical

and thermal attach and software application. The system designer is required to use the DTS to guarantee proper operation of the processor within its temperature operating specifications

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC.

5.1.5 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

5.1.6 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Intel Thermal Monitor 1 or Intel Thermal Monitor 2 is enabled (note that the Intel Thermal Monitor 1 or Intel Thermal Monitor 2 must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

In a dual core implementation, only a single PROCHOT# pin exists at a package level. When either core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clocks modulated. If TM2 is enabled, then regardless of which core(s) are above TCC temperature trip point, both cores will enter the lowest programmed TM2 performance state.

Note: It is important to note that Intel recommends both TM1 and TM2 be enabled.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on both cores, then both processor cores will have their core clocks modulated. If TM2 is enabled on both cores, then both processor core will enter the lowest programmed TM2 performance state.

One application is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very

short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

§

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Intel:

LE80539LF0282MXS L9JT LF80539GF0412MXS L9EH LE80539UE0092MXS L9JQ