

## Wide-Input Sensorless CC/CV Step-Down DC/DC Converter

### FEATURES

- 40V Input Voltage Surge
- 38V Steady State Operation
- Up to 3A output current
- Output Voltage up to 12V
- Patent Pending Active CC Sensorless Constant Current Control
  - Integrated Current Control Improves Efficiency, Lowers Cost, and Reduces Component Count
- Resistor Programmable
  - Current Limit from 1.5A to 3A
  - Patented Cable Compensation from 0Ω to 0.3Ω
- ±7.5% CC Accuracy
  - Compensation of Input /Output Voltage Change
  - Temperature Compensation
  - Independent of inductance and Inductor DCR
- 2% Feedback Voltage Accuracy
- Up to 94% Efficiency
- 225kHz Switching Frequency Eases EMI Design
- Advanced Feature Set
  - Integrated Soft Start
  - Thermal Shutdown
  - Secondary Cycle-by-Cycle Current Limit
  - Protection Against Shorted ISET Pin
- SOP-8EP Package

### APPLICATIONS

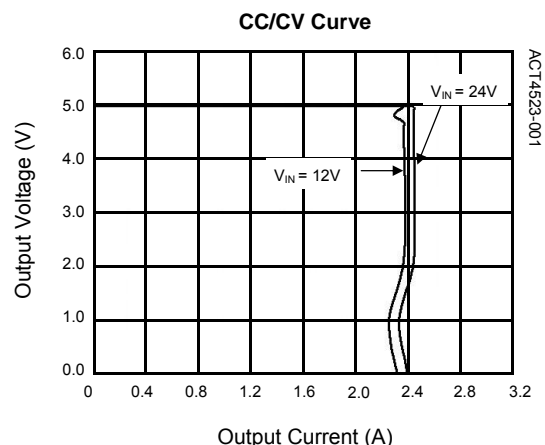
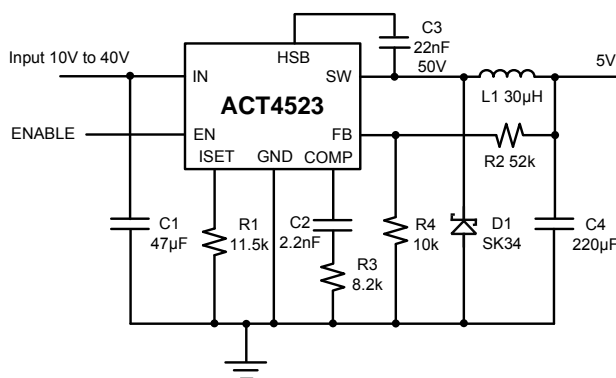
- Car Charger/ Adaptor
- Rechargeable Portable Devices
- General-Purpose CC/CV Supply

### GENERAL DESCRIPTION

ACT4523 is a wide input voltage, high efficiency Active CC step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. ACT4523 provides up to 3A output current at 225kHz switching frequency.

Active CC is a patent-pending control scheme to achieve highest accuracy sensorless constant current control. Active CC eliminates the expensive, high accuracy current sense resistor, making it ideal for battery charging applications and adaptors with accurate current limit. The ACT4523 achieves higher efficiency than traditional constant current switching regulators by eliminating its associated power loss.

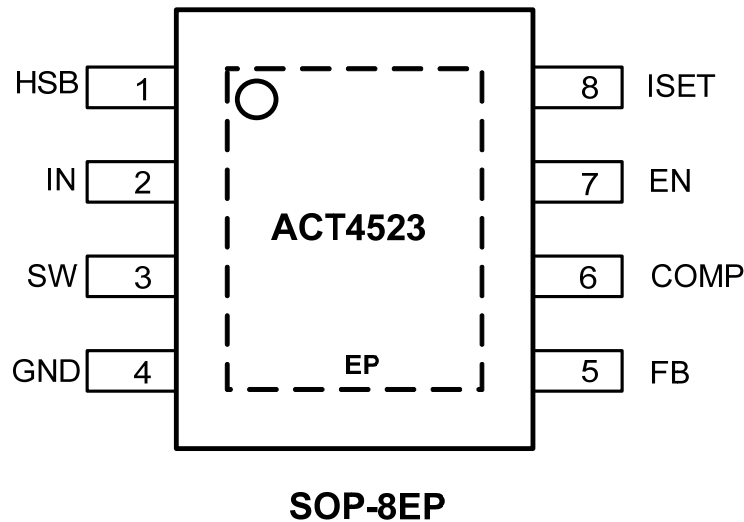
Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit. The devices are available in a SOP-8EP package and require very few external devices for operation.



## ORDERING INFORMATION

| PART NUMBER | OPERATION TEMPERATURE RANGE | PACKAGE | PINS | PACKING     |
|-------------|-----------------------------|---------|------|-------------|
| ACT4523YH-T | -40°C to 85°C               | SOP-8EP | 8    | TAPE & REEL |

## PIN CONFIGURATION



## PIN DESCRIPTIONS

| PIN | NAME        | DESCRIPTION  |
|-----|-------------|--|
| 1   | HSB         | High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.   |
| 2   | IN          | Power Supply Input. Bypass this pin with a 10µF ceramic capacitor to GND, placed as close to the IC as possible.   |
| 3   | SW          | Power Switching Output to External Inductor.   |
| 4   | GND         | Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.   |
| 5   | FB          | Feedback Input. The voltage at this pin is regulated to 0.808V. Connect to the resistor divider between output and GND to set the output voltage.  |
| 6   | COMP        | Error Amplifier Output. This pin is used to compensate the converter.  |
| 7   | EN          | Enable Input. EN is pulled up to 5V with a 4µA current, and contains a precise 1.6V logic threshold. Drive this pin to a logic-high or leave unconnected to enable the IC. Drive to a logic-low to disable the IC and enter shutdown mode. |
| 8   | ISET        | Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.   |
|     | Exposed Pad | Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.   |

## ABSOLUTE MAXIMUM RATINGS<sup>①</sup>

| PARAMETER                              | VALUE                          | UNIT |
|--|--------------------------------|------|
| IN to GND                              | -0.3 to 40                     | V    |
| SW to GND                              | -1 to $V_{IN} + 1$             | V    |
| HSB to GND                             | $V_{SW} - 0.3$ to $V_{SW} + 7$ | V    |
| FB, EN, ISET, COMP to GND              | -0.3 to + 6                    | V    |
| Junction to Ambient Thermal Resistance | 46                             | °C/W |
| Operating Junction Temperature         | -40 to 150                     | °C   |
| Storage Junction Temperature           | -55 to 150                     | °C   |
| Lead Temperature (Soldering 10 sec.)   | 300                            | °C   |

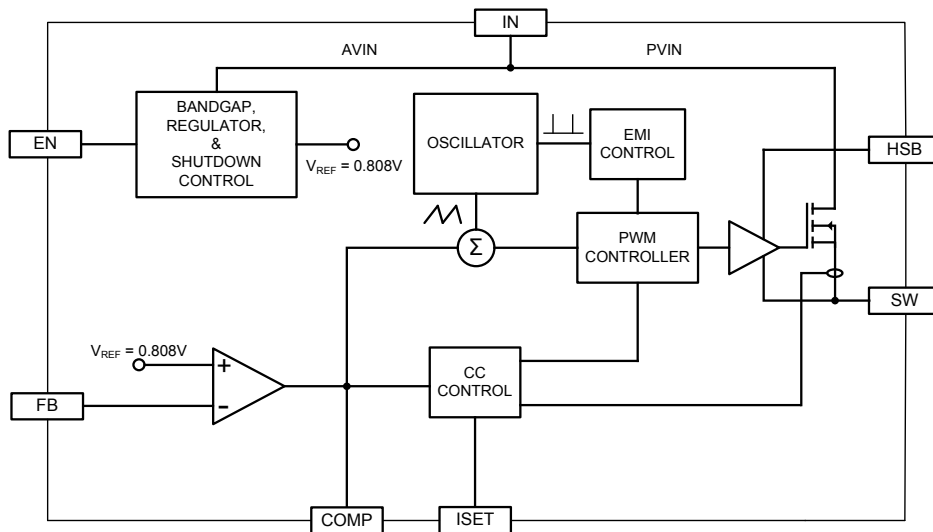
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 20V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| PARAMETER                               | TEST CONDITIONS  | MIN  | TYP   | MAX  | UNIT       |
|---|--|------|-------|------|------------|
| Input Voltage                           |  | 10   |       | 38   | V          |
| Input Voltage Surge                     |  |      |       | 40   | V          |
| $V_{IN}$ UVLO Turn-On Voltage           | Input Voltage Rising   | 9.0  | 9.4   | 9.7  | V          |
| $V_{IN}$ UVLO Hysteresis                | Input Voltage Falling  |      | 1.1   |      | V          |
| Standby Supply Current                  | $V_{EN} = 3V$ , $V_{FB} = 1V$                                    |      | 0.9   | 1.4  | mA         |
|   | $V_{EN} = 3V$ , $V_{OUT} = 5V$ , No load                         |      | 3.0   |      | mA         |
| Shutdown Supply Current                 | $V_{EN} = 0V$  |      | 75    | 115  | $\mu A$    |
| Feedback Voltage                        |  | 792  | 808   | 824  | mV         |
| Internal Soft-Start Time                |  |      | 400   |      | $\mu s$    |
| Error Amplifier Transconductance        | $V_{FB} = V_{COMP} = 0.8V$ ,<br>$\Delta I_{COMP} = \pm 10\mu A$  |      | 650   |      | $\mu A/V$  |
| Error Amplifier DC Gain                 |  |      | 4000  |      | V/V        |
| Switching Frequency                     | $V_{FB} = 0.808V$  | 200  | 225   | 250  | kHz        |
| Foldback Switching Frequency            | $V_{FB} = 0V$  |      | 30    |      | kHz        |
| Maximum Duty Cycle                      |  | 85   | 88    | 91   | %          |
| Minimum On-Time                         |  |      | 200   |      | ns         |
| COMP to Current Limit Transconductance  | $V_{COMP} = 1.2V$  |      | 5.25  |      | A/V        |
| Secondary Cycle-by-Cycle Current Limit  | Duty Cycle = 0%  |      | 4.5   |      | A          |
| Slope Compensation                      | Duty = $D_{MAX}$   |      | 1.2   |      | A          |
| ISET Voltage                            |  |      | 1     |      | V          |
| ISET to IOUT DC Room Temp Current Gain  | $I_{OUT} / I_{SET}$ , $R_{ISET} = 19.6k\Omega$                   |      | 25000 |      | A/A        |
| CC Controller DC Accuracy               | $R_{ISET} = 19.6k\Omega$ , $V_{OUT} = 3.5V$<br>Open-Loop DC Test | 1175 | 1190  | 1205 | mA         |
| EN Threshold Voltage                    | EN Pin Rising  | 1.47 | 1.6   | 1.73 | V          |
| EN Hysteresis                           | EN Pin Falling   |      | 125   |      | mV         |
| EN Internal Pull-up Current             |  |      | 4     |      | $\mu A$    |
| High-Side Switch ON-Resistance          |  |      | 0.16  |      | $\Omega$   |
| SW Off Leakage Current                  | $V_{EN} = V_{SW} = 0V$   |      | 1     | 10   | $\mu A$    |
| Thermal Shutdown Temperature            | Temperature Rising   |      | 150   |      | $^\circ C$ |
| Thermal Shutdown Temperature Hysteresis | Temperature Falling  |      | 20    |      | $^\circ C$ |

## FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### CV/CC Loop Regulation

As seen in *Functional Block Diagram*, the ACT4523 is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to  $V_{SW} + 5V$  when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from

regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 225kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 30kHz at  $V_{FB} = 0.15V$ .

### Enable Pin

The ACT4523 has an enable input EN for turning the IC on or off. The EN pin contains a precision 1.6V comparator with 125mV hysteresis and a 4 $\mu$ A pull-up current source. The comparator can be used with a resistor divider from  $V_{IN}$  to program a startup voltage higher than the normal UVLO value. It can be used with a resistor divider from  $V_{OUT}$  to disable charging of a deeply discharged battery, or it can be used with a resistor divider containing a thermistor to provide a temperature-dependent shutoff protection for over temperature battery. The thermistor should be thermally coupled to the battery pack for this usage.

If left floating, the EN pin will be pulled up to roughly 5V by the internal 4 $\mu$ A current source. It can be driven from standard logic signals greater than 1.6V, or driven with open-drain logic to provide digital on/off control.

### Thermal Shutdown

The ACT4523 disables switching when its junction temperature exceeds 150°C and resumes when the temperature has dropped by 20°C.

## APPLICATIONS INFORMATION

### Output Voltage Setting

Figure 1:

#### Output Voltage Setting

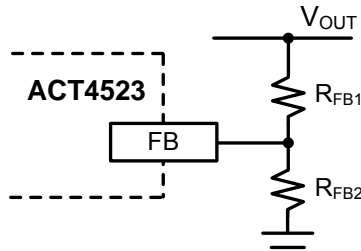


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors  $R_{FB1}$  and  $R_{FB2}$  based on the output voltage. Typically, use  $R_{FB2} \approx 10k\Omega$  and determine  $R_{FB1}$  from the following equation:

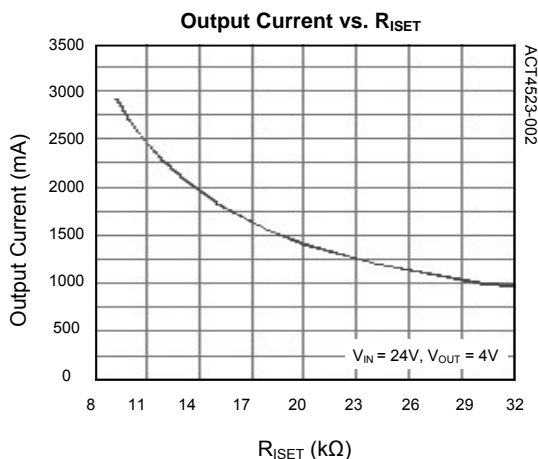
$$R_{FB1} = R_{FB2} \left( \frac{V_{OUT}}{0.808V} - 1 \right) \quad (1)$$

### CC Current Setting

ACT4523 constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 25000 (25mA/1μA). To determine the proper resistor for a desired current, please refer to Figure 2 below.

Figure 2:

#### Curve for Programming Output CC Current

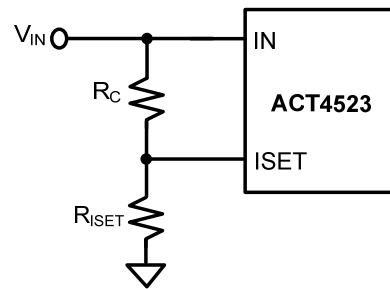


### CC Current Line Compensation

When operating at constant current mode, the current limit increase slightly with input voltage. For wide input voltage applications, a resistor  $R_C$  is added to compensate line change and keep output high CC accuracy, as shown in Figure 3.

Figure 3:

#### Output Line Compensation



### Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value  $L$  based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOADMAX} K_{RIPPLE}} \quad (2)$$

where  $V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage,  $f_{SW}$  is the switching frequency,  $I_{LOADMAX}$  is the maximum load current, and  $K_{RIPPLE}$  is the ripple factor. Typically, choose  $K_{RIPPLE} = 30\%$  to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (4)$$

## APPLICATIONS INFORMATION CONT'D

The selected inductor should not saturate at  $I_{LPK}$ . The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (5)$$

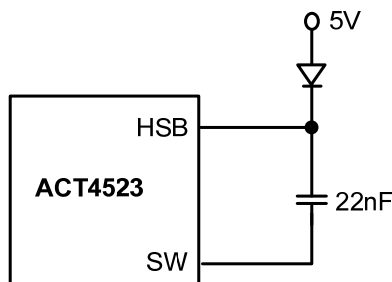
$I_{LIM}$  is the internal current limit, which is typically 3.2A, as shown in Electrical Characteristics Table.

### External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.

Figure 4:

External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

### Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10 $\mu$ F. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1 $\mu$ F ceramic capacitor is placed right next to the IC.

### Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \times f_{SW}^2 L C_{OUT}} \quad (6)$$

Where  $I_{OUTMAX}$  is the maximum output current,  $K_{RIPPLE}$  is the ripple factor,  $R_{ESR}$  is the ESR of the output capacitor,  $f_{SW}$  is the switching frequency, L is the inductor value, and  $C_{OUT}$  is the output capacitance. In the case of ceramic output capacitors,  $R_{ESR}$  is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by  $R_{ESR}$  multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

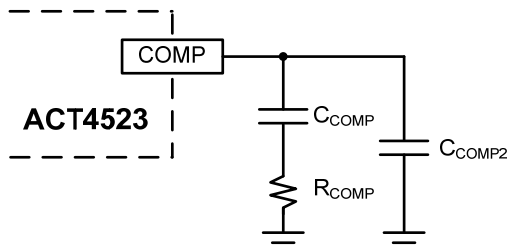
For ceramic output capacitor, typically choose a capacitance of about 22 $\mu$ F. For tantalum or electrolytic capacitors, choose a capacitor with less than 50m $\Omega$  ESR.

### Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

## STABILITY COMPENSATION

**Figure 5:**  
**Stability Compensation**



①: C<sub>COMP2</sub> is needed only for high ESR output capacitor

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 5. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808 V}{I_{OUT}} A_{VEA} G_{COMP} \quad (7)$$

The dominant pole P1 is due to C<sub>COMP</sub>:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (8)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (9)$$

The first zero Z1 is due to R<sub>COMP</sub> and C<sub>COMP</sub>:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (10)$$

And finally, the third pole is due to R<sub>COMP</sub> and C<sub>COMP2</sub> (if C<sub>COMP2</sub> is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (11)$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R<sub>COMP</sub>:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.808 V} = 5.12 \times 10^7 V_{OUT} C_{OUT} \quad (\Omega) \quad (12)$$

STEP 2. Set the zero f<sub>Z1</sub> at 1/4 of the cross over frequency. If R<sub>COMP</sub> is less than 15kΩ, the equation for C<sub>COMP</sub> is:

$$C_{COMP} = \frac{2.83 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (13)$$

If R<sub>COMP</sub> is limited to 15kΩ, then the actual cross over frequency is 6.58 / (V<sub>OUT</sub>C<sub>OUT</sub>). Therefore:

$$C_{COMP} = 6.45 \times 10^{-6} V_{OUT} C_{OUT} \quad (F) \quad (14)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C<sub>COMP2</sub> is required. The condition for using C<sub>COMP2</sub> is:

$$R_{ESRCOUT} \geq (\text{Min } \frac{1.77 \times 10^{-6}}{C_{OUT}}, 0.006 \times V_{OUT}) \quad (\Omega) \quad (15)$$

And the proper value for C<sub>COMP2</sub> is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \quad (16)$$

Though C<sub>COMP2</sub> is unnecessary when the output capacitor has sufficiently low ESR, a small value C<sub>COMP2</sub> such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

**Table 1:**  
**Typical Compensation for Different Output Voltages and Output Capacitors**

| V <sub>OUT</sub> | C <sub>OUT</sub> | R <sub>COMP</sub> | C <sub>COMP</sub> | C <sub>COMP2</sub> ① |
|------------------|------------------|-------------------|-------------------|----------------------|
| 2.5V             | 47μF Ceramic CAP | 5.6kΩ             | 3.3nF             | None                 |
| 3.3V             | 47μF Ceramic CAP | 6.2kΩ             | 3.3nF             | None                 |
| 5V               | 47μF Ceramic CAP | 8.2kΩ             | 3.3nF             | None                 |
| 2.5V             | 470μF/6.3V/30mΩ  | 39kΩ              | 22nF              | 47pF                 |
| 3.3V             | 470μF/6.3V/30mΩ  | 45kΩ              | 22nF              | 47pF                 |
| 5V               | 470μF/6.3V/30mΩ  | 51kΩ              | 22nF              | 47pF                 |

①: C<sub>COMP2</sub> is needed for high ESR output capacitor.  
C<sub>COMP2</sub> ≤ 47pF is recommended.

### CC Loop Stability

The constant-current control loop is internally compensated over the 1500mA-3000mA output range. No additional external compensation is required to stabilize the CC current.

### Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the ACT4523 integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in Figure 6 to choose the proper feedback resistance values for cable compensation.

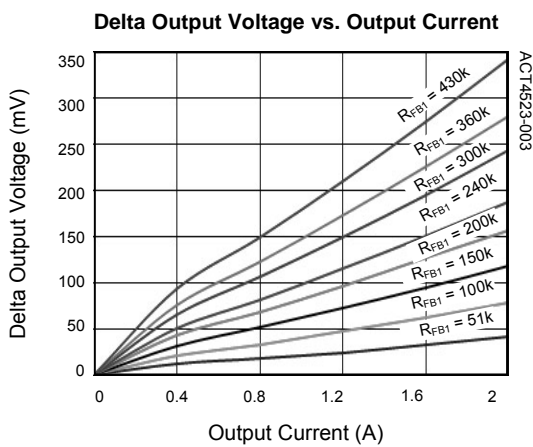


## STABILITY COMPENSATION CONT'D

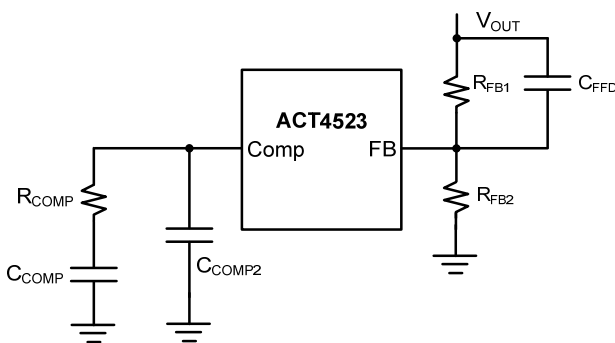
$R_{FB1}$  is the high side resistor of voltage divider.

In the case of high  $R_{FB1}$  used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 7, adding a capacitor in paralalled with  $R_{FB1}$  or increasing the compensation capacitance at COMP pin helps the system stability.

**Figure 6:**  
**Cable Compensation at Various Resistor Divider Values**



**Figure 7:**  
**Frequency Compensation for High  $R_{FB1}$**



## PC Board Layout Guidance

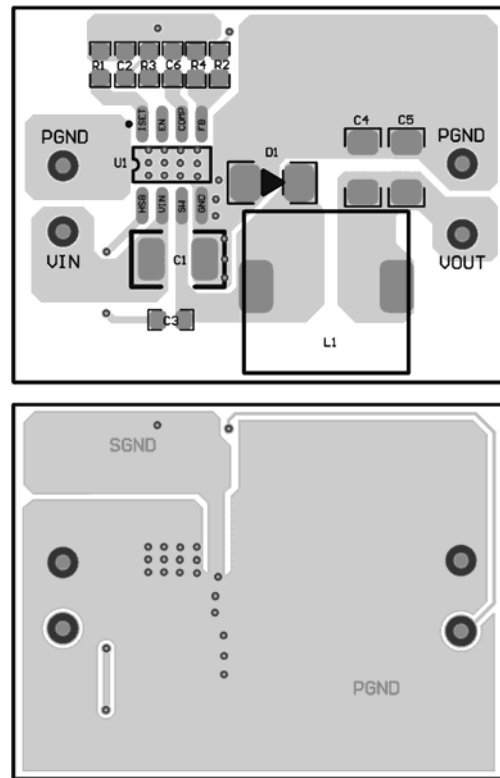
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

- 1) Arrange the power components to reduce the AC loop size consisting of  $C_{IN}$ , IN pin, SW pin and the schottky diode.
- 2) Place input decoupling ceramic capacitor  $C_{IN}$  as close to IN pin as possible.  $C_{IN}$  is connected

power GND with vias or short and wide path.

- 3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
- 4) Use copper plane for power GND for best heat dissipation and noise immunity.
- 5) Place feedback resistor close to FB pin.
- 6) Use short trace connecting HSB- $C_{HSB}$ -SW loop

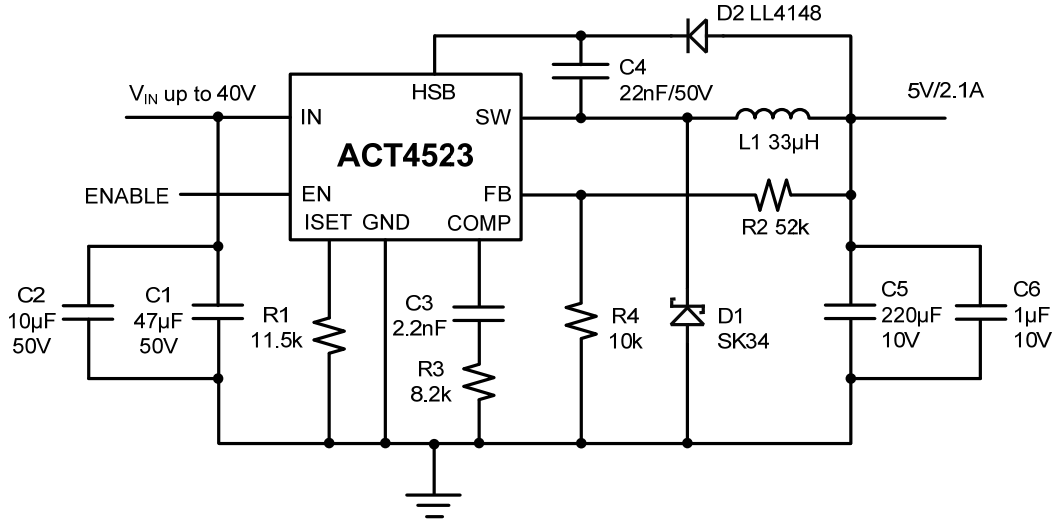
Figure 8 shows an example of PCB layout.



**Figure 8: PCB Layout**

Figure 9 gives one typical car charger application schematic and associated BOM list.

**Figure 9:**  
**Typical Application Circuit for 5V/2.1A Car Charger**

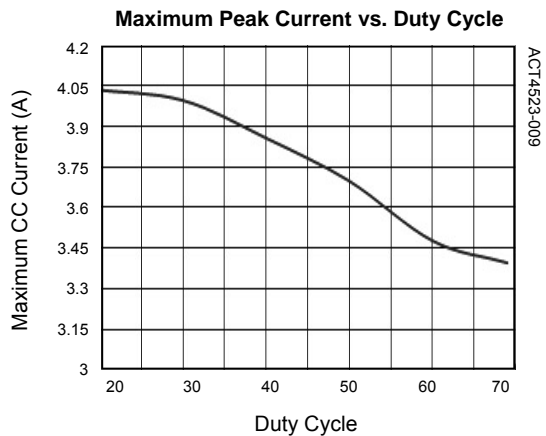
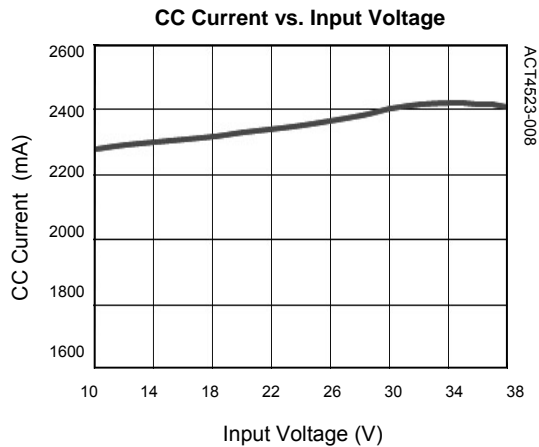
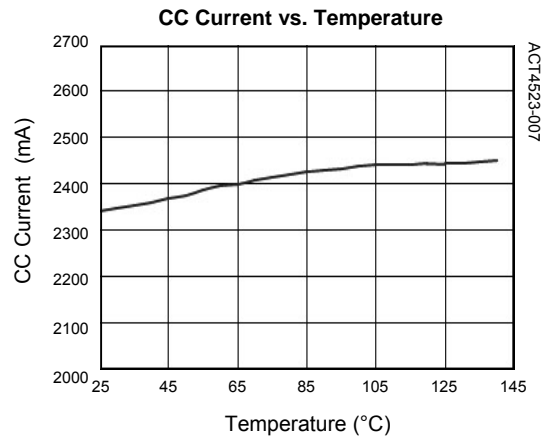
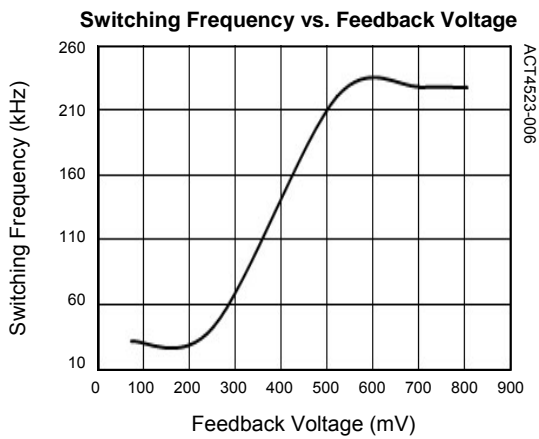
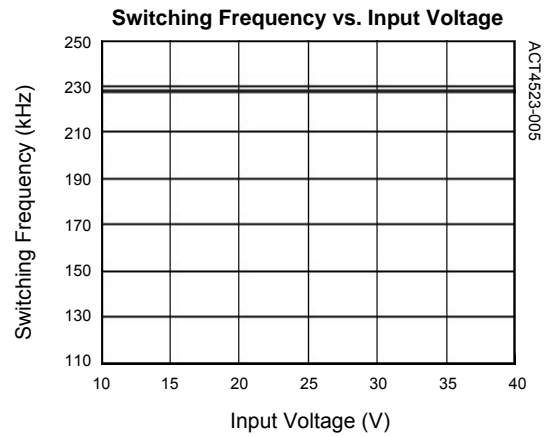
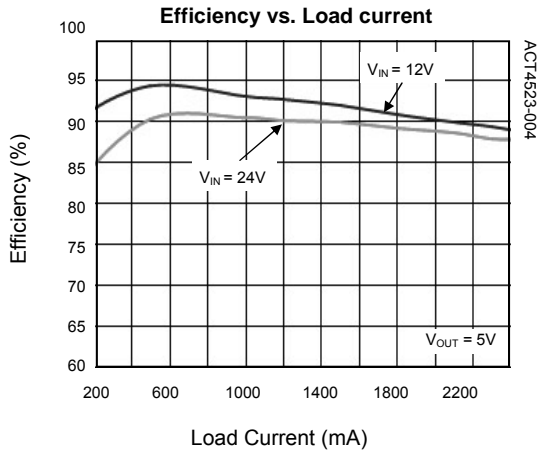


**Table 2:**  
**BOM List for 5V/2.1A Car Charger**

| ITEM | REFERENCE | DESCRIPTION                                 | MANUFACTURER     | QTY |
|------|-----------|---|------------------|-----|
| 1    | U1        | IC, ACT4523YH, SOP-8EP                      | Active-Semi      | 1   |
| 2    | C1        | Capacitor, Electrolytic, 47µF/50V, 6.3x7mm  | Murata, TDK      | 1   |
| 3    | C2        | Capacitor, Ceramic, 10µF/50V, 1206, SMD     | Murata, TDK      | 1   |
| 4    | C3        | Capacitor, Ceramic, 2.2nF/6.3V, 0603, SMD   | Murata, TDK      | 1   |
| 5    | C4        | Capacitor, Ceramic, 22nF/50V, 1206, SMD     | Murata, TDK      | 1   |
| 6    | C5        | Capacitor, Electrolytic, 220µF/10V, 6.3x7mm | Murata, TDK      | 1   |
| 7    | C6        | Capacitor, Ceramic, 1µF/10V, 0603, SMD      | Murata, TDK      | 1   |
| 8    | L1        | Inductor, 33µH, 3A, 20%, SMD                | Tyco Electronics | 1   |
| 9    | D1        | Diode, Schottky, 40V/3A, SK34               | Diodes           | 1   |
| 10   | D2        | Diode, 75V/150mA, LL4148                    | Good-ARK         | 1   |
| 11   | R1        | Chip Resistor, 11.5kΩ, 0603, 1%             | Murata, TDK      | 1   |
| 12   | R2        | Chip Resistor, 52kΩ, 0603, 1%               | Murata, TDK      | 1   |
| 13   | R3        | Chip Resistor, 8.2kΩ, 0603, 5%              | Murata, TDK      | 1   |
| 14   | R4        | Chip Resistor, 10kΩ, 0603, 1%               | Murata, TDK      | 1   |

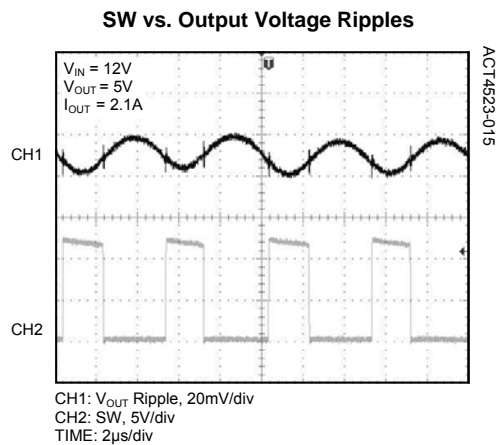
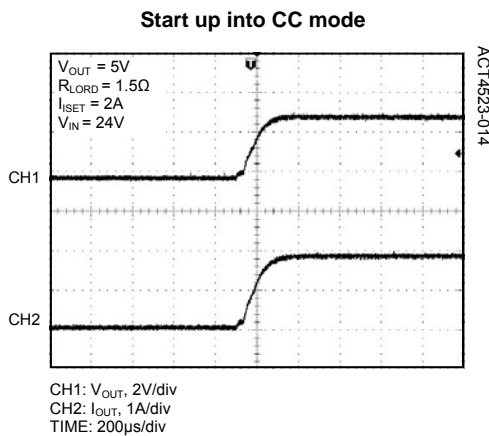
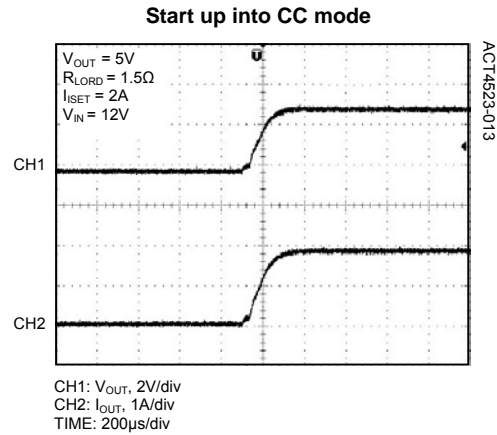
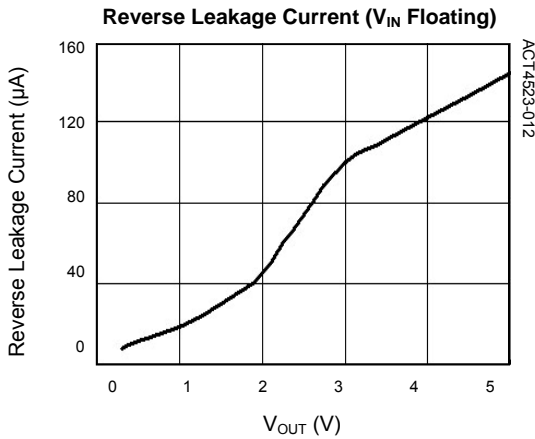
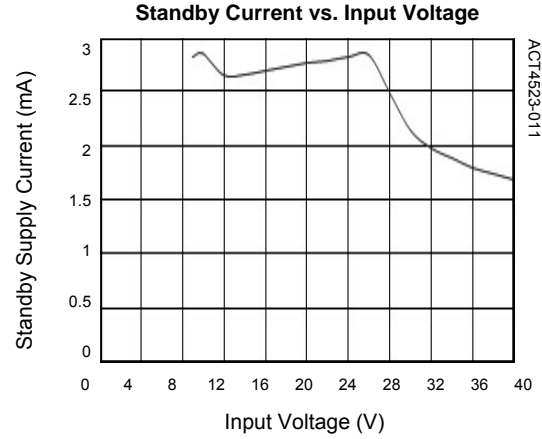
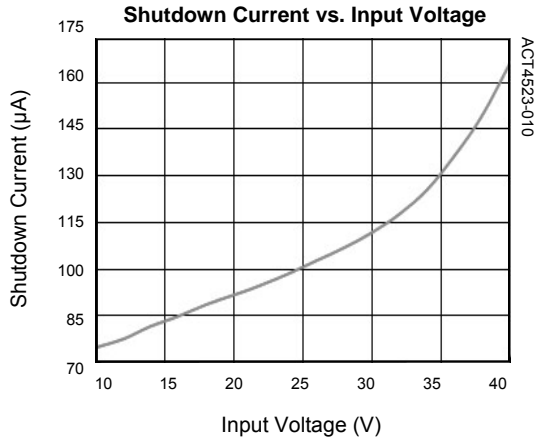
## TYPICAL PERFORMANCE CHARACTERISTICS

(L = 33μH, C<sub>IN</sub> = 10μF, C<sub>OUT</sub> = 47μF, T<sub>a</sub> = 25°C, R<sub>COMP</sub> = 8.2k, C<sub>COMP1</sub> = 2.2nF, C<sub>COMP2</sub> = NC)



## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

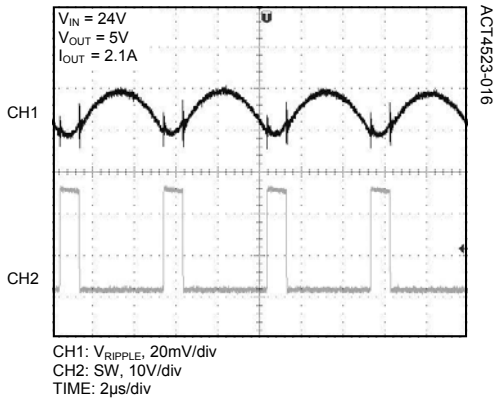
(L = 33 $\mu$ H, C<sub>IN</sub> = 10 $\mu$ F, C<sub>OUT</sub> = 47 $\mu$ F, T<sub>a</sub> = 25 $^{\circ}$ C, R<sub>COMP</sub> = 8.2k, C<sub>COMP1</sub> = 2.2nF, C<sub>COMP2</sub> = NC)



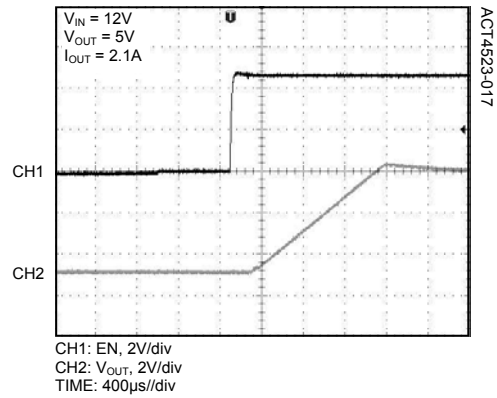
## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(L = 33μH, C<sub>IN</sub> = 10μF, C<sub>OUT</sub> = 47μF, T<sub>a</sub> = 25°C, R<sub>COMP</sub> = 8.2k, C<sub>COMP1</sub> = 2.2nF, C<sub>COMP2</sub> = NC)

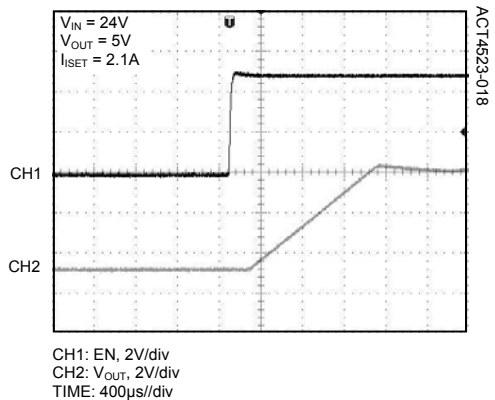
**SW vs. Output Voltage Ripple**



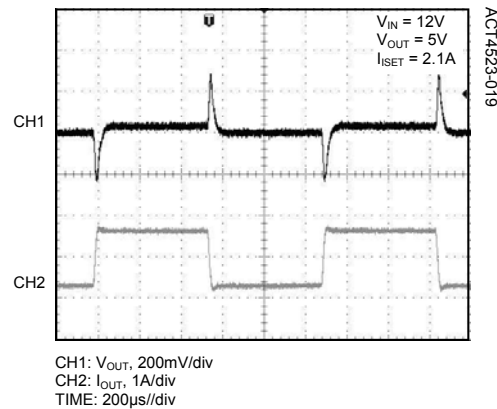
**Start up with EN**



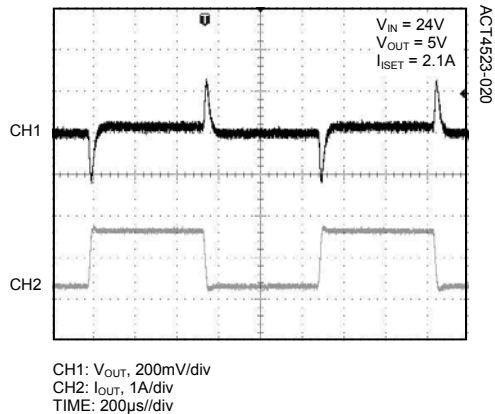
**Start up with EN**



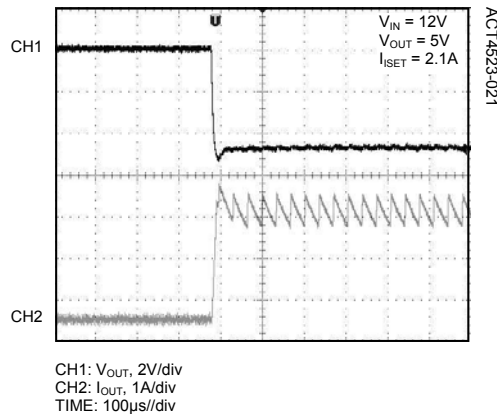
**Load Step Waveforms**



**Load Step Waveforms**

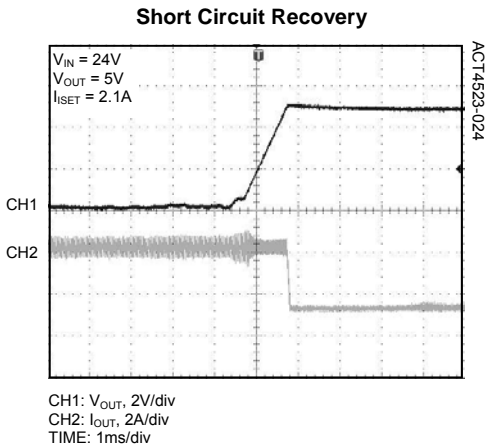
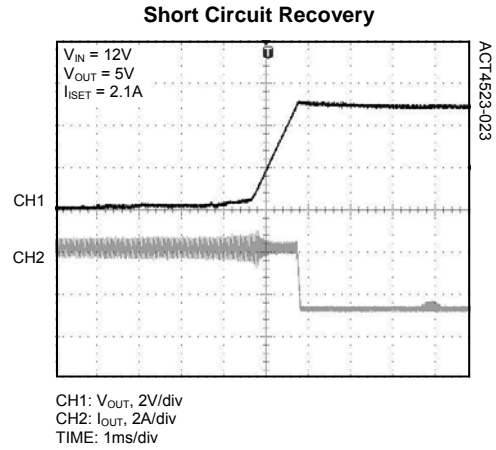
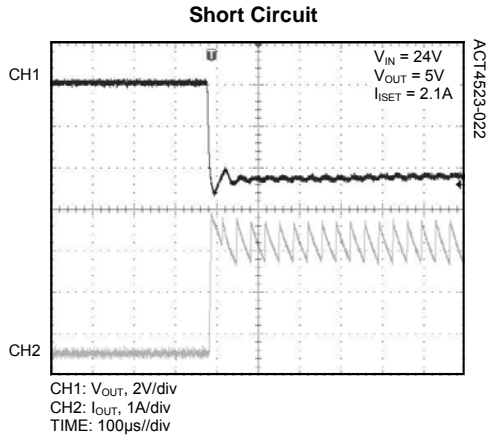


**Short Circuit**



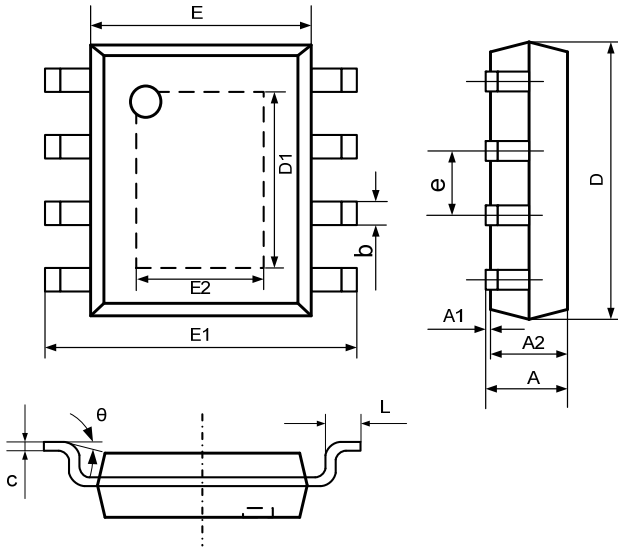
## TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(L = 33 $\mu$ H, C<sub>IN</sub> = 10 $\mu$ F, C<sub>OUT</sub> = 47 $\mu$ F, Ta = 25°C, R<sub>COMP</sub> = 8.2k, C<sub>COMP1</sub> = 2.2nF, C<sub>COMP2</sub> = NC)



## PACKAGE OUTLINE

### SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



| SYMBOL | DIMENSION IN MILLIMETERS |       | DIMENSION IN INCHES |       |
|--------|--------------------------|-------|---------------------|-------|
|        | MIN                      | MAX   | MIN                 | MAX   |
| A      | 1.350                    | 1.700 | 0.053               | 0.067 |
| A1     | 0.000                    | 0.100 | 0.000               | 0.004 |
| A2     | 1.350                    | 1.550 | 0.053               | 0.061 |
| b      | 0.330                    | 0.510 | 0.013               | 0.020 |
| c      | 0.170                    | 0.250 | 0.007               | 0.010 |
| D      | 4.700                    | 5.100 | 0.185               | 0.200 |
| D1     | 3.202                    | 3.402 | 0.126               | 0.134 |
| E      | 3.800                    | 4.000 | 0.150               | 0.157 |
| E1     | 5.800                    | 6.200 | 0.228               | 0.244 |
| E2     | 2.313                    | 2.513 | 0.091               | 0.099 |
| e      | 1.270 TYP                |       | 0.050 TYP           |       |
| L      | 0.400                    | 1.270 | 0.016               | 0.050 |
| θ      | 0°                       | 8°    | 0°                  | 8°    |

Note:

1. Lead Coplanarity is 0.1mm max.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
3. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. For the package reflow, 3x IR reflow is the maximum allowable reflow times for the SOP-8 standard and EP package families during the board mounting process.

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