

FEATURES

High speed

400 MHz, -3 dB full power bandwidth

2000 V/ μ s slew rate

Fixed gain of 2 with no external components

Internal common-mode feedback to improve gain and phase balance: -60 dB @ 10 MHz

Separate input to set the common-mode output voltage

Low distortion: 68 dB SFDR @ 5 MHz 200 Ω load

Power supply range +2.7 V to \pm 5 V

APPLICATIONS

Video line driver

Digital line driver

Low power differential ADC driver

Differential in/out level shifting

Single-ended input to differential output driver

GENERAL DESCRIPTION

The AD8131 is a differential or single-ended input to differential output driver requiring no external components for a fixed gain of 2. The AD8131 is a major advancement over op amps for driving signals over long lines or for driving differential input ADCs. The AD8131 has a unique internal feedback feature that provides output gain and phase matching that are balanced to -60 dB at 10 MHz, reducing radiated EMI and suppressing harmonics. Manufactured on the Analog Devices, Inc. next generation XFCB bipolar process, the AD8131 has a -3 dB bandwidth of 400 MHz and delivers a differential signal with very low harmonic distortion.

The AD8131 is a differential driver for the transmission of high-speed signals over low-cost twisted pair or coax cables. The AD8131 can be used for either analog or digital video signals or for other high-speed data transmission. The AD8131 driver is capable of driving either Cat3 or Cat5 twisted pair or coax with minimal line attenuation. The AD8131 has considerable cost and performance improvements over discrete line driver solutions.

The AD8131 can replace transformers in a variety of applications, preserving low frequency and dc information. The AD8131 does not have the susceptibility to magnetic interference and hysteresis of transformers. It is smaller, easier to work with, and has the high reliability associated with ICs.

Rev. B

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FUNCTIONAL BLOCK DIAGRAM

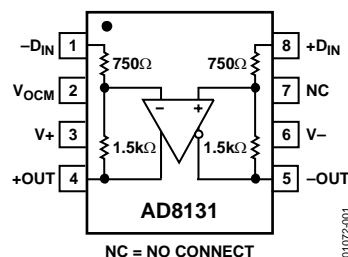


Figure 1.

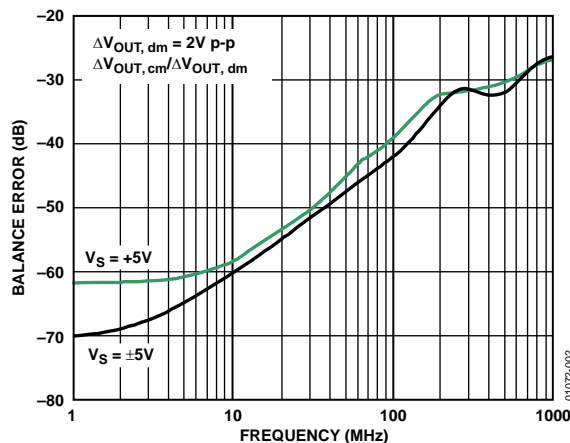


Figure 2. Output Balance Error vs. Frequency

The AD8131's differential output also helps balance the input for differential ADCs, optimizing the distortion performance of the ADCs. The common-mode level of the differential output is adjustable by a voltage on the V_{OCM} pin, easily level-shifting the input signals for driving single-supply ADCs with dual supply signals. Fast overload recovery preserves sampling accuracy.

The AD8131 is available in both SOIC and MSOP packages for operation over -40°C to $+125^{\circ}\text{C}$.

IMPORTANT LINKS for the [AD8131](#)*

Last content update 08/23/2013 05:36 pm

PARAMETRIC SELECTION TABLES

[Find Similar Products By Operating Parameters](#)

[Amplifiers for Video Distribution](#)

[High Speed Amplifiers Selection Table](#)

DOCUMENTATION

AN-692: Universal Precision Op Amp Evaluation Board

AN-649: Using the Analog Devices Active Filter Design Tool

AN-357: Operational Integrators

AN-356: User's Guide to Applying and Measuring Operational Amplifier Specifications

AN-584: Using the AD813X Differential Amplifier

[Video Amplifier Products](#)

UG-474: Evaluation Board for Differential Amplifiers Offered in 8-Lead SOIC Packages

UG-130: Differential Amplifier Evaluation Board for 8-lead SOIC and MSOP Packages

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[Security and Surveillance Applications Booklet](#)

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DESIGN TOOLS, MODELS, DRIVERS & SOFTWARE

[Analog Filter Wizard 2.0](#)

[AD8131 SPICE Macro-Model Maximum Values](#)

[AD8131 SPICE Macro-Model Typical Values](#)

EVALUATION KITS & SYMBOLS & FOOTPRINTS

[View the Evaluation Boards and Kits page for the AD8131](#)

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REVISION HISTORY

6/05—Rev. A to Rev. B

Updated Format.....	Universal
Changed Upper Operating Limit	Universal
Changes to Ordering Guide	20

SPECIFICATIONS

$\pm D_{IN}$ TO $\pm OUT$ SPECIFICATIONS

25°C, $V_S = \pm 5\text{ V}$, $V_{OCM} = 0\text{ V}$, $G = 2$, $R_{L, dm} = 200\ \Omega$, unless otherwise noted. Refer to Figure 5 and Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	$V_{OUT} = 2\text{ V p-p}$		400		MHz
–3 dB Small Signal Bandwidth	$V_{OUT} = 0.2\text{ V p-p}$		320		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 0.2\text{ V p-p}$		85		MHz
Slew Rate	$V_{OUT} = 2\text{ V p-p}$, 10% to 90%		2000		V/ μs
Settling Time	0.1%, $V_{OUT} = 2\text{ V p-p}$		14		ns
Overdrive Recovery Time	$V_{IN} = 5\text{ V}$ to 0 V Step		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 200\ \Omega$		–68		dBc
	$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 200\ \Omega$		–63		dBc
	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 800\ \Omega$		–95		dBc
	$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 800\ \Omega$		–79		dBc
	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 200\ \Omega$		–94		dBc
	$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 200\ \Omega$		–70		dBc
	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 800\ \Omega$		–101		dBc
	$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 800\ \Omega$		–77		dBc
Third Harmonic	20 MHz, $R_{L, dm} = 800\ \Omega$		–54		dBc
	20 MHz, $R_{L, dm} = 800\ \Omega$		30		dBm
	$f = 20\text{ MHz}$		25		nV/ $\sqrt{\text{Hz}}$
	NTSC, $R_{L, dm} = 150\ \Omega$		0.01		%
	NTSC, $R_{L, dm} = 150\ \Omega$		0.06		degrees
INPUT CHARACTERISTICS					
Input Resistance	Single-ended input		1.125		k Ω
	Differential input		1.5		k Ω
Input Capacitance			1		pF
Input Common-Mode Voltage			–7.0 to +5.0		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm} = \pm 0.5\text{ V}$		–70		dB
OUTPUT CHARACTERISTICS					
Offset Voltage (RTO)	$V_{OS, dm} = V_{OUT, dm}$; $V_{DIN+} = V_{DIN-} = V_{OCM} = 0\text{ V}$		± 2	± 7	mV
	T_{MIN} to T_{MAX} variation		± 8		$\mu\text{V}/^\circ\text{C}$
	$V_{OCM} = \text{float}$		± 4		mV
	T_{MIN} to T_{MAX} variation		± 10		$\mu\text{V}/^\circ\text{C}$
Output Voltage Swing	Maximum ΔV_{OUT} ; single-ended output		–3.6 to +3.6		V
Linear Output Current			60		mA
Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$; $\Delta V_{IN, dm} = \pm 0.5\text{ V}$	1.97	2	2.03	V/V
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm} = 1\text{ V}$		–70		dB

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V_{OCM} TO \pm OUT SPECIFICATIONS

25°C, V_S = \pm 5 V, V_{OCM} = 0 V, G = 2, R_{L, dm} = 200 Ω , unless otherwise noted. Refer to Figure 5 and Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$\Delta V_{OCM} = 600 \text{ mV}$		210		MHz
Slew Rate	V _{OCM} = –1 V to +1 V		500		V/ μ s
DC PERFORMANCE					
Input Voltage Range			± 3.6		V
Input Resistance			120		k Ω
Input Offset Voltage	V _{OS, cm} = V _{OUT, cm} ; V _{DIN+} = V _{DIN–} = V _{OCM} = 0 V V _{OCM} = float		± 1.5	± 7	mV
Input Bias Current			± 2.5		mV
VOCM CMRR			0.5		μ A
Gain	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; $\Delta V_{OCM} = \pm 0.5 \text{ V}$ $\Delta V_{OUT, cm}/\Delta V_{OCM}$; $\Delta V_{OCM} = \pm 1 \text{ V}$		–60		dB
POWER SUPPLY					
Operating Range		± 1.4		± 5.5	V
Quiescent Current	V _{DIN+} = V _{DIN–} = V _{OCM} = 0 V T _{MIN} to T _{MAX} variation	10.5	11.5	12.5	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; $\Delta V_S = \pm 1 \text{ V}$		25		μ A/°C
OPERATING TEMPERATURE RANGE		–40		+125	°C

±D_{IN} TO ±OUT SPECIFICATIONS

25°C, $V_S = 5\text{ V}$, $V_{OCM} = 2.5\text{ V}$, $G = 2$, $R_{L, dm} = 200\ \Omega$, unless otherwise noted. Refer to Figure 5 and Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	$V_{OUT} = 2\text{ V p-p}$		385		MHz
–3 dB Small Signal Bandwidth	$V_{OUT} = 0.2\text{ V p-p}$		285		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 0.2\text{ V p-p}$		65		MHz
Slew Rate	$V_{OUT} = 2\text{ V p-p}$, 10% to 90%		1600		V/ μ s
Settling Time	0.1%, $V_{OUT} = 2\text{ V p-p}$		18		ns
Overdrive Recovery Time	$V_{IN} = 5\text{ V}$ to 0 V Step		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 200\ \Omega$		–67		dBc
	$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 200\ \Omega$		–56		dBc
	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 800\ \Omega$		–94		dBc
	$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 800\ \Omega$		–77		dBc
	Third Harmonic	$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 200\ \Omega$	–74		dBc
		$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 200\ \Omega$	–67		dBc
		$V_{OUT} = 2\text{ V p-p}$, 5 MHz, $R_{L, dm} = 800\ \Omega$	–95		dBc
		$V_{OUT} = 2\text{ V p-p}$, 20 MHz, $R_{L, dm} = 800\ \Omega$	–74		dBc
IMD	20 MHz, $R_{L, dm} = 800\ \Omega$		–51		dBc
IP3	20 MHz, $R_{L, dm} = 800\ \Omega$		29		dBm
Voltage Noise (RTO)	$f = 20\text{ MHz}$		25		nV/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $R_{L, dm} = 150\ \Omega$		0.02		%
Differential Phase Error	NTSC, $R_{L, dm} = 150\ \Omega$		0.08		degrees
INPUT CHARACTERISTICS					
Input Resistance	Single-ended input		1.125		k Ω
	Differential input		1.5		k Ω
Input Capacitance			1		pF
Input Common-Mode Voltage			–1.0 to +4.0		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm} = \pm 0.5\text{ V}$		–70		dB
OUTPUT CHARACTERISTICS					
Offset Voltage (RTO)	$V_{OS, dm} = V_{OUT, dm}$; $V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5\text{ V}$		±3	±7	mV
	T_{MIN} to T_{MAX} variation		±8		$\mu\text{V}/^\circ\text{C}$
	$V_{OCM} = \text{float}$		±4		mV
	T_{MIN} to T_{MAX} variation		±10		$\mu\text{V}/^\circ\text{C}$
Output Voltage Swing	Maximum ΔV_{OUT} ; single-ended output		1.0 to 3.7		V
Linear Output Current			45		mA
Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$; $\Delta V_{IN, dm} = \pm 0.5\text{ V}$	1.96	2	2.04	V/V
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm} = 1\text{ V}$		–62		dB

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V_{OCM} TO \pm OUT SPECIFICATIONS

25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = 2, R_{L, dm} = 200 Ω , unless otherwise noted. Refer to Figure 5 and Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$\Delta V_{OCM} = 600 \text{ mV}$		200		MHz
Slew Rate	$V_{OCM} = 1.5 \text{ V to } 3.5 \text{ V}$		450		V/ μ s
DC PERFORMANCE					
Input Voltage Range			1.0 to 3.7		V
Input Resistance			30		k Ω
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 \text{ V}$ $V_{OCM} = \text{float}$		± 5 ± 10	± 12	mV mV
Input Bias Current			0.5		μ A
V _{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}; \Delta V_{OCM} = 2.5 \text{ V} \pm 0.5 \text{ V}$		–60		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}; \Delta V_{OCM} = 2.5 \text{ V} \pm 1 \text{ V}$	0.985	1	1.015	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current	$V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 \text{ V}$ T_{MIN} to T_{MAX} variation	9.25	10.25	11.25	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S; \Delta V_S = \pm 0.5 \text{ V}$		–70	–56	dB
OPERATING TEMPERATURE RANGE		–40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.¹

Parameter	Rating
Supply Voltage	± 5.5 V
V_{OCM}	$\pm V_S$
Internal Power Dissipation	250 mW
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering 10 sec)	300°C

¹Thermal resistance measured on SEMI standard 4-layer board.
 8-lead SOIC: $\theta_{JA} = 121^{\circ}\text{C/W}$.
 8-lead MSOP: $\theta_{JA} = 142^{\circ}\text{C/W}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

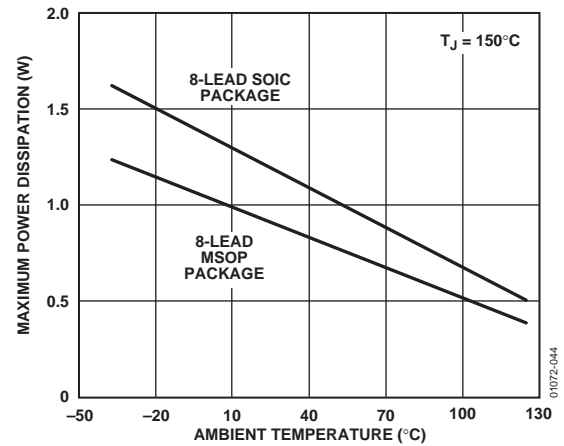


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD8131

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

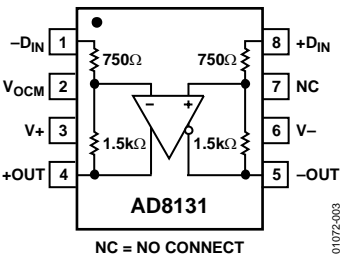


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$-D_{IN}$	Negative Input.
2	V_{OCM}	Common-Mode Output Voltage. Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} will set the dc bias level on +OUT and -OUT to 1 V.
3	$V+$	Positive Supply Voltage.
4	+OUT	Positive Output. Note: the voltage at $-D_{IN}$ is inverted at +OUT.
5	-OUT	Negative Output. Note: the voltage at $+D_{IN}$ is inverted at -OUT.
6	$V-$	Negative Supply Voltage.
7	NC	No Connect.
8	$+D_{IN}$	Positive Input.

TYPICAL PERFORMANCE CHARACTERISTICS

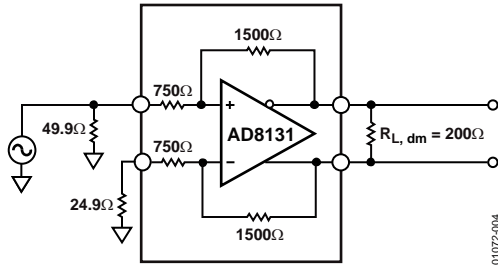


Figure 5. Basic Test Circuit

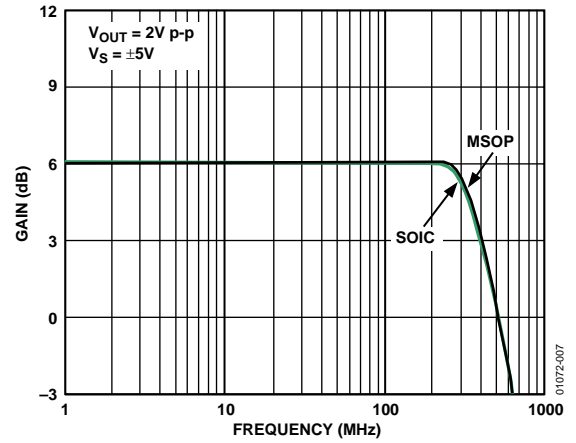


Figure 8. Large Signal Frequency Response

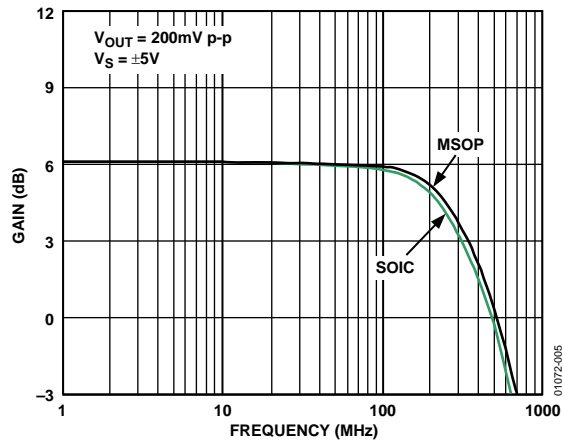


Figure 6. Small Signal Frequency Response

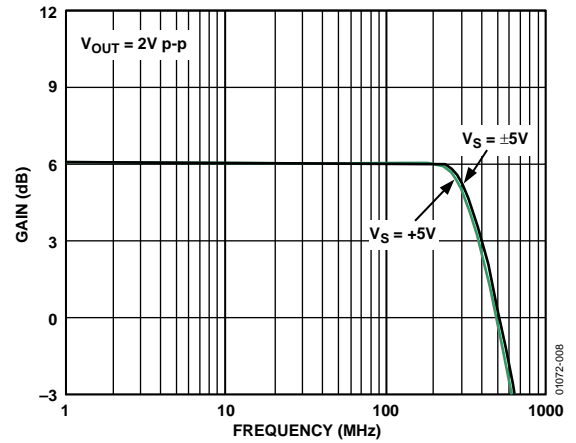


Figure 9. Large Signal Frequency Response

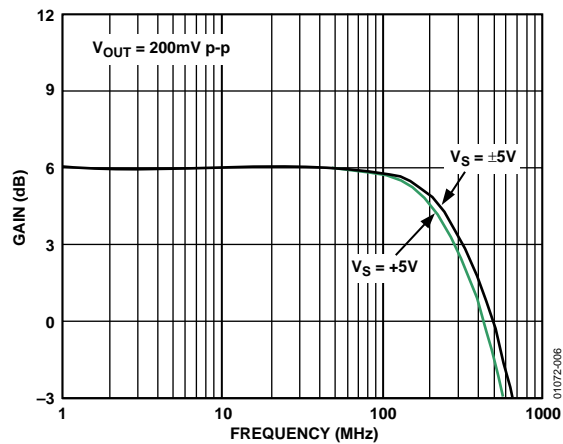


Figure 7. Small Signal Frequency Response

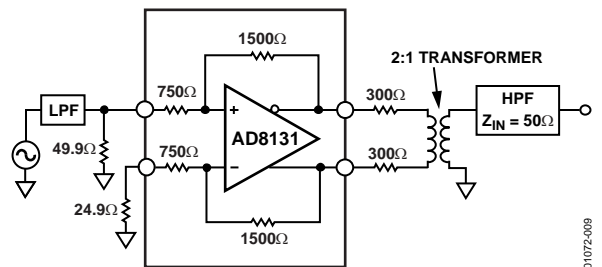


Figure 10. Harmonic Distortion Test Circuit ($R_{L, dm} = 800\Omega$)

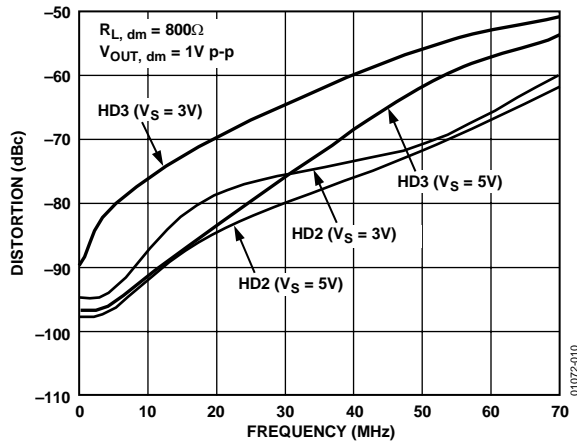


Figure 11. Harmonic Distortion vs. Frequency

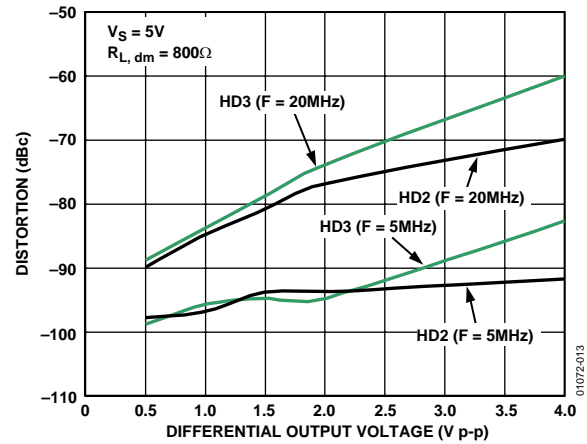


Figure 14. Harmonic Distortion vs. Differential Output Voltage

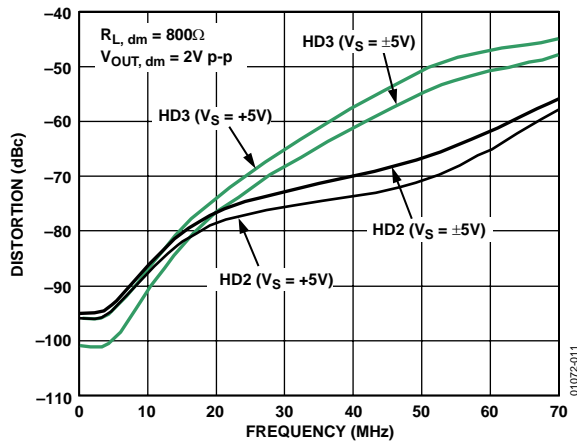


Figure 12. Harmonic Distortion vs. Frequency

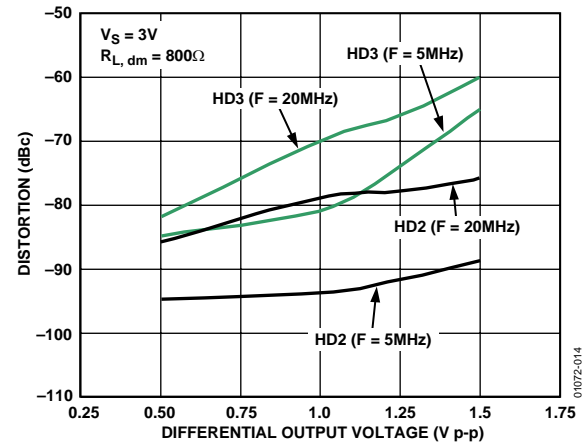


Figure 15. Harmonic Distortion vs. Differential Output Voltage

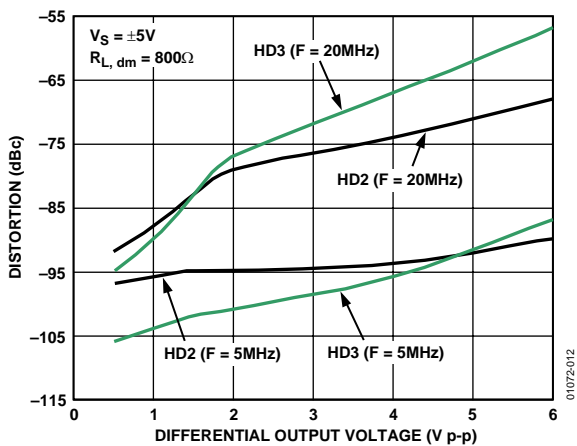


Figure 13. Harmonic Distortion vs. Differential Output Voltage

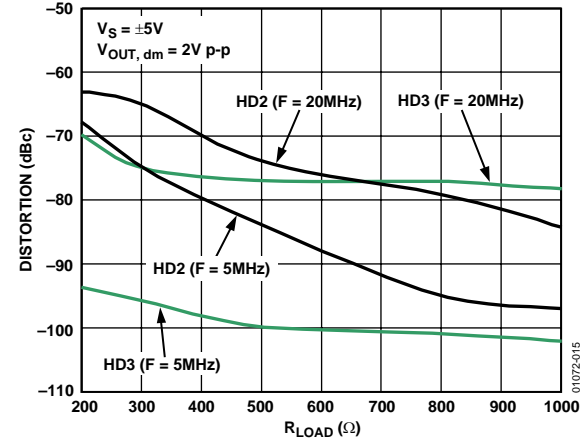


Figure 16. Harmonic Distortion vs. R_{LOAD}

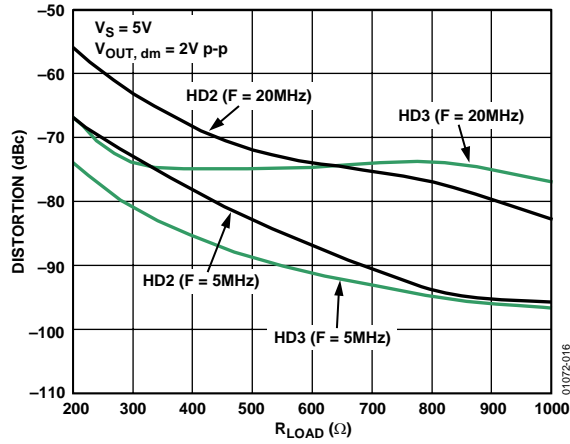


Figure 17. Harmonic Distortion vs. R_{LOAD}

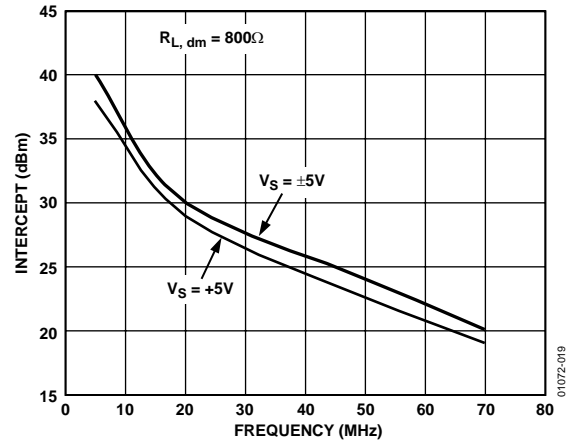


Figure 20. Third Order Intercept vs. Frequency

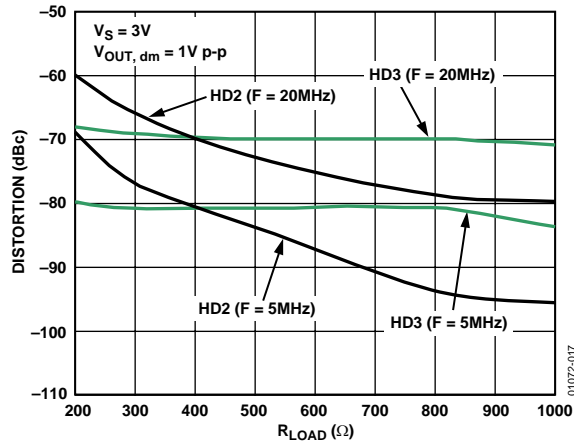


Figure 18. Harmonic Distortion vs. R_{LOAD}

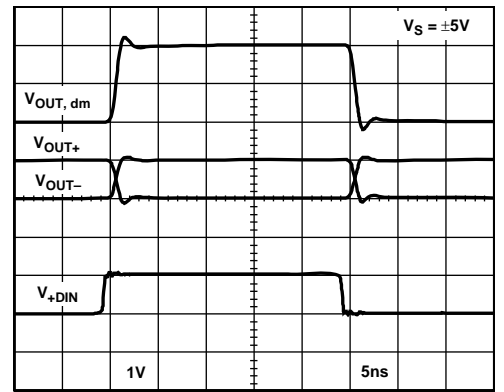


Figure 21. Large Signal Transient Response

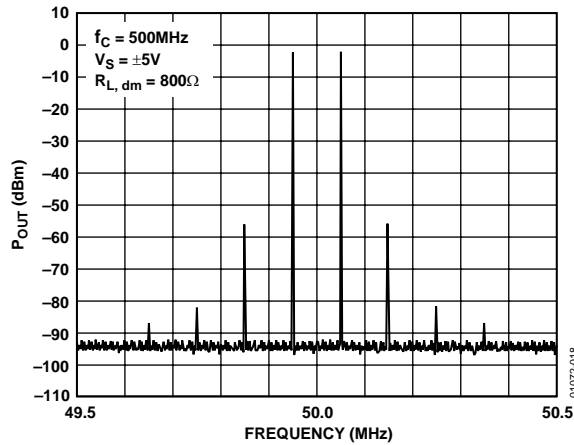


Figure 19. Intermodulation Distortion

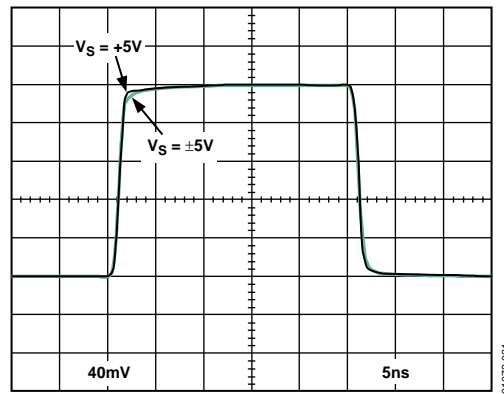


Figure 22. Small Signal Transient Response

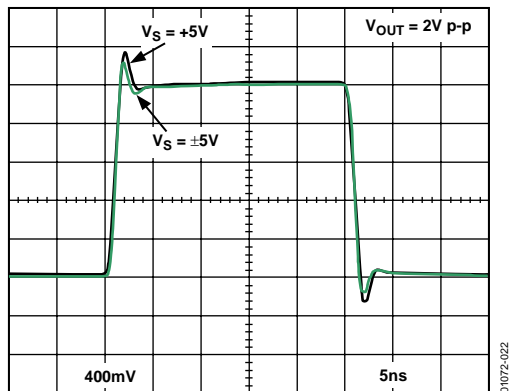


Figure 23. Large Signal Transient Response

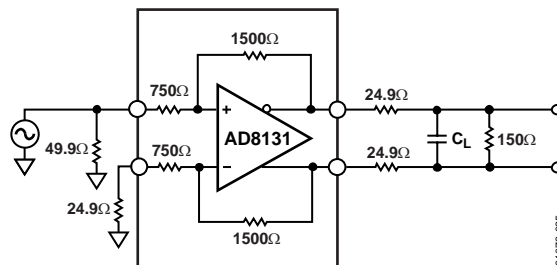


Figure 26. Capacitor Load Drive Test Circuit

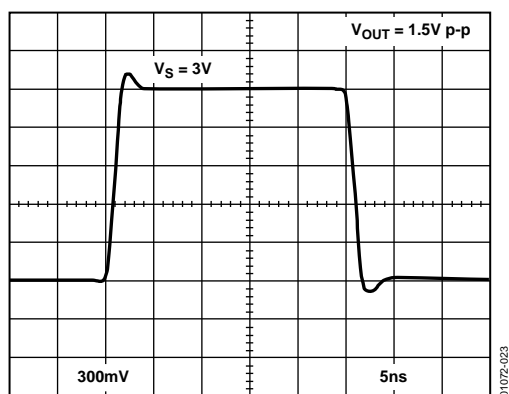


Figure 24. Large Signal Transient Response

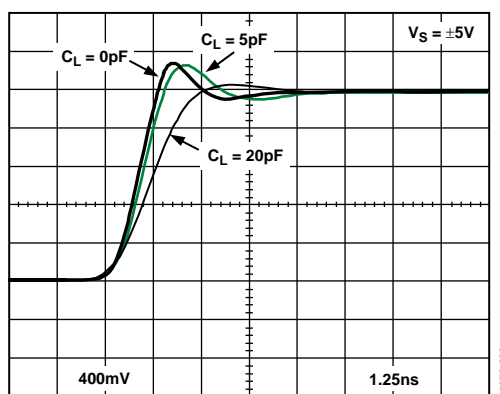


Figure 27. Large Signal Transient Response for Various Capacitor Loads

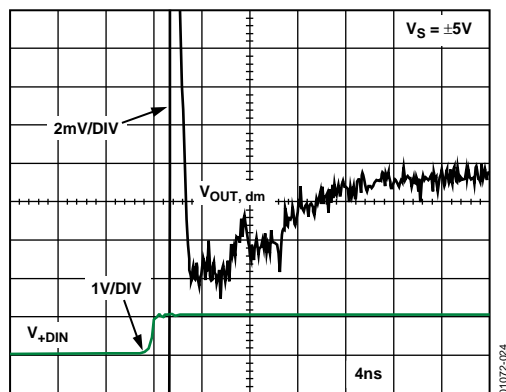


Figure 25. 0.1% Settling Time

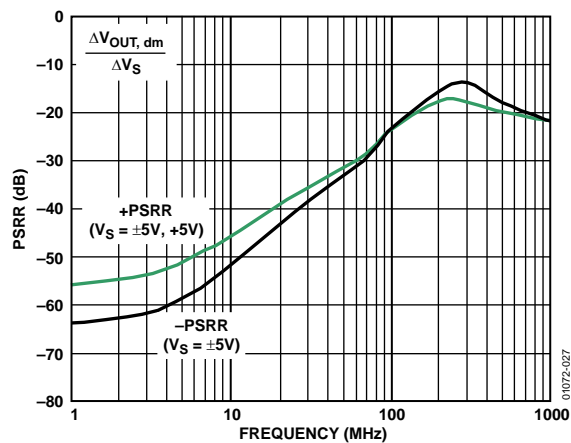


Figure 28. PSRR vs. Frequency

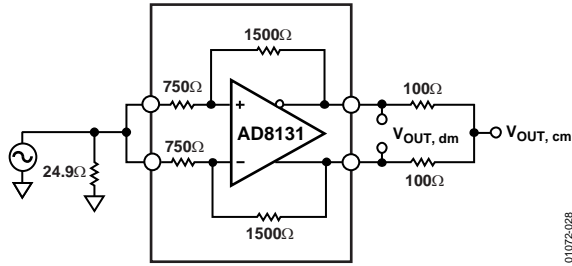


Figure 29. CMRR Test Circuit

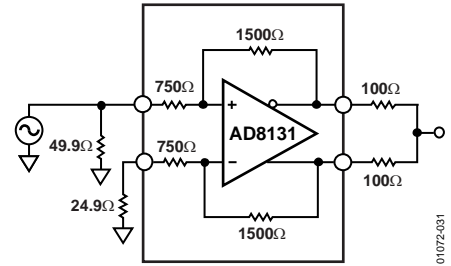


Figure 32. Output Balance Error Test Circuit

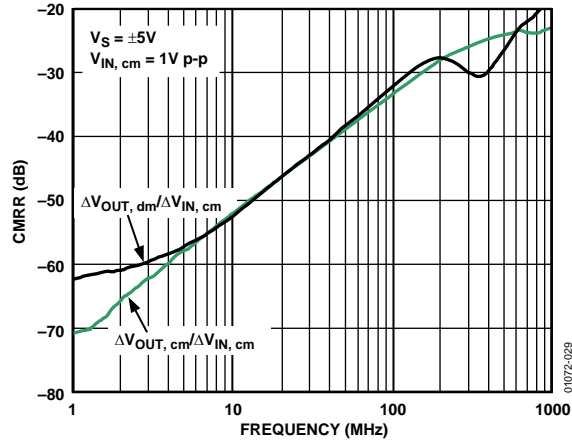


Figure 30. CMRR vs. Frequency

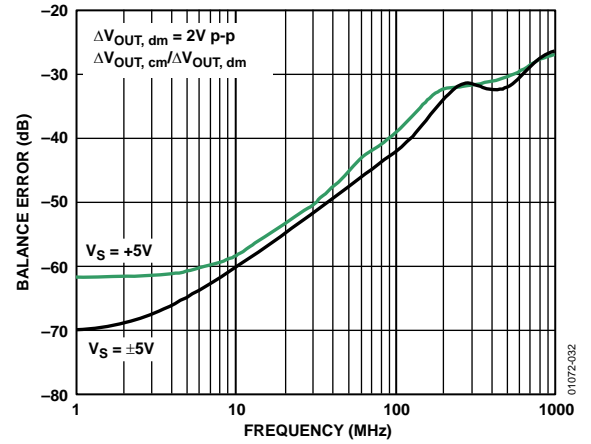


Figure 33. Output Balance Error vs. Frequency

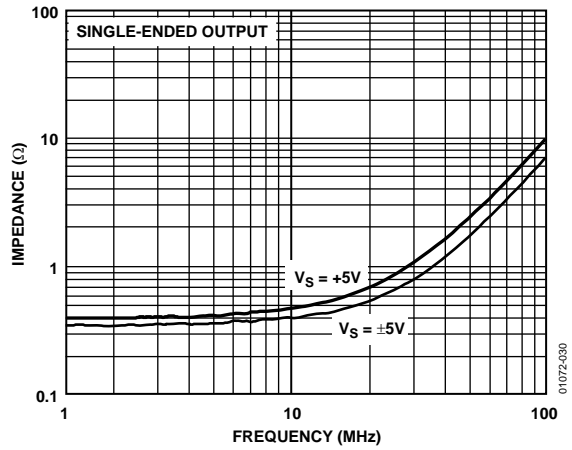


Figure 31. Single-Ended Z_{OUT} vs. Frequency

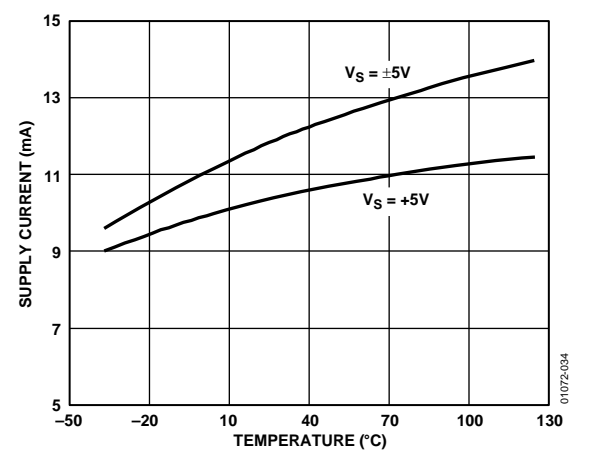


Figure 34. Quiescent Current vs. Temperature

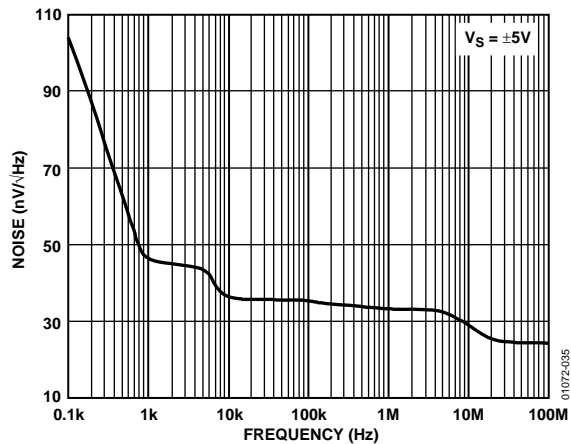


Figure 35. Voltage Noise vs. Frequency

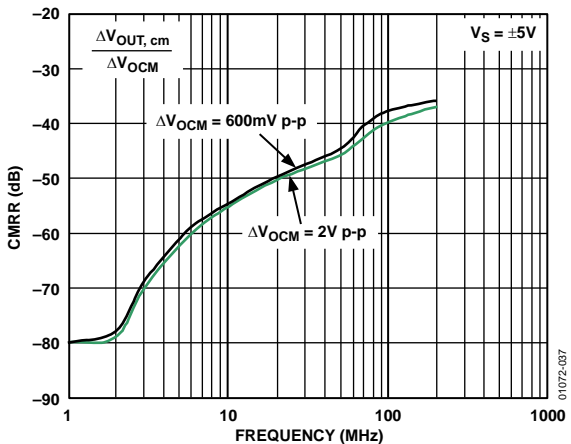


Figure 37. V_{OCM} CMRR vs. Frequency

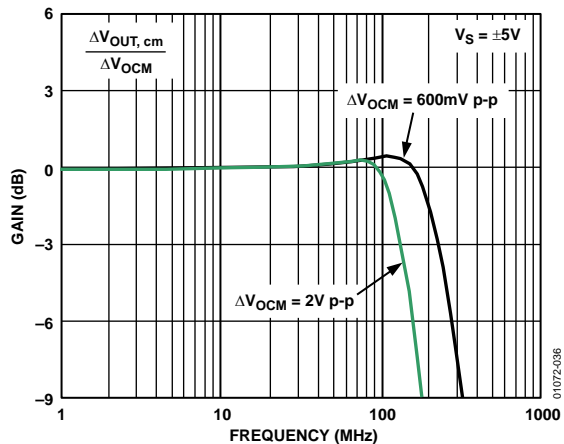


Figure 36. V_{OCM} Gain Response

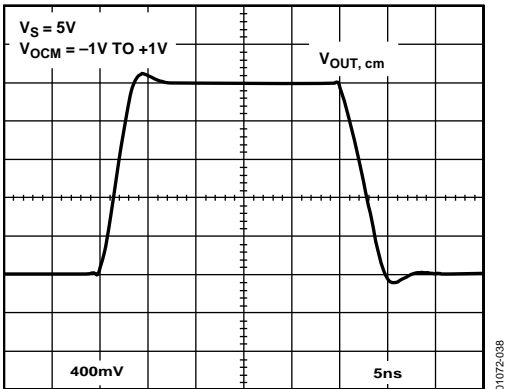


Figure 38. V_{OCM} Transient Response

THEORY OF OPERATION

The AD8131 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8131 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals.

Previous discrete and integrated differential driver designs used two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level shifting has also been difficult with previous differential drivers. Level shifting required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

The AD8131 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set by internal resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the common-mode output level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The AD8131 architecture results in outputs that are very highly balanced over a wide frequency range without requiring external components or adjustments. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs, of identical amplitude and exactly 180 degrees apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The AD8131 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and –IN in Figure 39. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also

be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 39 can be described by the following equation:

$$\left| \frac{V_{OUT, dm}}{V_{IN, dm}} \right| = \frac{R_F}{R_G} = 2$$

where $R_F = 1.5 \text{ k}\Omega$ and $R_G = 750 \text{ }\Omega$ nominally.

ESTIMATING THE OUTPUT NOISE VOLTAGE

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and –IN, by the circuit noise gain. The noise gain is defined as

$$G_N = 1 + \left(\frac{R_F}{R_G} \right) = 3$$

The total output referred noise for the AD8131, including the contributions of R_F , R_G , and op amp, is nominally $25 \text{ nV}/\sqrt{\text{Hz}}$ at 20 MHz.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit such as that in Figure 39, at + D_{IN} and – D_{IN} , will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN, dm}$) between the inputs (+ D_{IN} and – D_{IN}) is

$$R_{IN, dm} = 2 \times R_G = 1.5 \text{ k}\Omega$$

In the case of a single-ended input signal (for example if – D_{IN} is grounded and the input signal is applied to + D_{IN}), the input impedance becomes

$$R_{IN, dm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = 1.125 \text{ k}\Omega$$

The input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G .

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The AD8131 is optimized for level-shifting ground referenced input signals. For a single-ended input this would imply, for example, that the voltage at $-D_{IN}$ in Figure 39 would be zero volts when the amplifier's negative power supply voltage (at $V-$) was also set to zero volts.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The AD8131's V_{OCM} pin is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on $V+$ and $V-$). Relying on this internal bias results in an output common-mode voltage that is within about 25 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10 k Ω resistors), be used.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the pin and bondwire inductance of the AD8131 resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small resistor in series with the amplifier's outputs as shown in Figure 26.



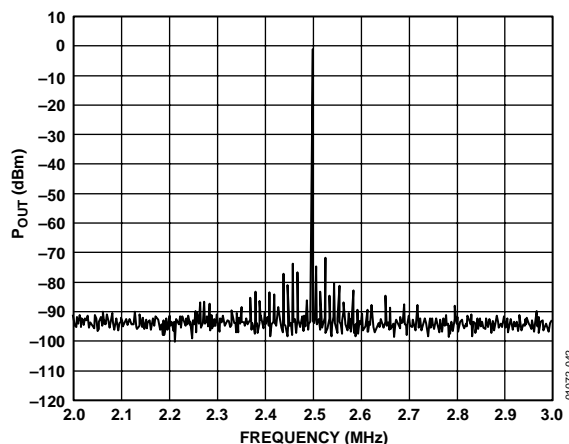


Figure 42. FFT Plot for AD8131/AD9203

UNITY-GAIN, SINGLE-ENDED-TO-DIFFERENTIAL DRIVER

If it is not necessary to offset the output common-mode voltage (via the V_{OCM} pin), then the AD8131 can make a simple unity-gain single-ended-to-differential amplifier that does not require any external components. Figure 43 shows the schematic for this circuit.

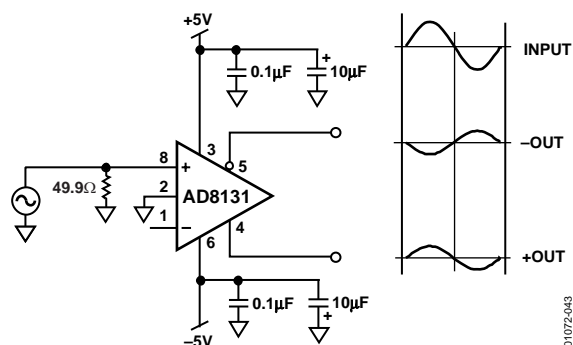
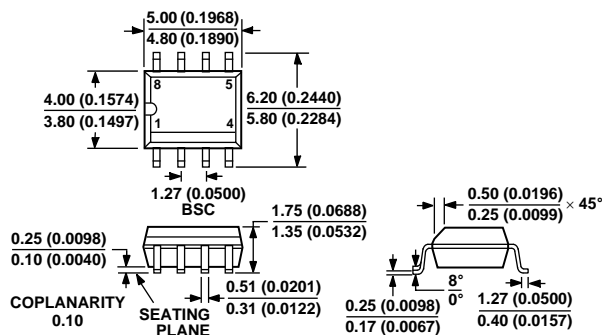


Figure 43. Unity Gain, Single-Ended-to-Differential Amplifier

As shown above, when $-D_{IN}$ is left floating, there is 100% feedback of $+OUT$ to $-IN$ via the internal feedback resistor. This contrasts with the typical gain of 2 operation where $-D_{IN}$ is grounded and one third of the $+OUT$ is fed back to $-IN$. The result is a closed-loop differential gain of 1.

Upon careful observation, it can be seen that only $+D_{IN}$ and V_{OCM} are referenced to ground. The ground voltage at V_{OCM} is the reference for this circuit. In this unity gain configuration, if a dc voltage is applied to V_{OCM} to shift the common-mode voltage, a differential dc voltage will be created at the output, along with the common-mode voltage change. Thus, this configuration cannot be used when it is desired to offset the common-mode voltage of the output with respect to the input at $+D_{IN}$.

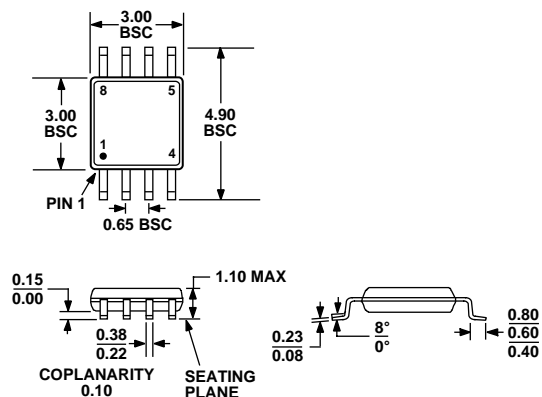
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 44. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body

(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 45. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8131AR	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8131AR-REEL	-40°C to +125°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8131AR-REEL7	-40°C to +125°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8131ARZ ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8131ARZ-REEL ¹	-40°C to +125°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8131ARZ-REEL7 ¹	-40°C to +125°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8131ARM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	HJA
AD8131ARM-REEL	-40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HJA
AD8131ARM-REEL7	-40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HJA
AD8131ARMZ ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	HJA#
AD8131ARMZ-REEL ¹	-40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HJA#
AD8131ARMZ-REEL7 ¹	-40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HJA#

¹ Z = Pb-free part, # denotes Pb-free part; may be top or bottom marked.

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