



## Introduction

This user guide introduces the evaluation kits for the Atmel® SAMA5D3 series embedded MPUs listed below:

- SAMA5D31
- SAMA5D33
- SAMA5D34
- SAMA5D35
- SAMA5D36

It pertains to the following evaluation kit references:

- SAMA5D31-EK
- SAMA5D33-EK
- SAMA5D34-EK
- SAMA5D35-EK
- SAMA5D36-EK

## Contents

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**Important:** Unpack and assemble the kit carefully, following the assembly guide provided in the box.

- Boards
  - One SAMA5D3 main board (MB)
  - One of the five available CPU module (CM) boards
    - SAMA5D31-CM
    - SAMA5D33-CM
    - SAMA5D34-CM
    - SAMA5D35-CM
    - SAMA5D36-CM
  - One optional Display Module (DM) board (5"\_WVGA\_R-DM), available for all SAMA5D3x evaluation kits that feature an LCD interface: SAMA5D31, SAMA5D33, SAMA5D34, SAMA5D36
- Power supply
  - One universal input AC/DC power supply with US, Europe and UK plug adapters
  - One 3V lithium battery type CR1225
- Cables
  - One micro A/B-type USB cable
  - One RJ45 crossed cable
- A welcome letter

## Related Items

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- [Atmel SAMA5D3 Series Datasheet](#)

## Table of Contents

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Introduction . . . . .	1
Contents . . . . .	2
Related Items . . . . .	2
Table of Contents . . . . .	3
<b>1. Evaluation Kit Specifications . . . . .</b>	<b>4</b>
1.1 Electrostatic Warning . . . . .	4
<b>2. Power Up . . . . .</b>	<b>5</b>
2.1 Power up the Board . . . . .	5
2.2 Sample Code and Technical Support . . . . .	5
<b>3. Evaluation Kit Hardware . . . . .</b>	<b>6</b>
3.1 Introduction . . . . .	6
<b>4. CPU Module (CM) Board . . . . .</b>	<b>7</b>
4.1 Overview . . . . .	7
4.2 Equipment List . . . . .	10
4.3 Functional Blocks . . . . .	12
4.4 Embest/Flextronics Schematics . . . . .	27
4.5 Ronetix Schematics . . . . .	43
<b>5. Main Board (MB) . . . . .</b>	<b>53</b>
5.1 Main Board Overview . . . . .	53
5.2 Function Blocks. . . . .	58
5.3 Configuration. . . . .	74
5.4 PIO Usage and Interface Connectors Details . . . . .	76
5.5 Main Board Schematics . . . . .	101
<b>6. Optional Display Module (DM) Board . . . . .</b>	<b>116</b>
6.1 DM Board Overview . . . . .	116
6.2 Schematics . . . . .	119
<b>7. Troubleshooting and Recommendations . . . . .</b>	<b>120</b>
7.1 Errata . . . . .	120
<b>8. Revision History . . . . .</b>	<b>121</b>

# 1. Evaluation Kit Specifications

Table 1-1. Evaluation Kit Specifications

Characteristic	Specifications
Clock speed	Up to 536 MHz PCK, up to 166 MHz MCK
Ports	10/100/1000 Ethernet, USB, RS232, JTAG, CAN, Audio, HDMI, SD card
Board supply voltage	5V DC from connector
Dimensions: MB (Main Board) CM (Computer Module) Board DM (Display Module) Board	165 * 135 * 20 mm 67.60 * (40 to 47) * 5 mm 135 * 80 * 6 mm
RoHS status	Compliant
CE and FCC Part 15 status	Compliant
Kit Identification	SAMA5D31-EK SAMA5D33-EK SAMA5D34-EK SAMA5D35-EK SAMA5D36-EK

## 1.1 Electrostatic Warning

**Warning:** ESD-Sensitive Electronic Equipment!

The evaluation kit is shipped in a protective anti-static package. The board system must not be subjected to high electrostatic potentials.

We strongly recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

## 2. Power Up

### 2.1 Power up the Board

Unpack the board, taking care to avoid electrostatic discharge. Unpack the power supply, select the right power plug adapter corresponding to that of your country and insert it in the power supply.

Connect the power supply DC connector to the board and plug the power supply to an AC power plug.

The LCD should light up and display a welcome page. Click or touch icons displayed on the screen and view the demo (the red ones need to be replaced by demo software).

### 2.2 Sample Code and Technical Support

After booting up the board, you can run sample code or your own application on the development kit. You can download sample code and get technical support from the [Atmel web site](#).

Linux software and demos can be found on the web site [Linux4SAM](#).

## 3. Evaluation Kit Hardware

### 3.1 Introduction

The Atmel SAMA5D3 series evaluation kit is a fully-featured evaluation platform for Atmel SAMA5D3 series microcontrollers. The evaluation kit allows users to extensively evaluate, prototype and create application-specific designs.

The Atmel SAMA5D3 series evaluation kit is a platform architecture based on a main board, a computer module equipped with a SAMA5D3 series processor and an optional display module, providing maximum flexibility for kit users.

The SAMA5D3 series evaluation kit consists of three boards:

- The computer module (CM) board, is a single-board computer that integrates all the core components and is mounted onto an application-specific main board (MB). The computer module has specified pinouts based on the SODIMM200 connector. It provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, audio, mass storage, network and multiple serial and USB ports. A single SODIMM200 connector provides the main board interface to carry all the I/O signals to and from the computer module.
- The main board (MB) provides all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a densely-packed solution, which results in a more reliable product while simplifying system integration.
- The display module board (DM) integrates LCD, touchscreen and Qtouch<sup>®</sup> technology

**Table 3-1. Evaluation Kit Features**

Feature	SAMA5D31	SAMA5D33	SAMA5D34	SAMA5D35	SAMA5D36
CAN0			X	X	X
CAN1			X	X	X
GMAC		X	X	X	X
EMAC	X			X	X
HSMCI1	X	X	X	X	X
HSMCI2		X	X	X	X
LCDC	X	X	X		X
UART0	X			X	X
UART1	X			X	X
ISI	X	X	X	X	X
SHA	X	X	X	X	X
AES	X	X	X	X	X
TDES	X	X	X	X	X
TC1	X	X	X	X	X

## 4. CPU Module (CM) Board

### 4.1 Overview

The CPU module (CM) board is the heart of the SAMA5D3x-EK. It connects to the main board through a SODIMM200 interface and integrates the SAMA5D3 series processor and external memories. The CM board serves as a minimal CPU sub-system. All five SAMA5D31, SAMA5D33, SAMA5D34, SAMA5D35 and SAMA5D36 processors share the same CM board circuitry with minor configuration settings.

The CM board connects to a carrier board containing its connectors, power supply and any expansion I/O through a standard gold-plated SODIMM 200-pin connection.

Note: There are five CM boards from three different manufacturers. The five processors are implemented as shown in [Table 4-1](#).

**Table 4-1. CM Board Implementation**

Manufacturer and Module Kind	SAMA5D31-CM	SAMA5D33-CM	SAMA5D34-CM	SAMA5D35-CM	SAMA5D36-CM
Embest/Flextronics	X		X		X
Ronetix	X	X	X	X	

The five CM boards share the same circuitry design with different designator information and PCB layouts. The circuitry reference in this guide, for common design parts, refers to schematics from SAMA5D3 series-CM (mfg2). All the other schematics are provided in the [Section 4.4 “Embest/Flextronics Schematics”](#) and [Section 4.5 “Ronetix Schematics”](#).

Figure 4-1. CPU Module Board from Embest/Flextronics

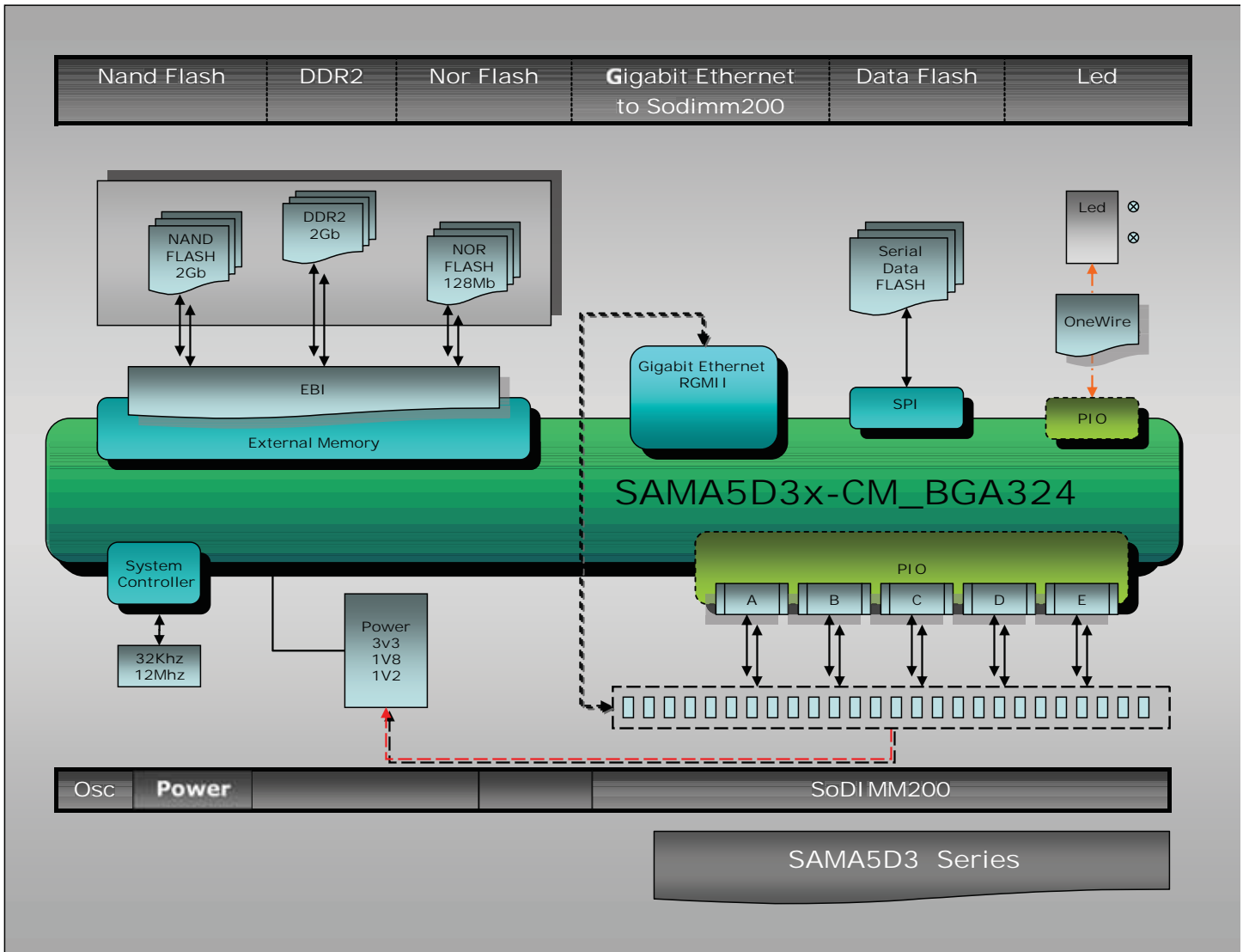


Figure 4-2. CPU Module Board from Ronetix





Figure 4-3. Board Architecture



Note: Different interfaces on the main board share the same connections to the CPU module. The actual usage depends on the CPU module featured in your evaluation kit.

## 4.2 Equipment List

The CM board is built around an ARM® Cortex®-A5-based microcontroller (BGA 324 package) with external memory and Gigabit Ethernet PHYsical layer transceiver.

### 4.2.1 Devices

Table 4-2. CPU Module Specifications

Characteristic	Specifications
PCB	CPU Module (10 layers)
Dimensions in mm: (L x W x H)	67.60 *(40 to 47) * 5 max
Processor	SAMA5D31, SAMA5D33, SAMA5D34, SAMA5D35 and SAMA5D36 (324-ball BGA package)
Clock speed	12 MHz crystal 32.768 kHz
Memory	2 x DDR2 2 Gb 16 Meg x 16 x 8 banks 1 x SLC NAND Flash 2/4Gb 8-bit data 1 x NOR 128 Mb 16-bit data
On-board I/O Ports	One Serial EEPROM SPI One 1-Wire EEPROM DS2431 One user-powered red LED and one user blue LED One gigabit Ethernet PHY
Connector	SODIMM200
Board supply voltage	3.3V from SODIMM200 connector On-board power regulation
Temperature: - operating - storage	0°C to +60°C -40°C to +85°C
Relative humidity	0 to 90% (non condensing)
RoHS status	Compliant
Board Identification	SAMA5D31-CM SAMA5D33-CM SAMA5D34-CM
Silkscreen top	SAMA5D35-CM SAMA5D36-CM

### 4.2.2 Interface Connection

- SODIMM200 card edge interface

### 4.2.3 Configuration Items

- One jumper for SPI DataFlash chip select connection

## 4.2.4 Boot Options

Table 4-3 lists the supported boot options

Table 4-3. Boot Options

Boot Mode	Boot Device	Type	Note
BMS OPEN	Embedded ROM Boot	ROM Boot followed by: - SPI0, NPCS0 - SD/MMC MCI0, MCI1 - NAND Flash - SPI0, NPCS1 - TWI0 - SAM-BA®	Default boot is from embedded ROM
BMS CLOSE	NOR Flash	On-board NOR Flash using NCS0	Boot from external NOR Flash memory

### 4.2.4.1 Boot Configuration

In order to use SAM-BA boot, the NAND Flash and SPI DataFlash must be deselected.

Pressing the pushbutton PB4 (CS boot disable) disconnects these two components from the system while the ROM Boot is searching for a boot device after reset. A reset can be forced by pressing the PB1 (NRST) pushbutton. Note that PB1 and PB4 pushbuttons are located on the main board (MB).

In order to boot from SAM-BA, both PB1 and PB4 should be pressed, then PB1 released while PB4 is kept pressed until SAM-BA boots.

## 4.3 Functional Blocks

### 4.3.1 Processor

The CM board is equipped with one Atmel SAMA5D3 ARM-based embedded MPU from the list below:

- SAMA5D31
- SAMA5D33
- SAMA5D34
- SAMA5D35
- SAMA5D36

The SAMA5D3x devices are packaged in a BGA324-ball BGA package and share an identical footprint.

.As different interfaces can be defined using the same pins, the functions available on the evaluation board depend on the actual configuration of the CPU.

The Atmel SAMA5D3 series is a high-performance, power-efficient embedded MPU based on the ARM Cortex-A5 processor, achieving 536 MHz with power consumption levels below 0.5 mW in low-power mode. The device features a floating point unit for high-precision computing and accelerated data processing, and a high data bandwidth architecture. It integrates advanced user interface and connectivity peripherals and security features.

The SAMA5D3 series features an internal multi-layer bus architecture associated with 39 DMA channels to sustain the high bandwidth required by the processor and the high-speed peripherals. The device offers support for DDR2/LPDDR/LPDDR2 and MLC NAND Flash memory with 24-bit ECC.

The comprehensive peripheral set includes an LCD controller with overlays for hardware-accelerated image composition, a touchscreen interface and a CMOS sensor interface. Connectivity peripherals include Gigabit EMAC with IEEE1588, 10/100 EMAC, multiple CAN, UART, SPI and I2C. With its secure boot mechanism, hardware accelerated engines for encryption (AES, TDES) and hash function (SHA), the SAMA5D3 ensures anti-cloning, code protection and secure external data transfers.

Refer to [Section 4. “CPU Module \(CM\) Board” on page 7](#) for details.

The processor runs at frequencies up to 536 MHz for the core and up to 166 MHz for the system bus.

### 4.3.2 Clock Circuitry

The CM board includes three clock sources:

- Two clocks are alternatives for the SAMA5D3 series processor main clock
- One crystal oscillator is used for the Ethernet RGMII chip

**Table 4-4. Main Components Associated with the Clock Systems**

Quantity	Description	Component Assignment
1	Crystal for internal clock, 12 MHz	Y1
1	Crystal for RTC clock, 32.768 kHz	Y2
1	Oscillator for ethernet clock RGMII, 25 MHz	Y3

### 4.3.3 Reset Circuitry

The reset sources for the CM board are:

- Power-on reset
- Pushbutton reset (Pushbutton is equipped on main board)
- JTAG reset from an in-circuit emulator (MB features an on-board JTAG interface)

#### 4.3.4 Power Supplies

The CM board is driven by +3.3V input power rail from the MB through the SODIMM200 connector. The CM board embeds all necessary power rails required for the microprocessor.

When additional voltages are required, they are generated on-board from the 3.3V supply (power source is a linear regulator or a switching regulator). The detailed power supply requirements for given modules are specified within the corresponding product documentation.

Table 4-5 summarizes the power specifications.

**Table 4-5. Supply Group Configuration**

Nominal	Name	Powers	Component
3.0V	VDDBU	the Slow Clock oscillator, the internal 32K RC, the internal 12M RC and a part of the System Controller	From VBAT 3V, SODIMM200 connector
3.3V	VDDIOP0	a part of peripheral I/O lines	From main 3.3V, SODIMM200 connector
3.3V	VDDIOP1	a part of peripheral I/O lines	From main 3.3V, SODIMM200 connector
3.3V	VDDUTMII	the USB device and host UTMI + interface	From main 3.3V, SODIMM200 connector
3.3V	VDDOSC	the main oscillator cells	From main 3.3V, SODIMM200 connector
3.3V	VDDANA	the analog-to-digital converter	From main 3.3V, SODIMM200 connector
1.2V	VDDCORE	the core, including the processor, the embedded memories and the peripherals	Regulator on-board
1.2V	VDDUTMIC	the USB device and host UTMI + core	Regulator on-board
1.2V	VDDPLLA	the PLLA cell	Regulator on-board
1.8V	VDDIODDR	DDR2 interface I/O lines	Regulator on-board
1.8V	VDDIOM	NAND, NOR Flash and SMC interface I/O lines	Regulator on-board
3.0V to 3.3V	ADVREF	ADC reference voltage	From ADVREF, SODIMM200 connector
2.5V	VDDFUSE	Fuse box for programming	Regulator on-board

Figure 4-4. Embest/Flextronics Power Supply

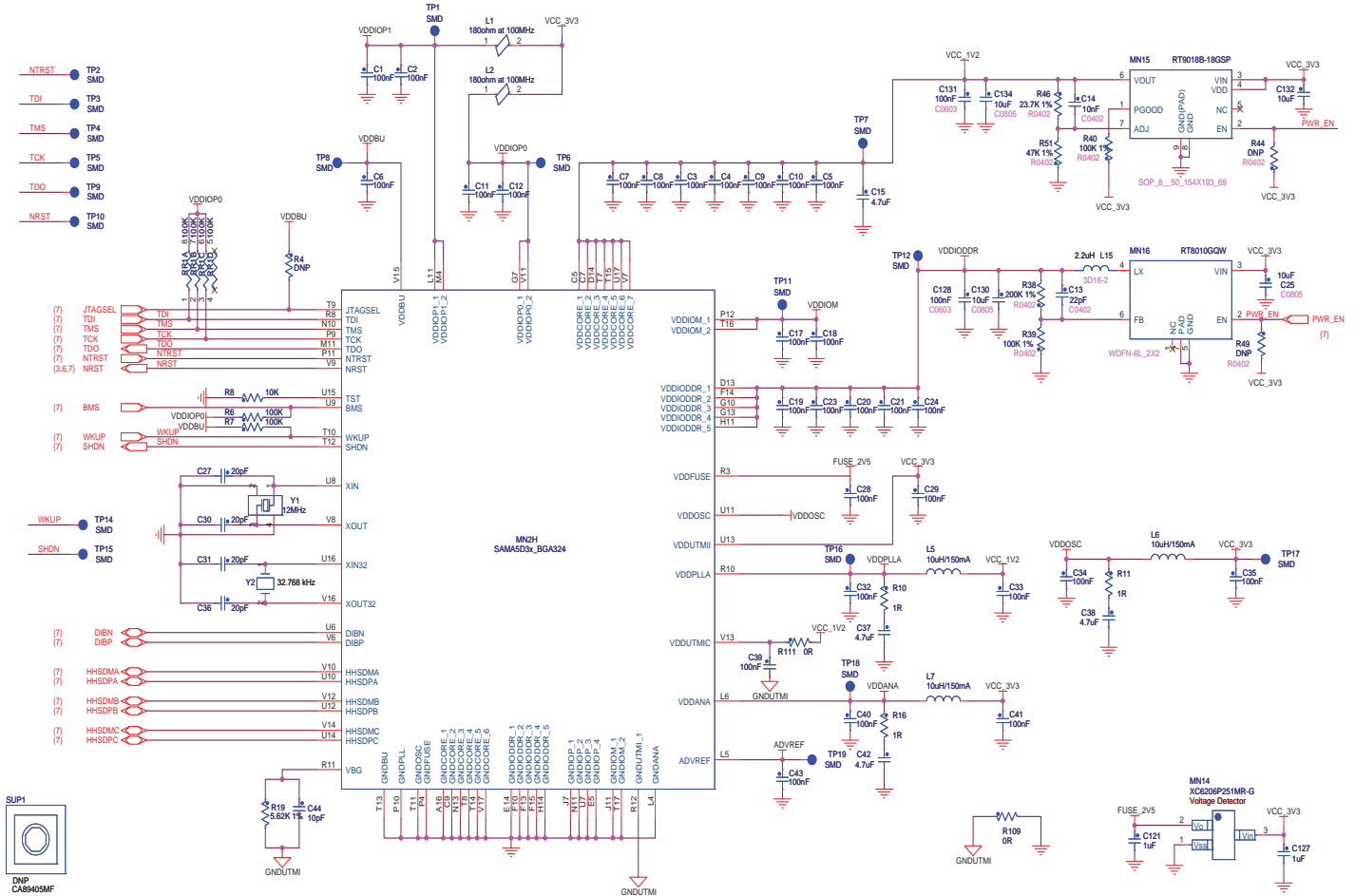


Figure 4-5. Ronetix Power Supply

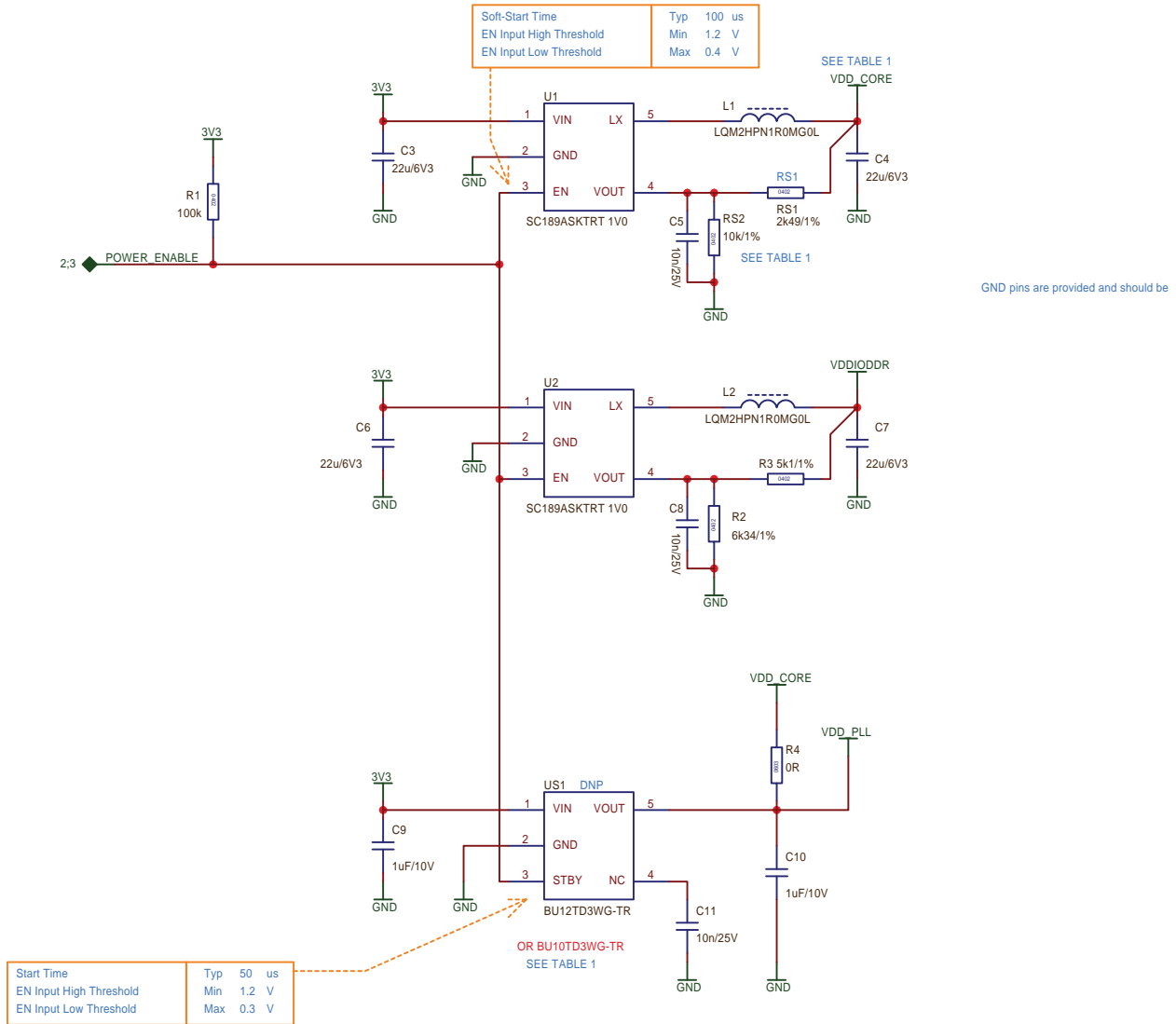
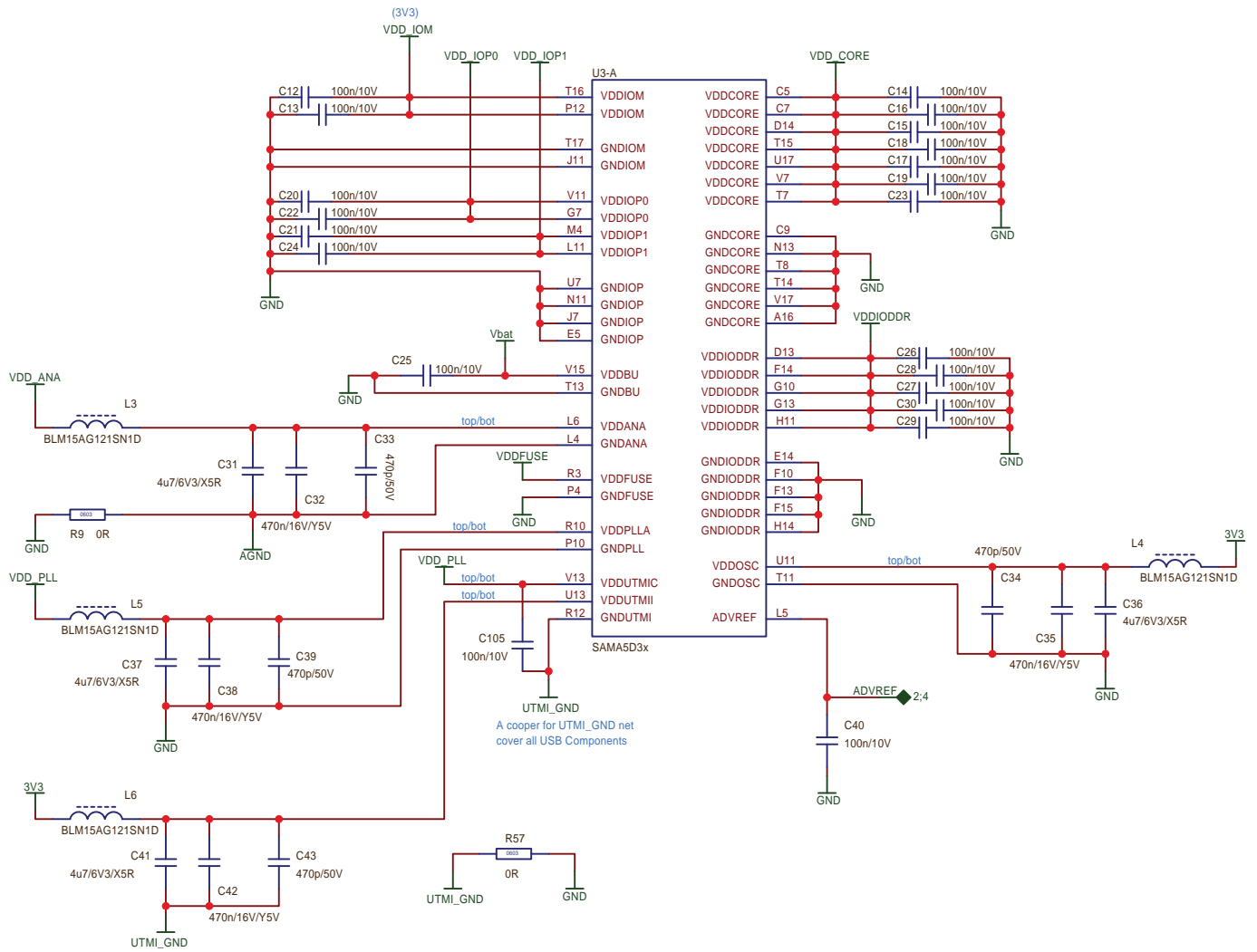


Figure 4-6. Ronetix Power Supply (Continued)





## 4.3.5 Memory

### 4.3.5.1 Memory Organization

The SAMA5D3 series processor features a DDR/SDR memory interface and an External Bus Interface (EBI) to interface to a wide range of external memories and to almost any kind of parallel peripheral.

### 4.3.5.2 Resource Allocation

This section describes the memory devices that equip the SAMA5D3 series CM board.

- Two SDRAM/DDR2 are used as main system memory. MT47H128M16 - 2 Gb - 16 Meg x 16 x 8 banks, the board provides up to 2 Gb of on-board, soldered DDR2 SDRAM. The memory bus is 32 bits wide and operates at up to 166 MHz.

Figure 4-7. Embest/Flextronics DDR2 Memory

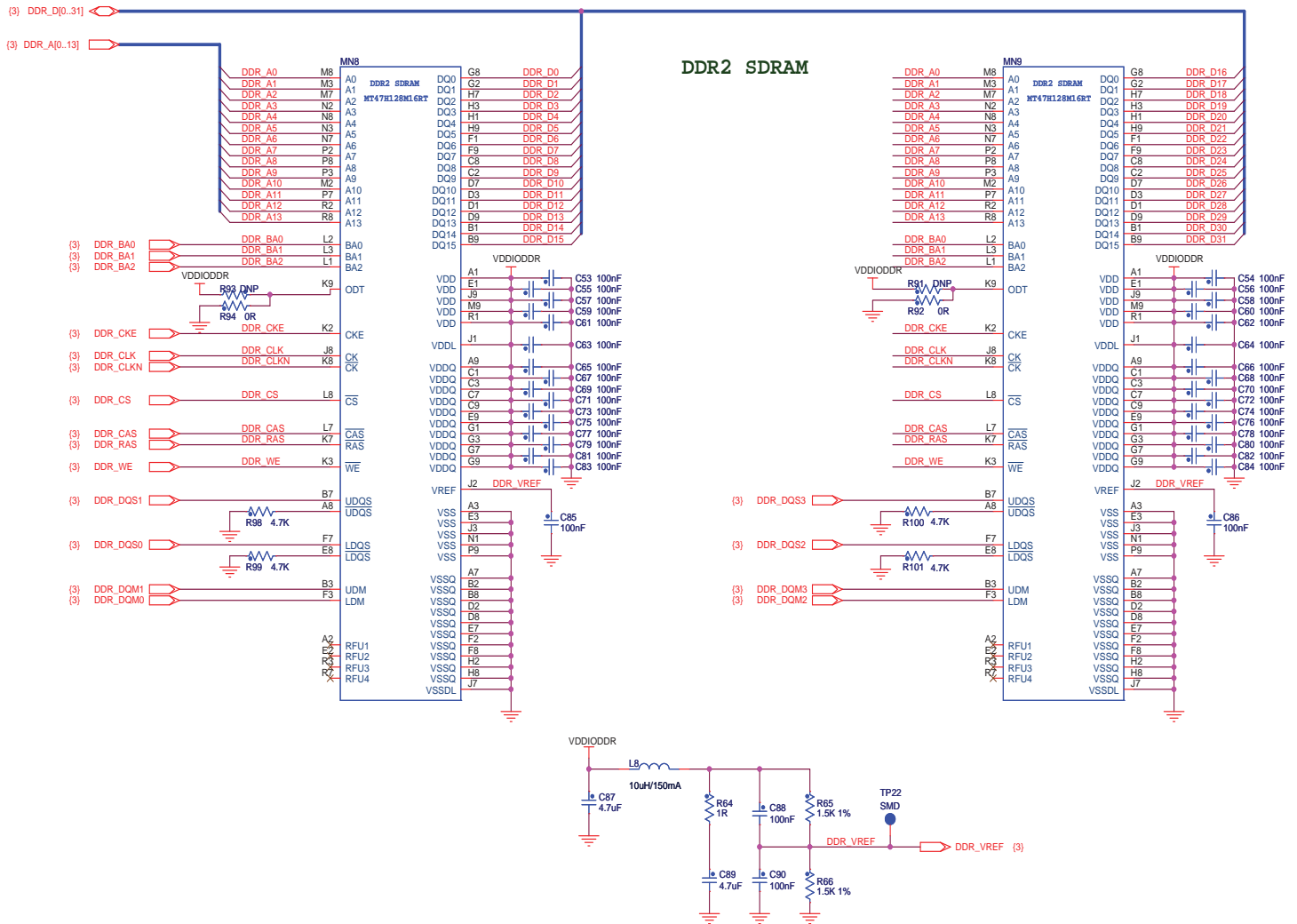
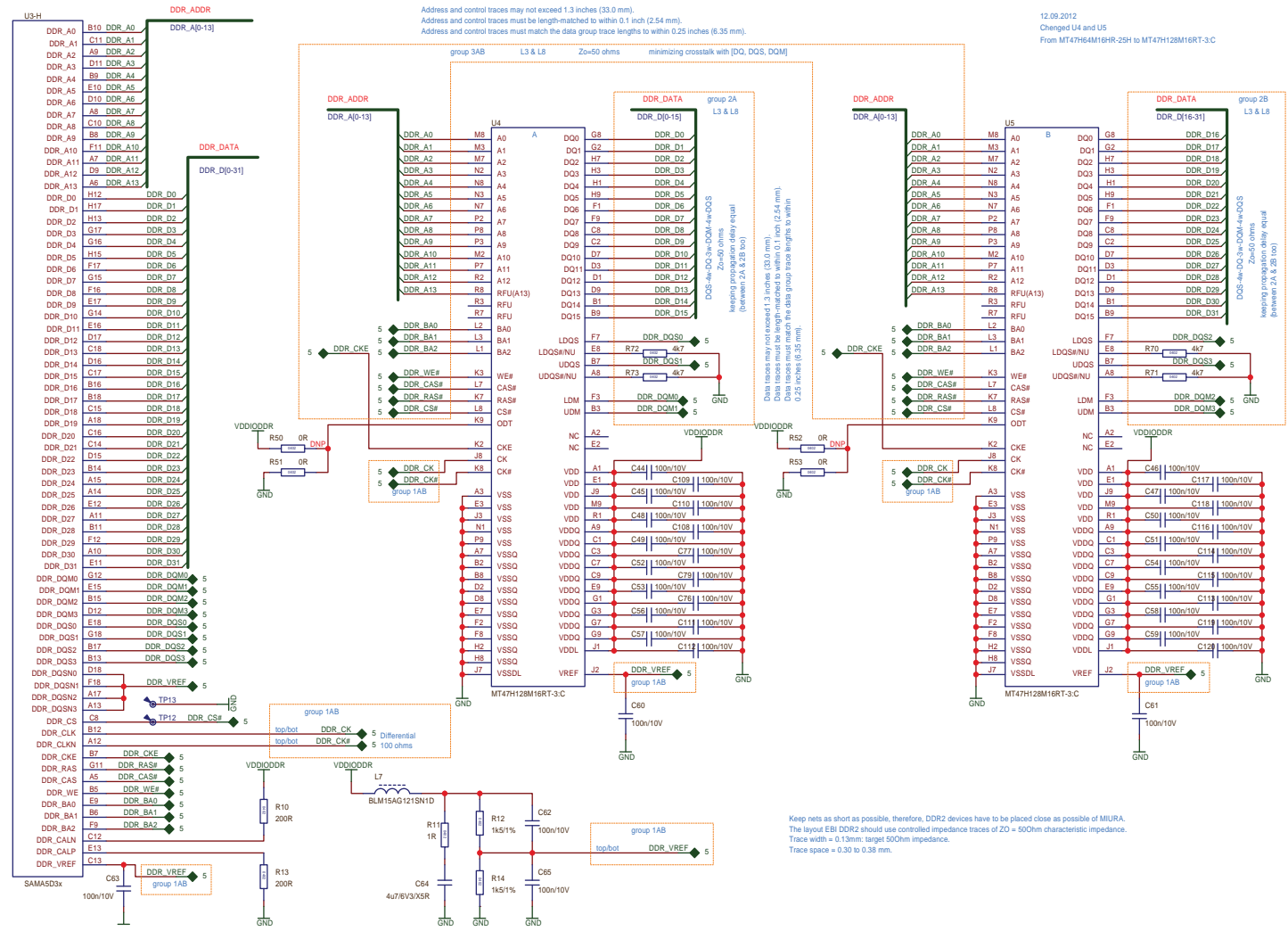


Figure 4-8. Ronetix DDR2 Memory



- One NAND Flash: NAND is connected to the processor. Maximum size is 256 bytes.
- One NOR Flash (optional, not populated): NOR Flash is 16 bits wide. Maximum size is 128 Mbytes.

Figure 4-9. Embest/Flextronics External Memory

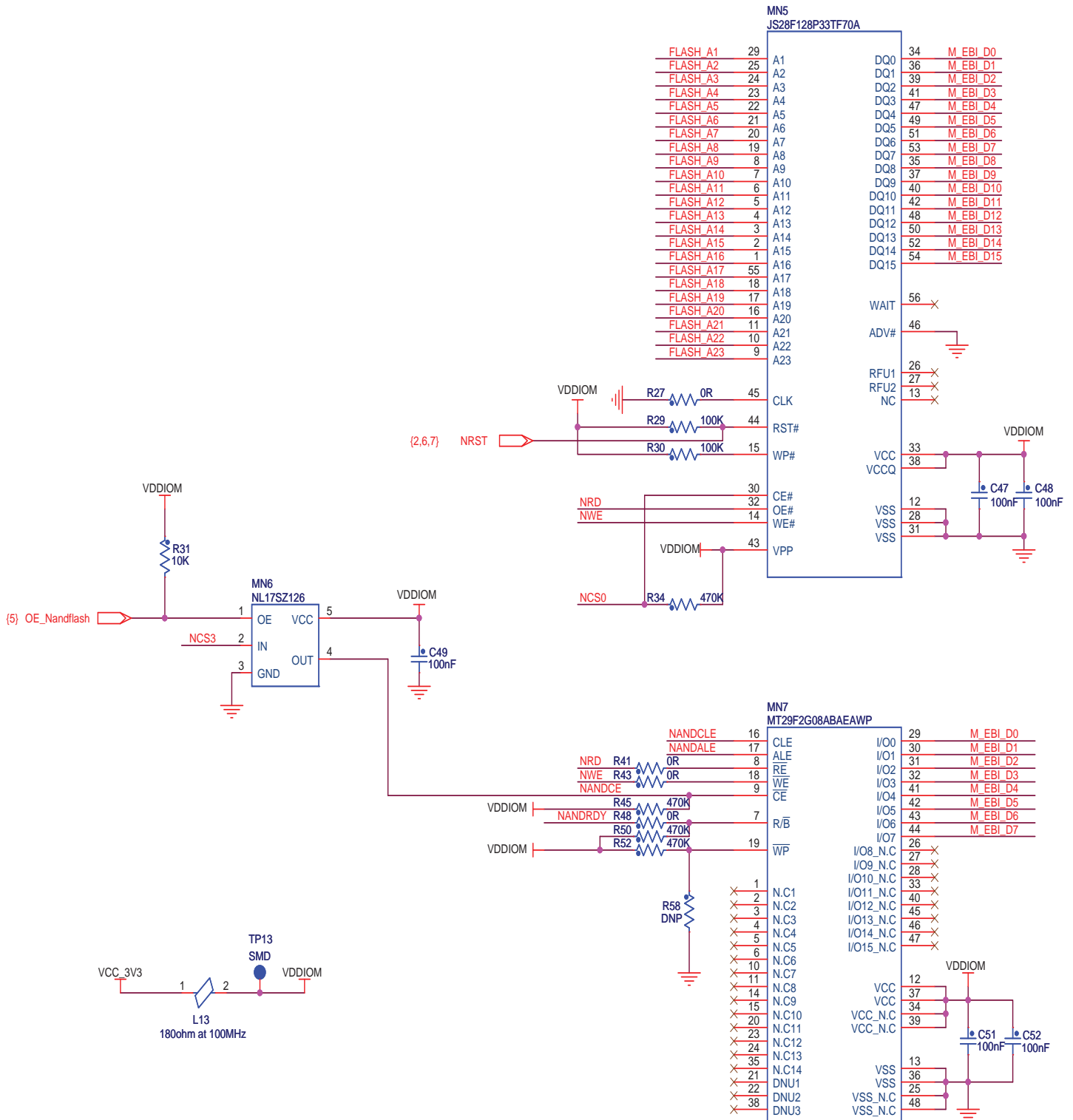
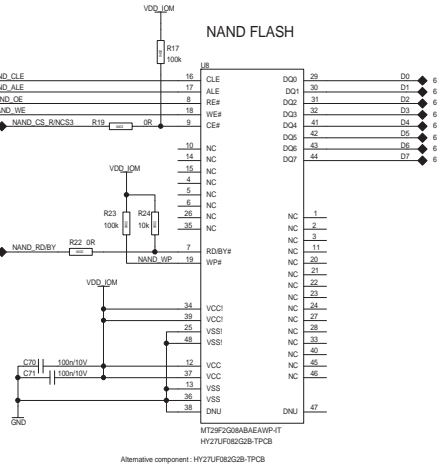
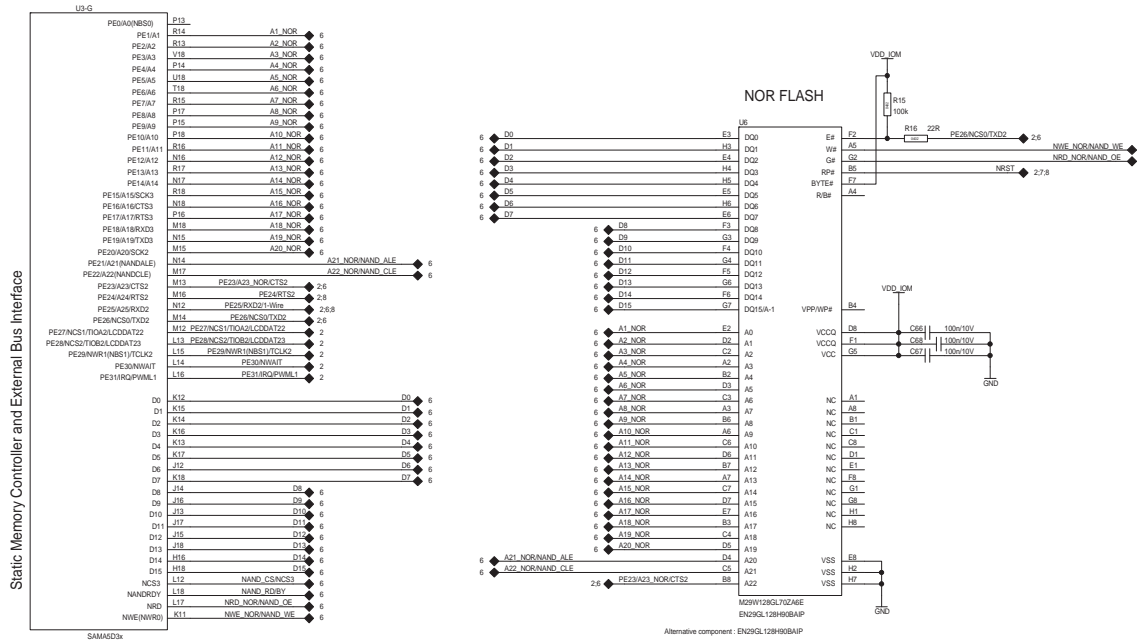


Figure 4-10. Ronetix External Memory



### 4.3.6 Serial Peripheral Interface Controller (SPI)

The SAMA5D3 series processor provides two high-speed Serial Peripheral Interface (SPI) controllers. One port is used to interface with the on-board serial DataFlash. Note that the on-board serial DataFlash is enabled through a jumper: JP1 on Embest modules, J1 on Ronetix modules. The jumper must be in place access (and boot) the serial DataFlash.

Figure 4-11. Embest/Flextronics Serial DataFlash on SPI

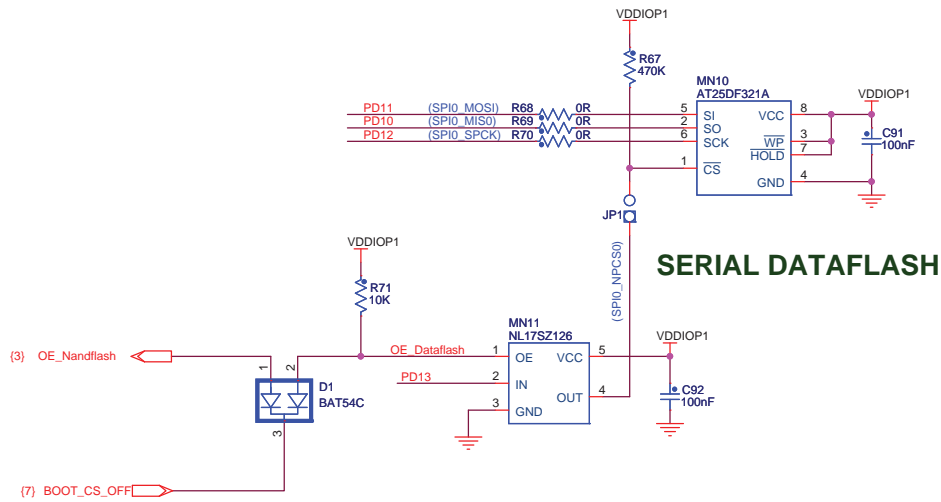
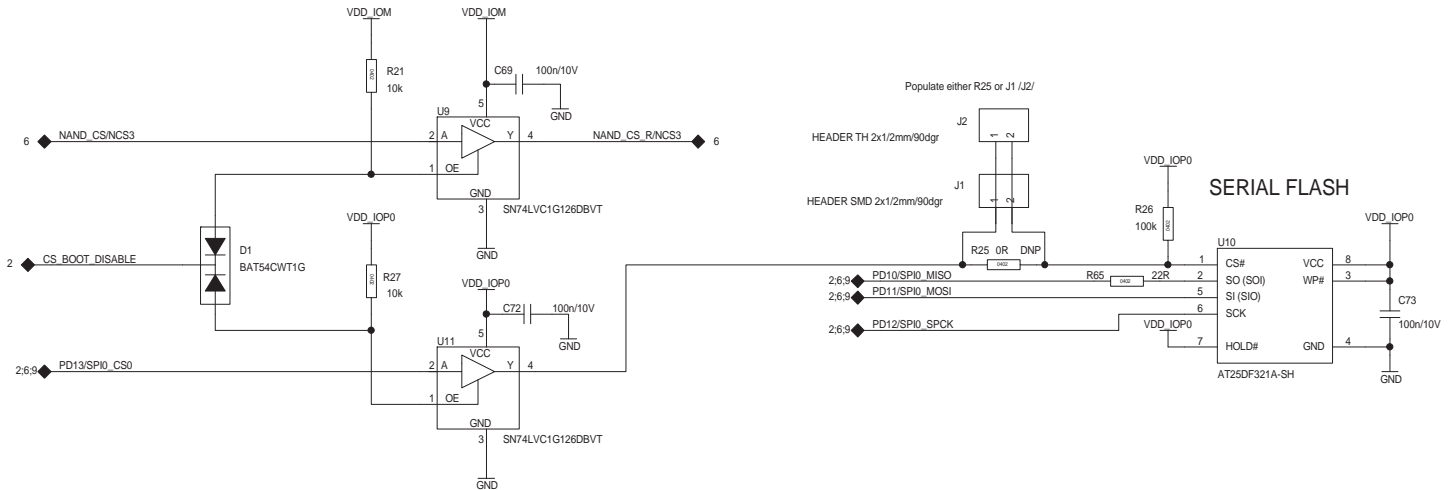


Figure 4-12. Ronetix Serial DataFlash on SPI



### 4.3.7 1-Wire EEPROM

The SAMA5D3 series CM board uses a 1-wire device as a “soft label” to store information such as chip type, manufacture name, production date, etc.

Only page 1 is used.

**Warning:** Do not modify the information contained in this page.

Pages 2 to n remain free for the user.

Figure 4-13. Embest 1-Wire EEPROM

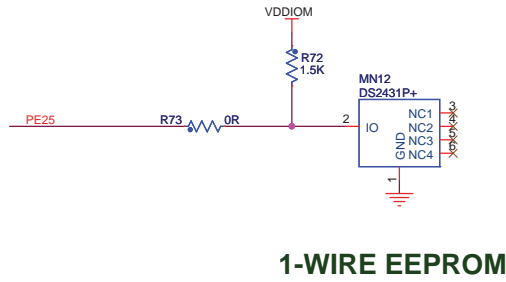
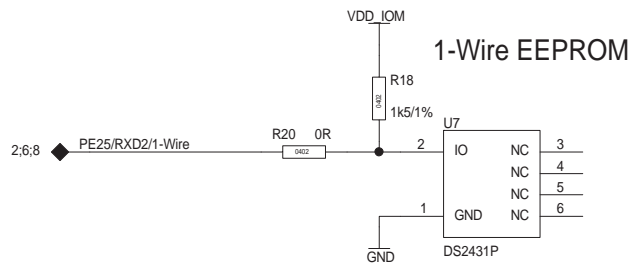


Figure 4-14. Ronetix 1-Wire EEPROM

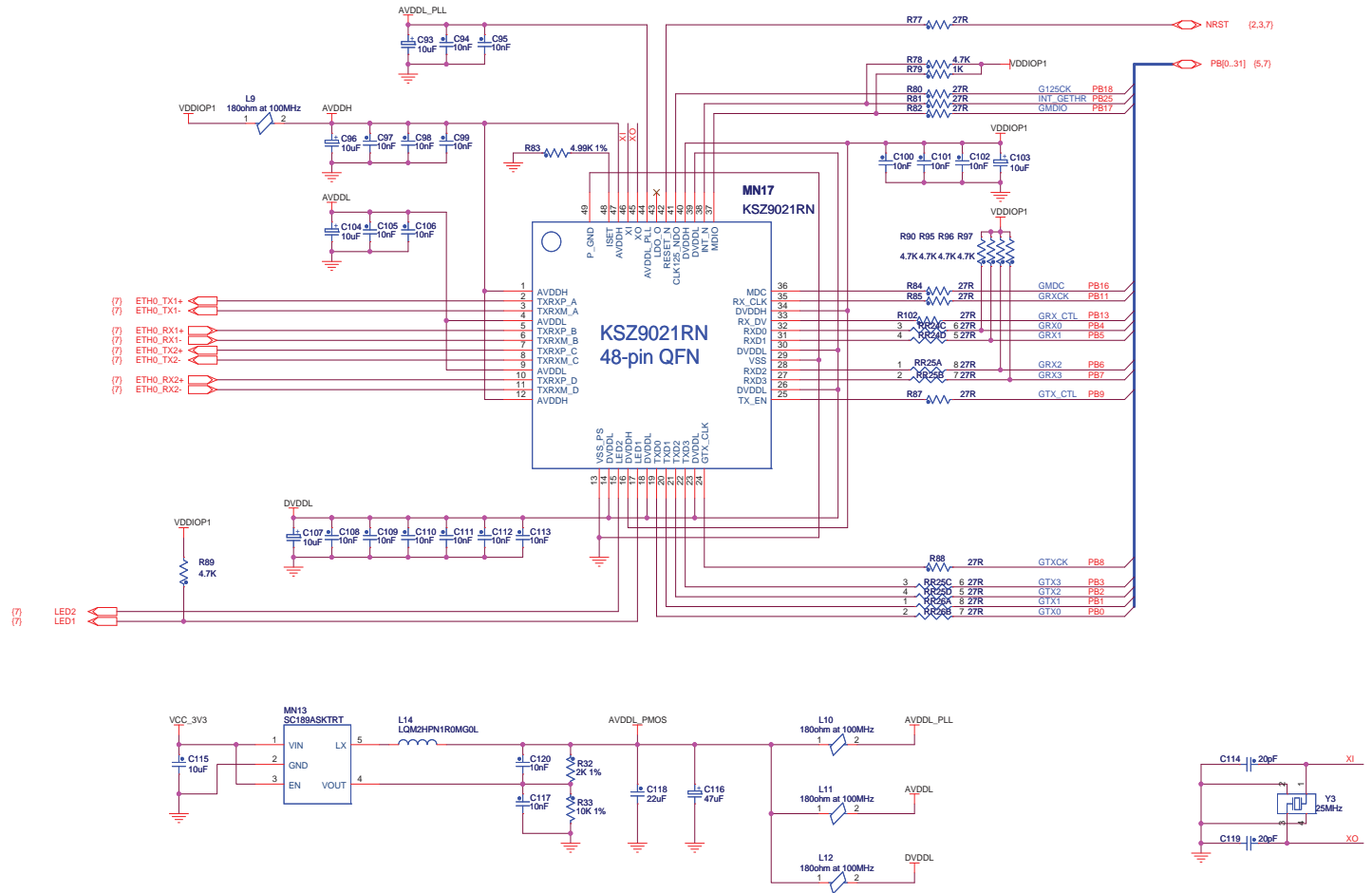


### 4.3.8 Tri-Speed Ethernet PHY

The SAMA5D3 series CM board is equipped with a MICREL PHY device (MICREL KSZ9021/31) operating at 10/100/1000 Mbps. The board supports the RGMII interface mode. The Ethernet interface consists of four pairs of low-voltage differential pair signals designated from GRX± and GTx± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 Base-T RJ45 connector integrated on the main board.

For more information about the Ethernet controller device, refer to the MICREL KSZ89021RN controller manufacturer's datasheet.

Figure 4-15. Embest/Flextronics GEthernet ETH0







### 4.3.9 Indicators

There are two LEDs on the SAMA5D3 series CM board that can be controlled by the user. Both are controlled by GPIO lines PE24 and PE25 as shown below.

Figure 4-17. Embest/Flextronics LED Indicators

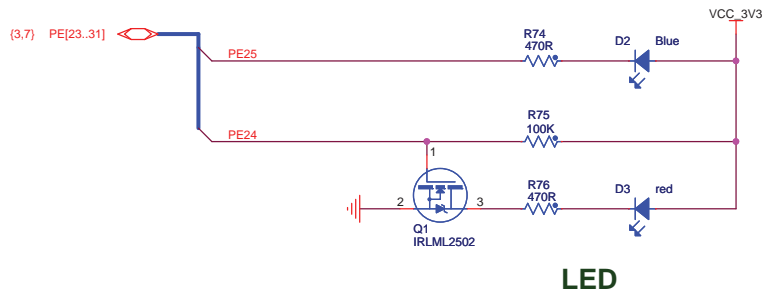
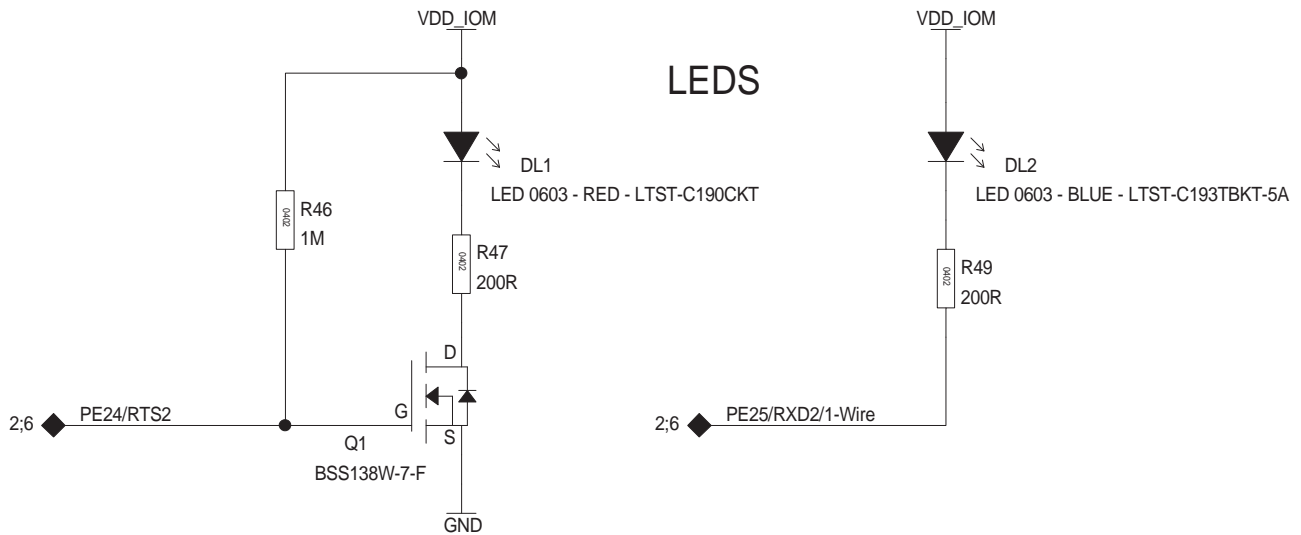


Figure 4-18. Ronetix LED Indicators



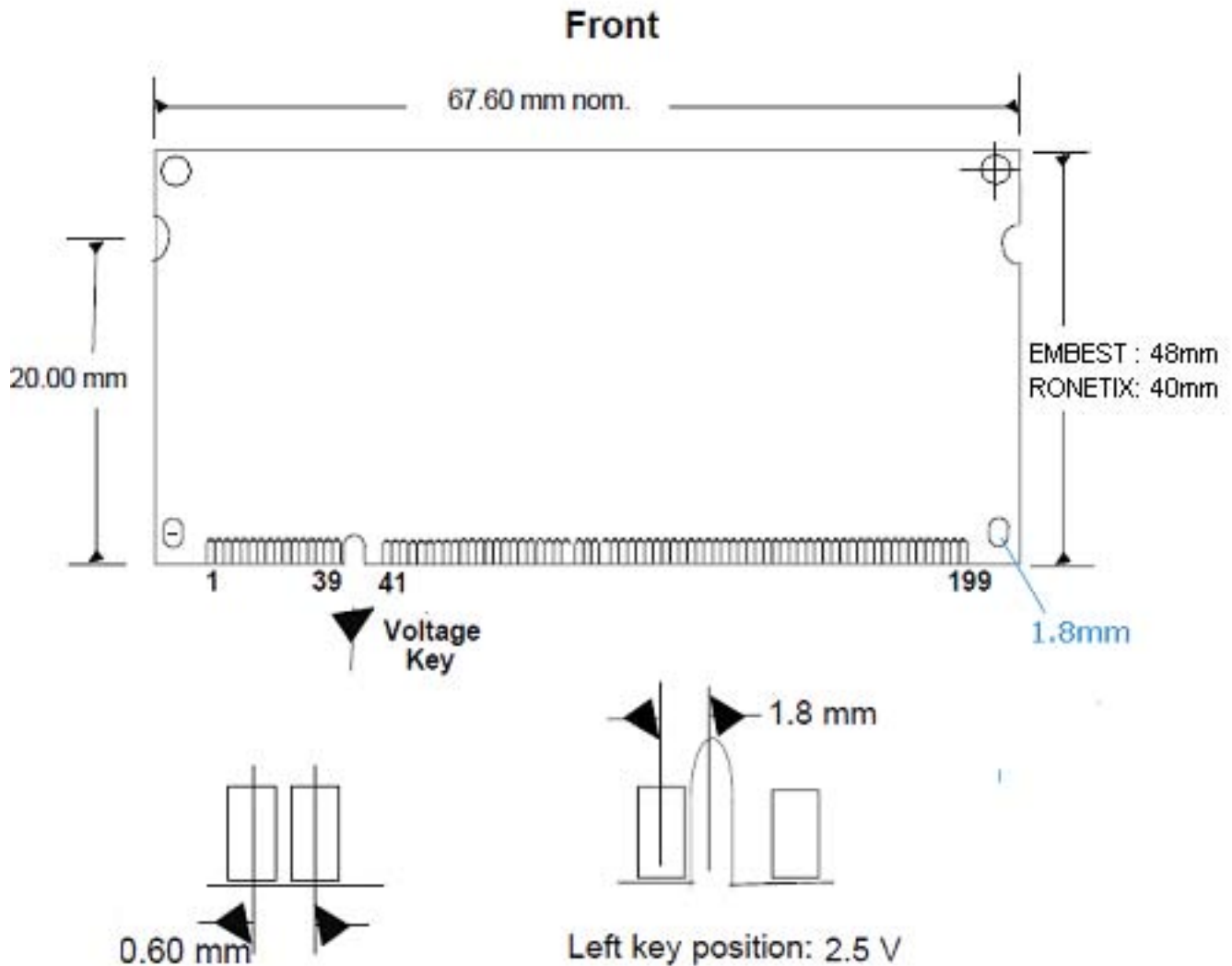
### 4.3.10 SODIMM200 Interface

The SAMA5D3 series CM board uses SODIMM200 card edge connector to interface with the MB board. Refer to [Section 5.4.22 “SODIMM Card Edge Socket”](#).

### 4.3.11 Connectors

[Figure 4-19](#) shows the mechanical dimensions of the SAMA5D3 series CM board outline and the mounting holes.

Figure 4-19. CPU Module Board Dimensions



Holes for mounting screws on carrier board.

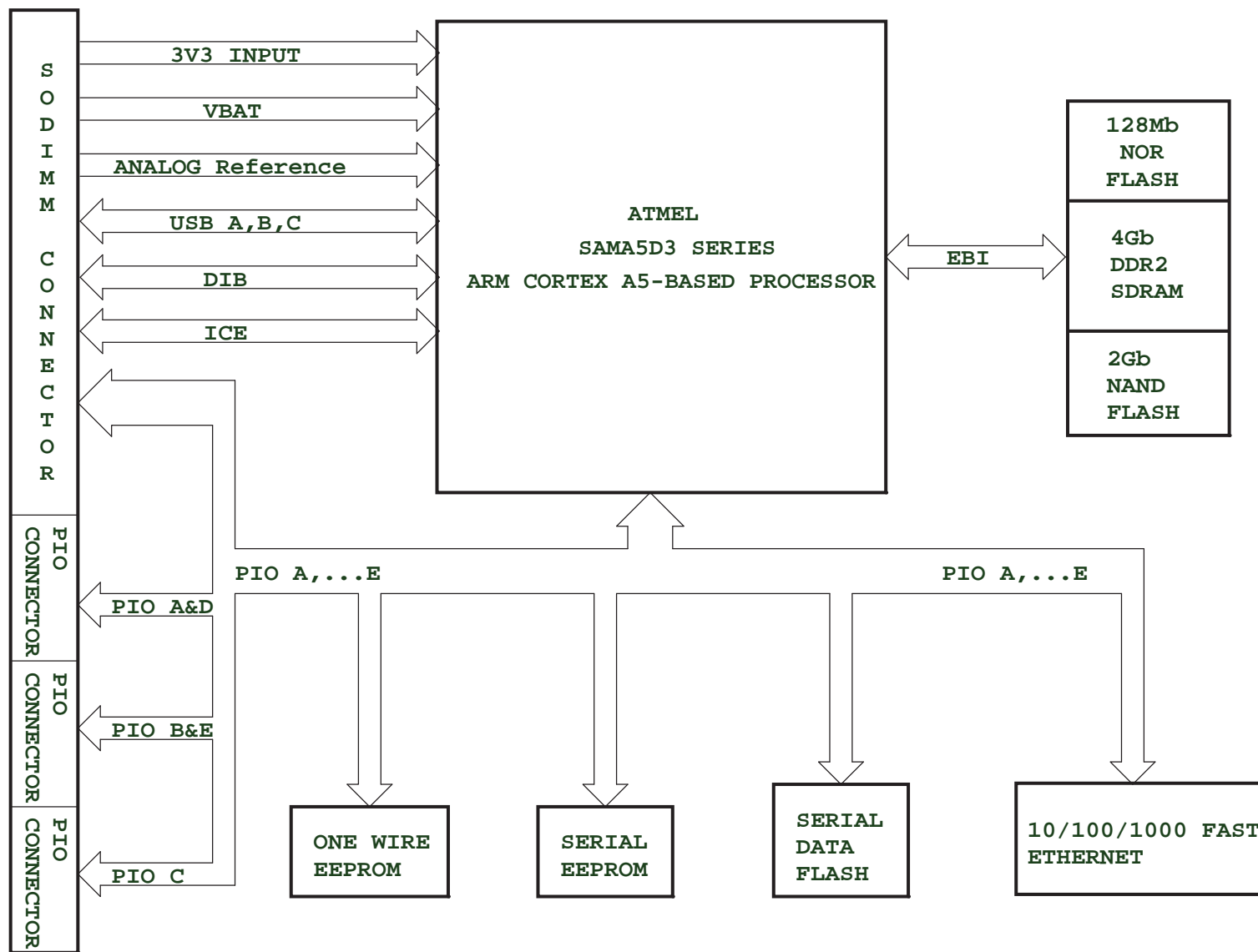
## 4.4 Embest/Flextronics Schematics

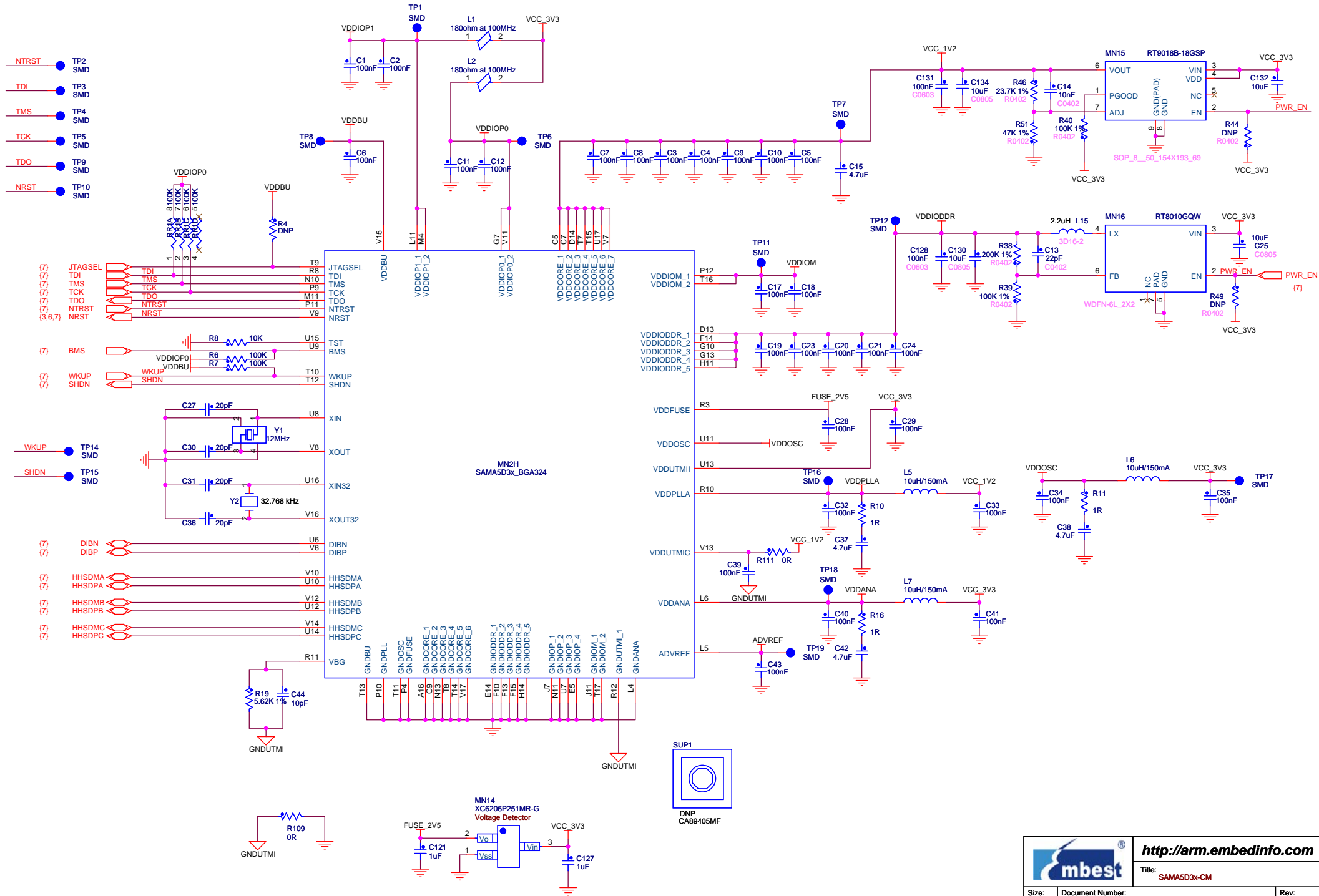
This SAMA5D3x-EK CM board manufactured by Embest/Flextronics is available in Revision D and Revision E. In this section, schematics are provided for both revisions.

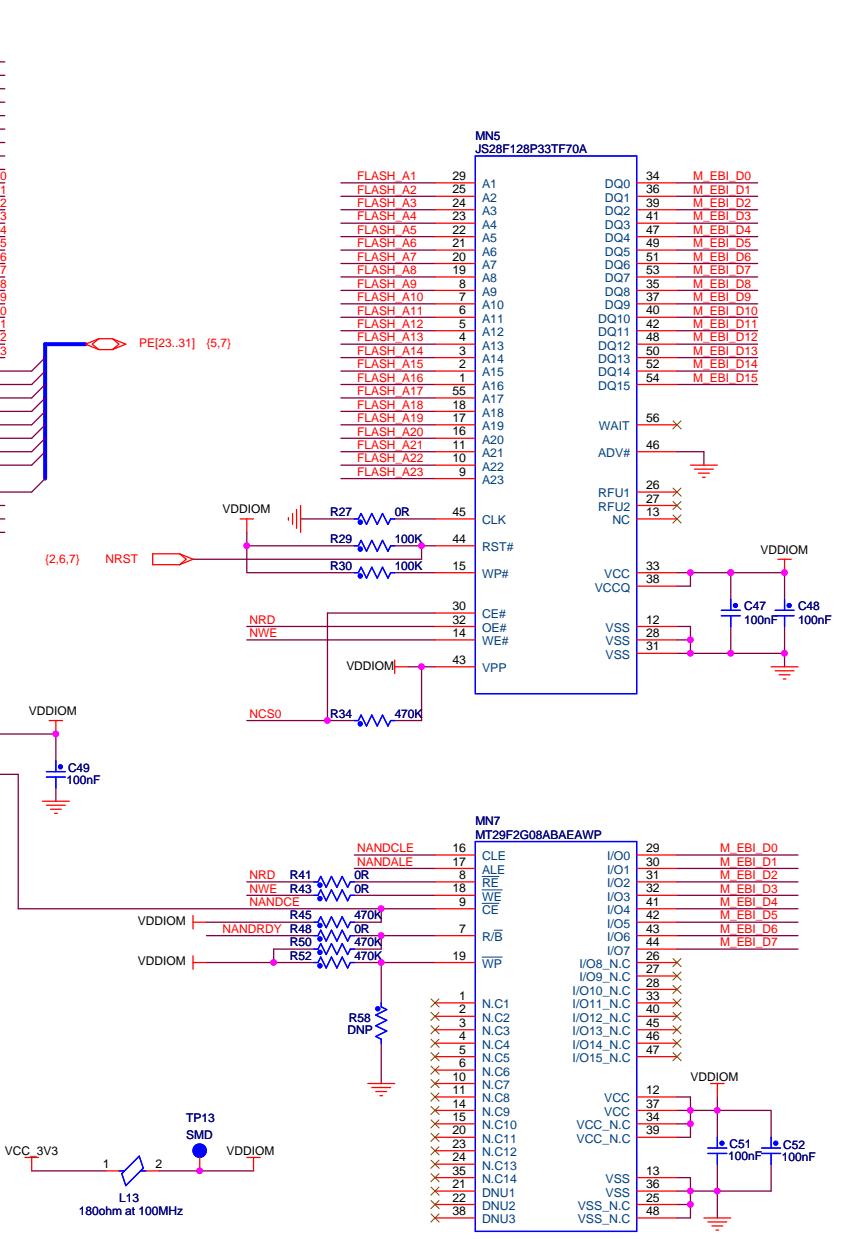
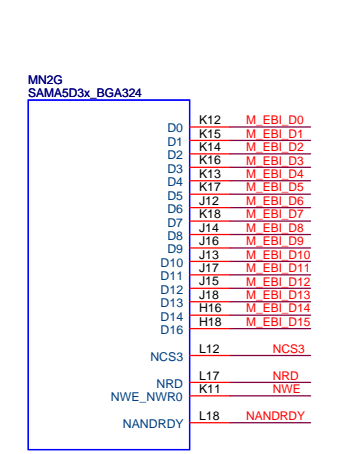
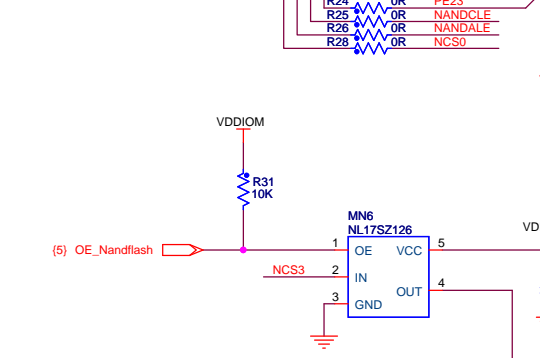
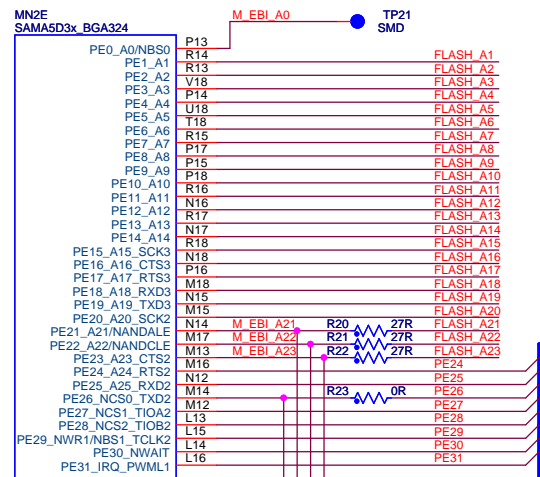
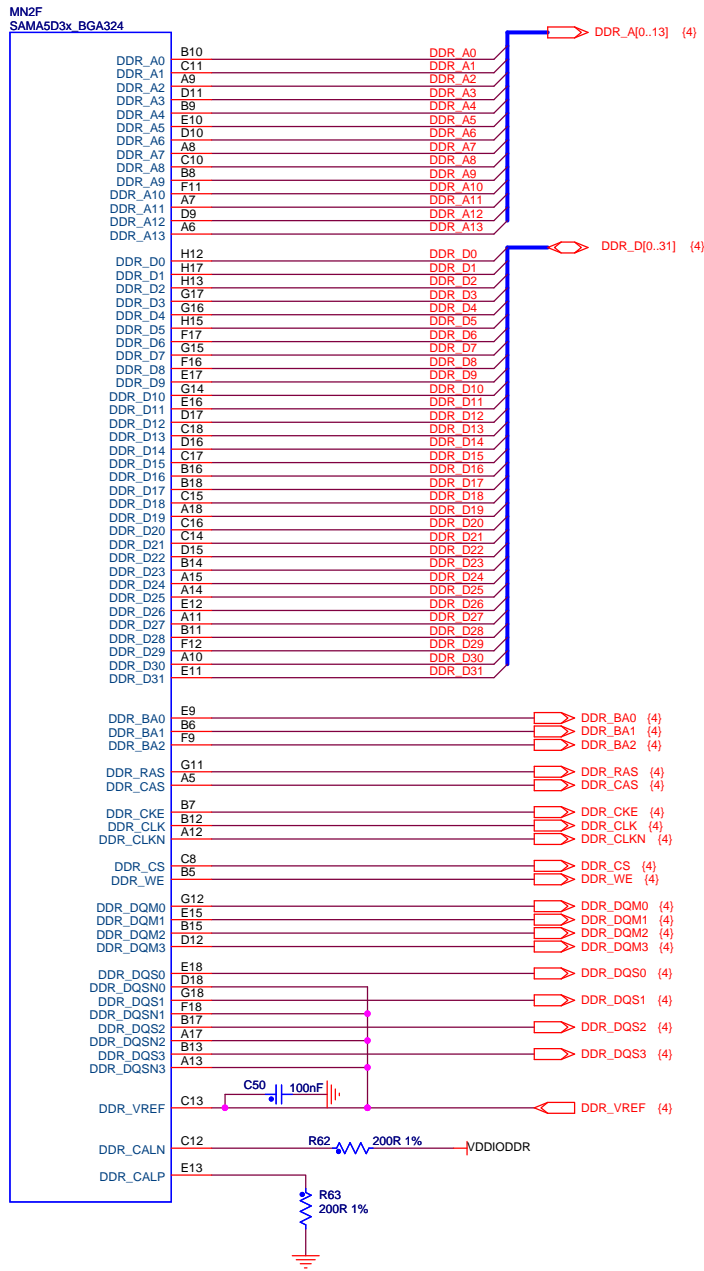
### 4.4.1 CPU Module Revision D Schematics

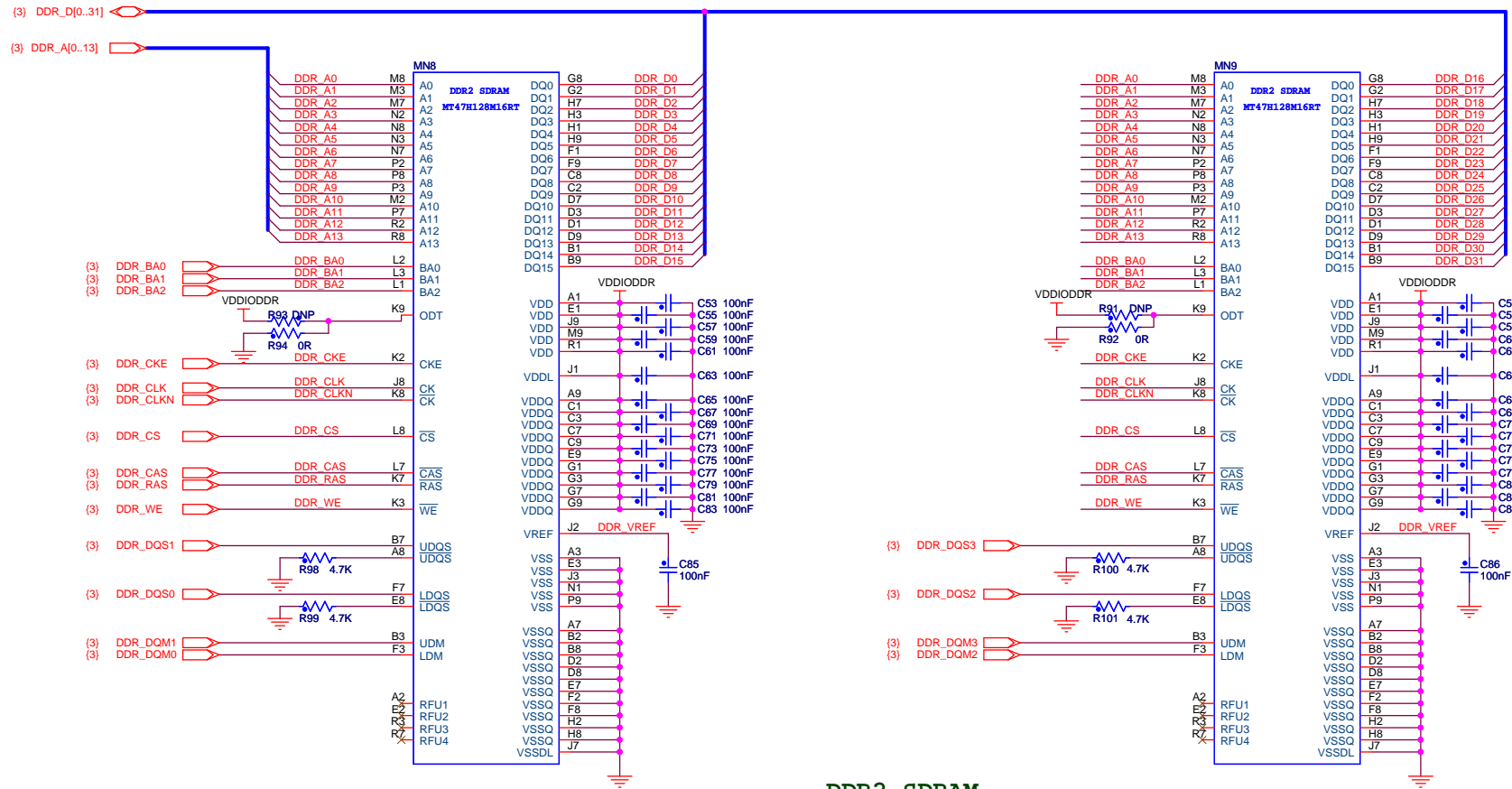
This section contains the following schematics:

- Block diagram
- SAMA5D3x power
- SAMA5D3x NOR and NAND
- 4 Gb DDR2
- SAMA5D3x DataFlash, 1-wire, LED
- Ethernet
- 200-pin SODIMM

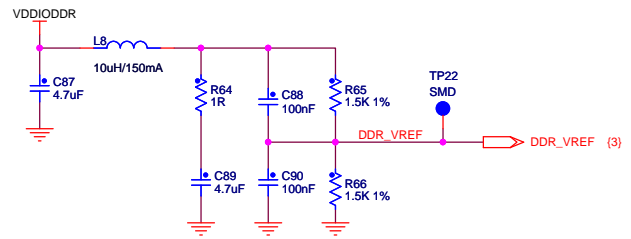







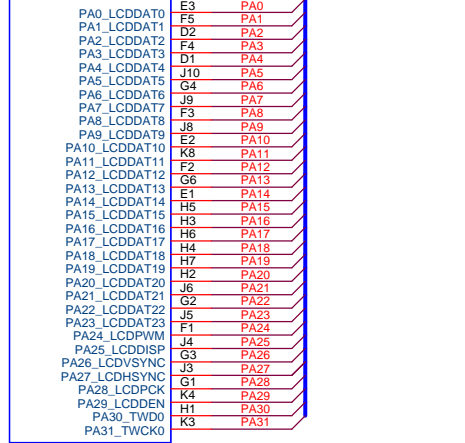


**DDR2 SDRAM**

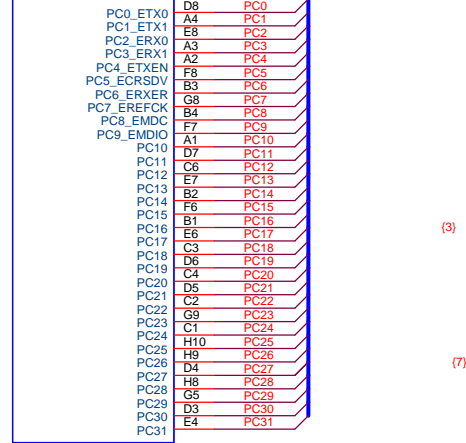


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Size: A3	Document Number: 4Gb DDR2	Rev: D	
Draw By: Zhu Xueliang	Date: Wednesday, September 19, 2012	Sheet: 4 of 7	

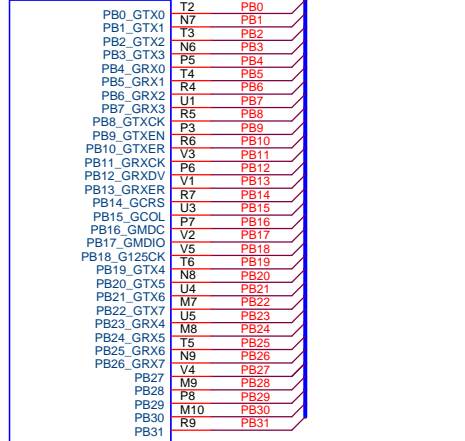
MN2A  
SAMASD3x BGA324



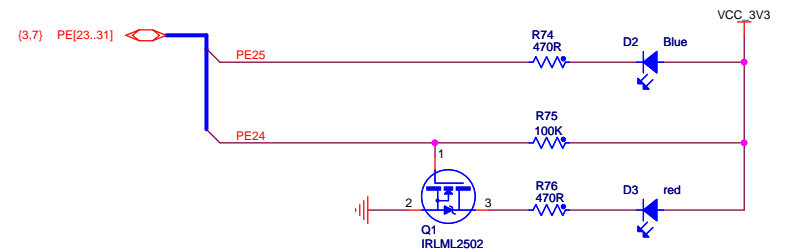
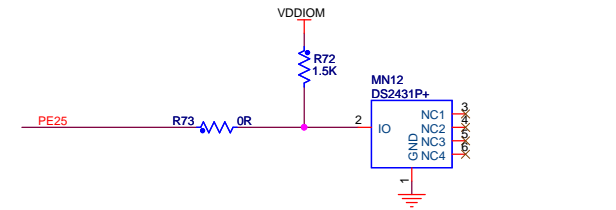
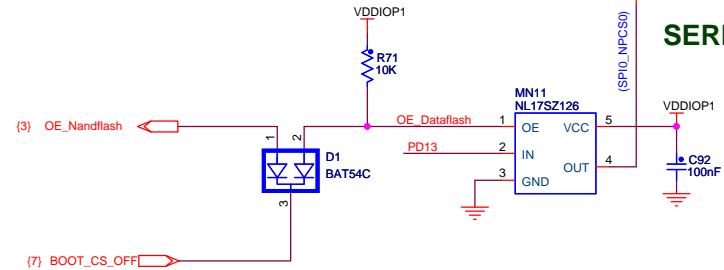
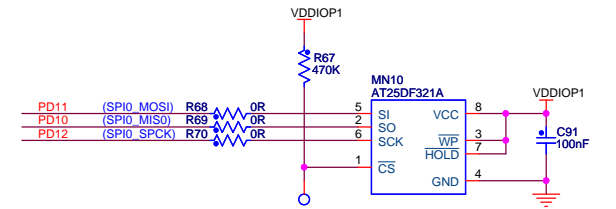
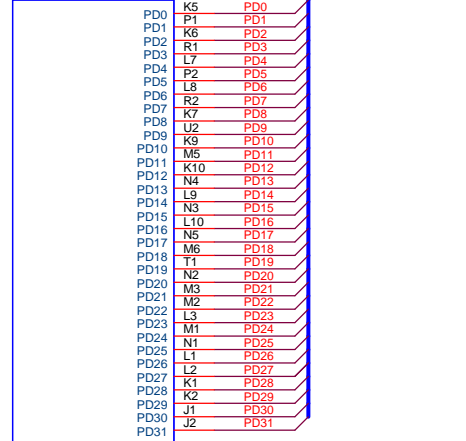
MN2C  
SAMASD3x BGA324



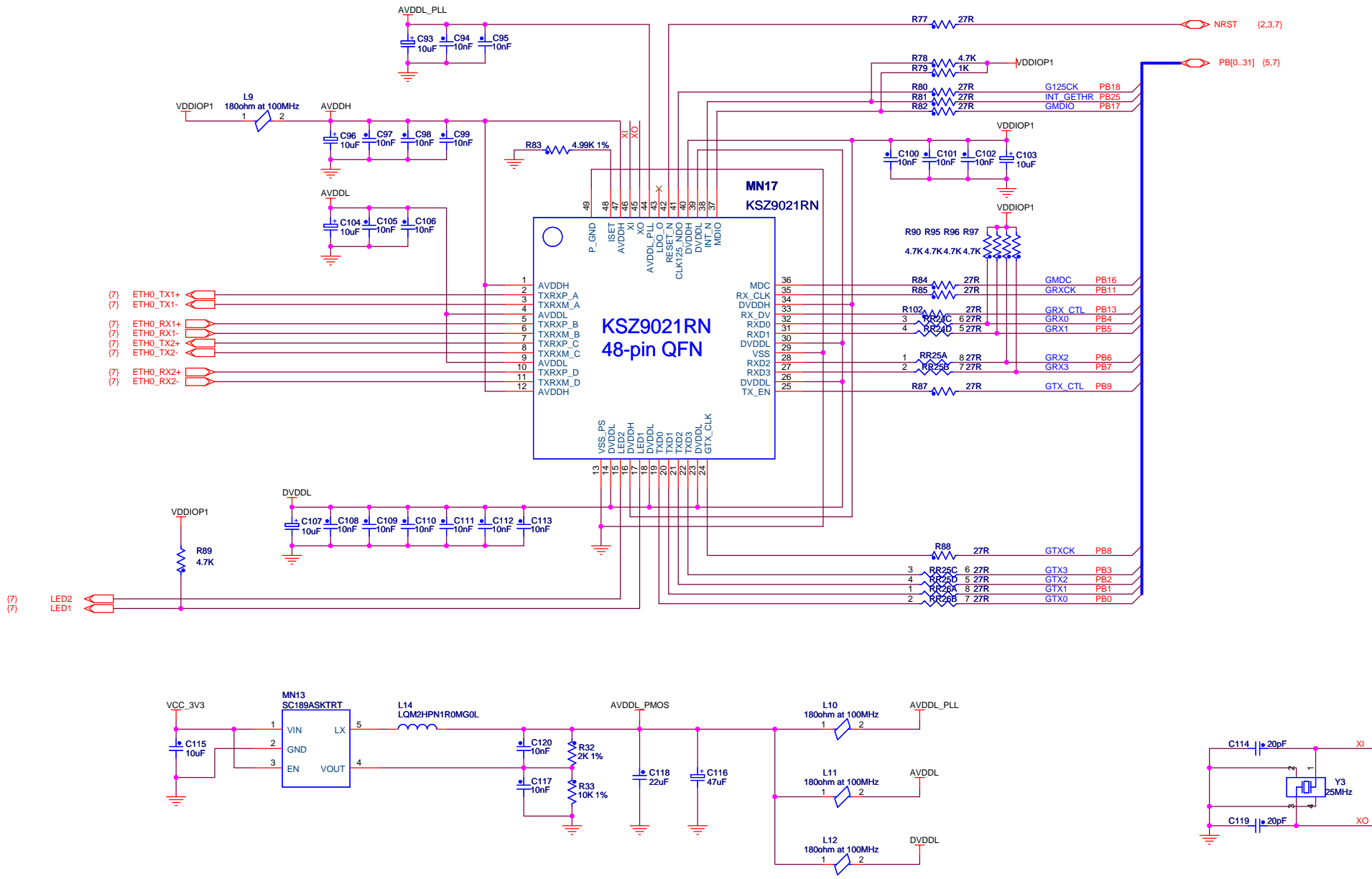
MN2B  
SAMASD3x BGA324



MN2D  
SAMASD3x BGA324



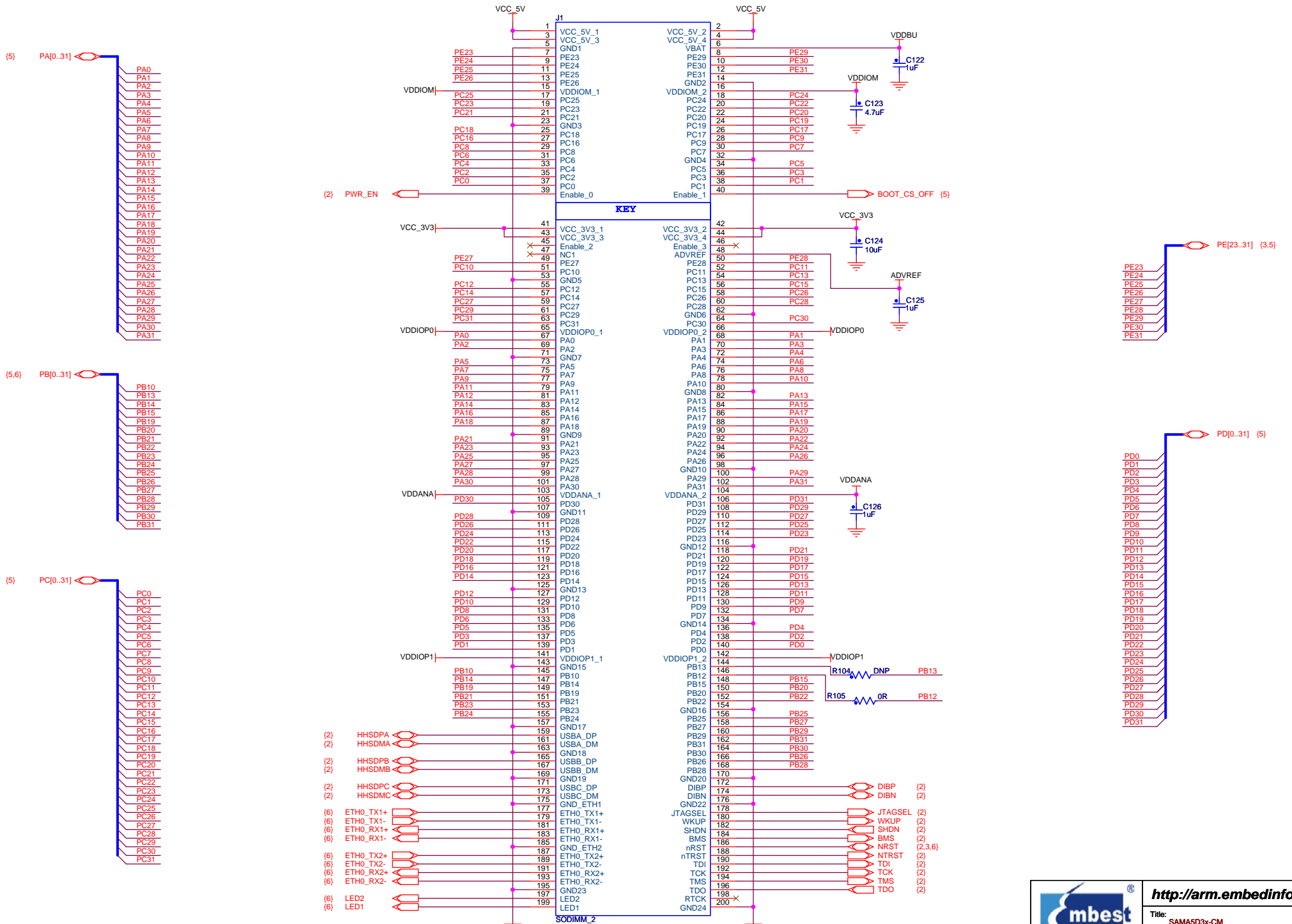




(7) ETH0\_TX1+  
(7) ETH0\_TX1-  
(7) ETH0\_RX1+  
(7) ETH0\_RX1-  
(7) ETH0\_TX2+  
(7) ETH0\_TX2-  
(7) ETH0\_RX2+  
(7) ETH0\_RX2-

(7) LED2  
(7) LED1

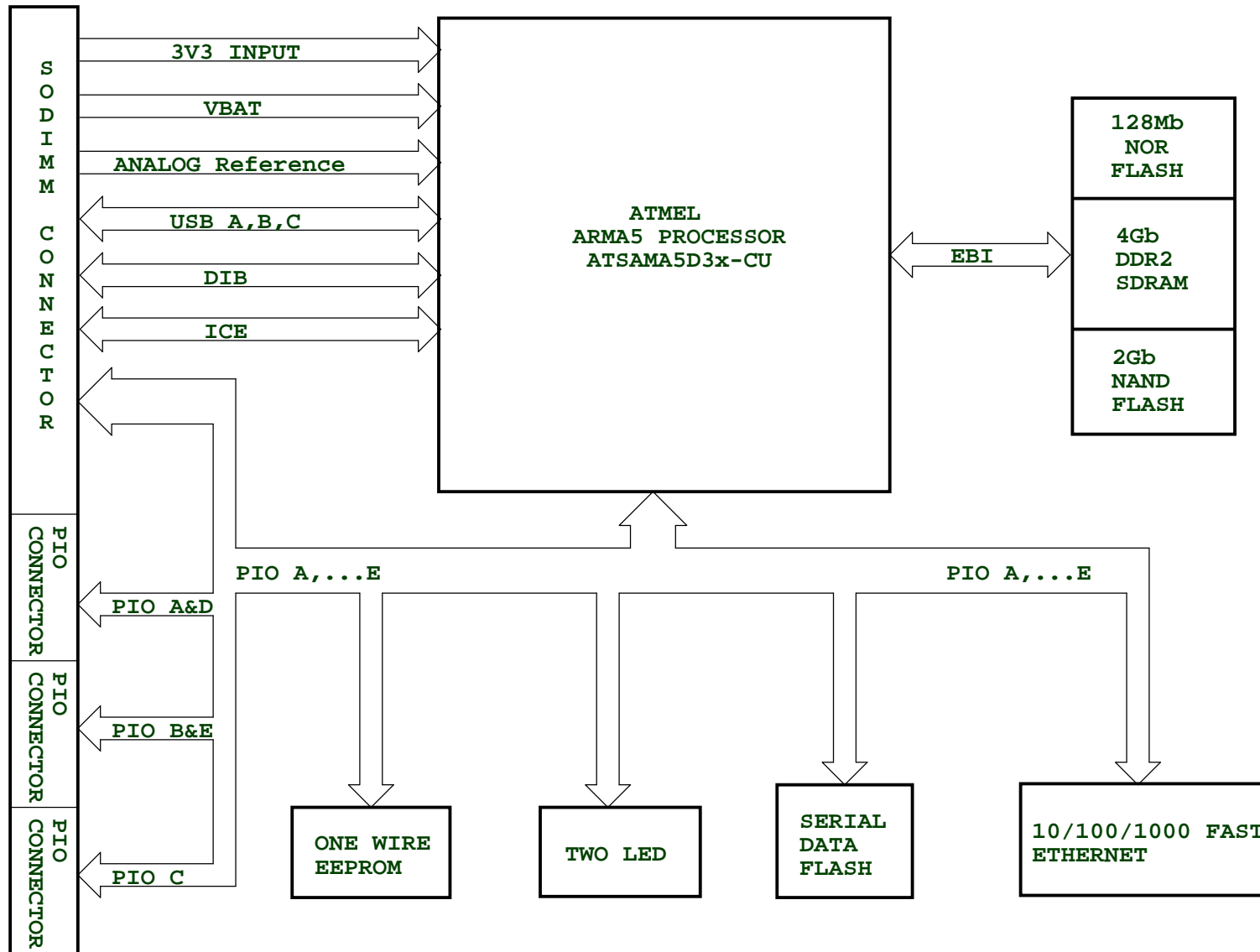
		<a href="http://arm.embedinfo.com">http://arm.embedinfo.com</a>	
		Title: SAMASD3x-CM	
Size: A3	Document Number: ETHERNET	Rev: D	
Draw By: Zhu Xueliang	Date: Friday, September 21, 2012	Sheet: 6 of 7	



#### 4.4.2 CPU Module Revision E Schematics

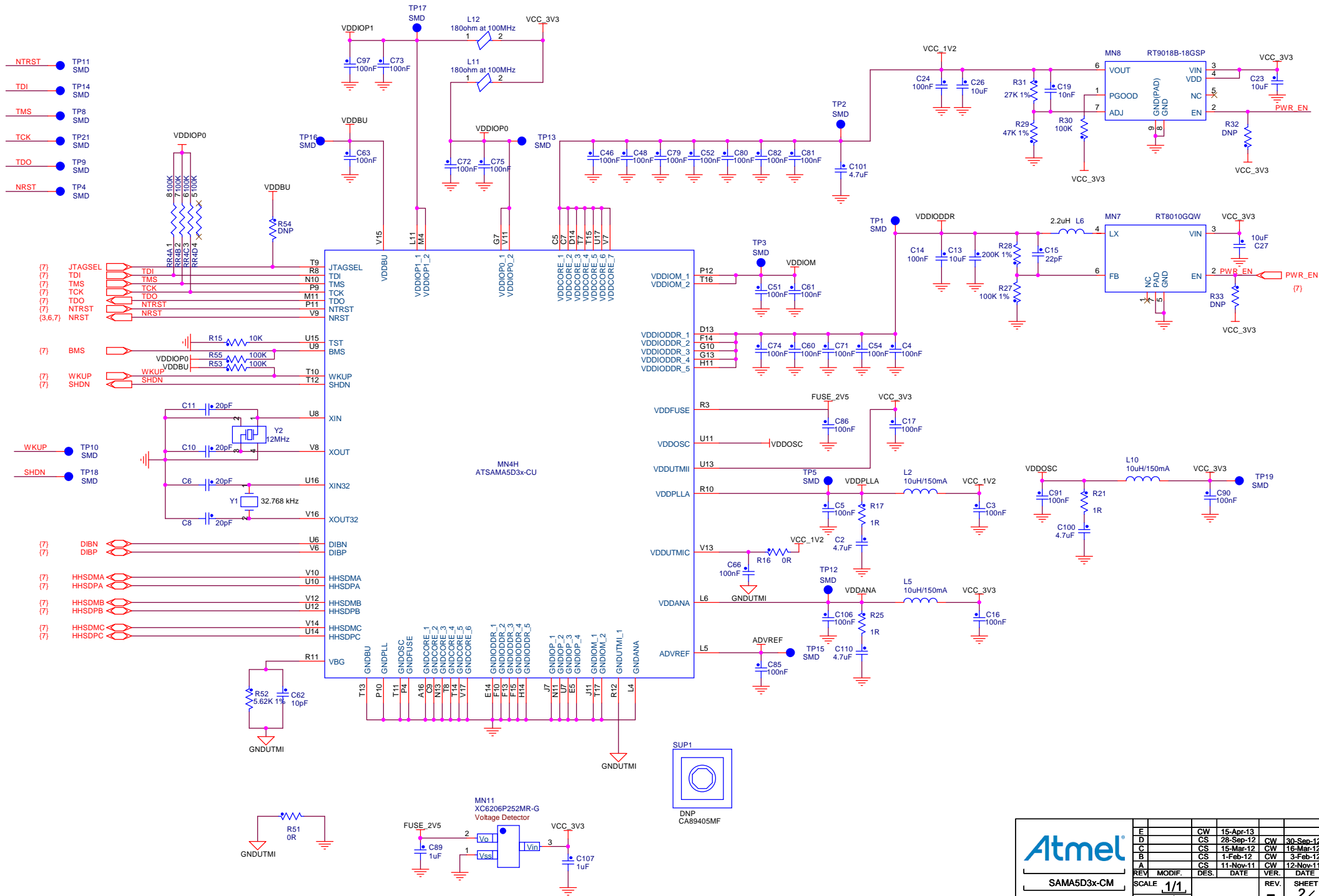
This section contains the following schematics:

- Main sheet
- SODIMM 200
- Power supply
- CPU power supply
- DDR2 interface
- FI: NAND, NOR, Serial, I2C, 1-wire
- Ethernet
- USB, JTAG, LEDs
- Bus interface



		REV	MODIF.	DES.	DATE	REV.	DATE
E		CW		15-Apr-13			
D		CS		28-Sep-12	CW		30-Sep-12
C		CS		15-Mar-12	CW		16-Mar-12
B		CS		1-Feb-12	CW		3-Feb-12
A		CS		11-Nov-11	CW		12-Nov-11
SCALE	1/1	REV.			SHEET		
SAMA5D3x-CM		E			1/1		
BLOCK DIAGRAM							

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Atmel		SAMA5D3x-CM		SAMA5D3x-I&POWER	
REV	MODIF.	DES.	DATE	VER.	DATE
A		CS	11-Nov-11	CW	12-Nov-11
B		CS	15-Mar-12	CW	16-Mar-12
C		CS	28-Sep-12	CW	30-Sep-12
D		CS	28-Sep-12	CW	30-Sep-12
E		CW	15-Apr-13		
SCALE 1/1				REV. E	SHEET 2/4

SAMA5D3x-CM

SAMA5D3x-I&POWER

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MN4A  
ATSAMA5D3x-CU

PA0_LCDDAT0	E3	PA0
PA1_LCDDAT1	F5	PA1
PA2_LCDDAT2	D2	PA2
PA3_LCDDAT3	F4	PA3
PA4_LCDDAT4	D1	PA4
PA5_LCDDAT5	J10	PA5
PA6_LCDDAT6	G4	PA6
PA7_LCDDAT7	J9	PA7
PA8_LCDDAT8	F3	PA8
PA9_LCDDAT9	J8	PA9
PA10_LCDDAT10	E2	PA10
PA11_LCDDAT11	K8	PA11
PA12_LCDDAT12	F2	PA12
PA13_LCDDAT13	G6	PA13
PA14_LCDDAT14	E1	PA14
PA15_LCDDAT15	H5	PA15
PA16_LCDDAT16	H3	PA16
PA17_LCDDAT17	H6	PA17
PA18_LCDDAT18	H4	PA18
PA19_LCDDAT19	H7	PA19
PA20_LCDDAT20	H2	PA20
PA21_LCDDAT21	J6	PA21
PA22_LCDDAT22	G2	PA22
PA23_LCDDAT23	J5	PA23
PA24_LCDDAT24	F1	PA24
PA25_LCDDAT25	J4	PA25
PA26_LCDDAT26	G3	PA26
PA27_LCDDAT27	J3	PA27
PA28_LCDDAT28	G1	PA28
PA29_LCDDAT29	K4	PA29
PA30_LCDDAT30	H1	PA30
PA31_LCDDAT31	K3	PA31

PA[0..31] (7)

MN4C  
ATSAMA5D3x-CU

PC0_ETX0	D8	PC0
PC1_ETX1	A4	PC1
PC2_ERX0	E8	PC2
PC3_ERX1	A3	PC3
PC4_ETXEN	A2	PC4
PC5_ECRSDV	F8	PC5
PC6_ERXER	B3	PC6
PC7_EREFCK	G8	PC7
PC8_EMDC	B4	PC8
PC9_EMPIO	F7	PC9
PC10	A1	PC10
PC11	D7	PC11
PC12	C6	PC12
PC13	E7	PC13
PC14	B2	PC14
PC15	F6	PC15
PC16	B1	PC16
PC17	E6	PC17
PC18	C3	PC18
PC19	D6	PC19
PC20	C4	PC20
PC21	D5	PC21
PC22	C2	PC22
PC23	G9	PC23
PC24	F1	PC24
PC25	H10	PC25
PC26	H9	PC26
PC27	D4	PC27
PC28	H8	PC28
PC29	G5	PC29
PC30	D3	PC30
PC31	E4	PC31

PC[0..31] (7)

MN4B  
ATSAMA5D3x-CU

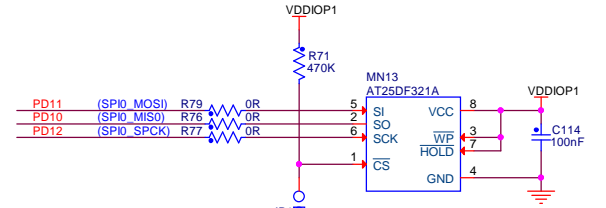
PB0_GTX0	T2	PB0
PB1_GTX1	N7	PB1
PB2_GTX2	T3	PB2
PB3_GTX3	N6	PB3
PB4_GRX0	P5	PB4
PB5_GRX1	T4	PB5
PB6_GRX2	R4	PB6
PB7_GRX3	U1	PB7
PB8_GTXCK	R5	PB8
PB9_GTXEN	P3	PB9
PB10_GTXER	R6	PB10
PB11_GRXCK	V3	PB11
PB12_GRXDV	P6	PB12
PB13_GRXER	V1	PB13
PB14_GCRS	R7	PB14
PB15_GCOL	U3	PB15
PB16_GMDC	P7	PB16
PB17_GMDIO	V2	PB17
PB18_G125CK	V5	PB18
PB19_GTX4	T6	PB19
PB20_GTX5	N8	PB20
PB21_GTX6	U4	PB21
PB22_GTX7	M7	PB22
PB23_GRX4	U5	PB23
PB24_GRX5	M8	PB24
PB25_GRX6	T5	PB25
PB26_GRX7	N9	PB26
PB27	V4	PB27
PB28	M9	PB28
PB29	P8	PB29
PB30	M10	PB30
PB31	R9	PB31

PB[0..31] (6,7)

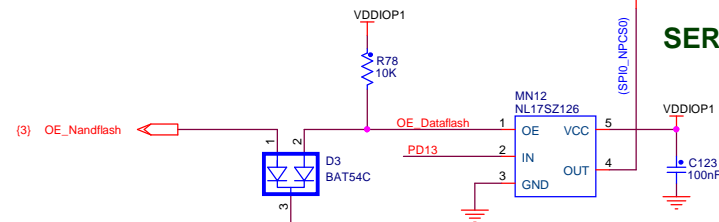
MN4D  
ATSAMA5D3x-CU

PD0	K5	PD0
PD1	P1	PD1
PD2	K6	PD2
PD3	R1	PD3
PD4	L7	PD4
PD5	P2	PD5
PD6	L3	PD6
PD7	R2	PD7
PD8	K7	PD8
PD9	U2	PD9
PD10	K9	PD10
PD11	M5	PD11
PD12	K10	PD12
PD13	N4	PD13
PD14	L9	PD14
PD15	N3	PD15
PD16	L10	PD16
PD17	N5	PD17
PD18	M6	PD18
PD19	T1	PD19
PD20	N8	PD20
PD21	M3	PD21
PD22	M2	PD22
PD23	L3	PD23
PD24	M1	PD24
PD25	N1	PD25
PD26	L1	PD26
PD27	L2	PD27
PD28	K1	PD28
PD29	K2	PD29
PD30	J1	PD30
PD31	J2	PD31

PD[0..31] (7)

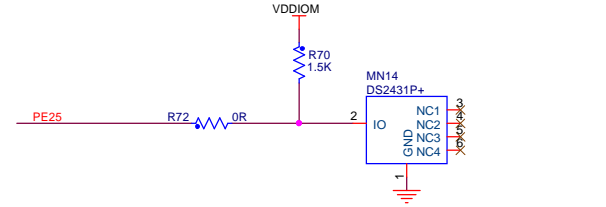


**SERIAL DATAFLASH**

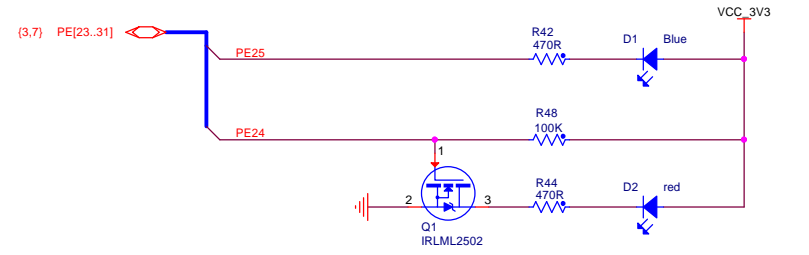


(3) OE\_Nandflash

(7) BOOT\_CS\_OFF



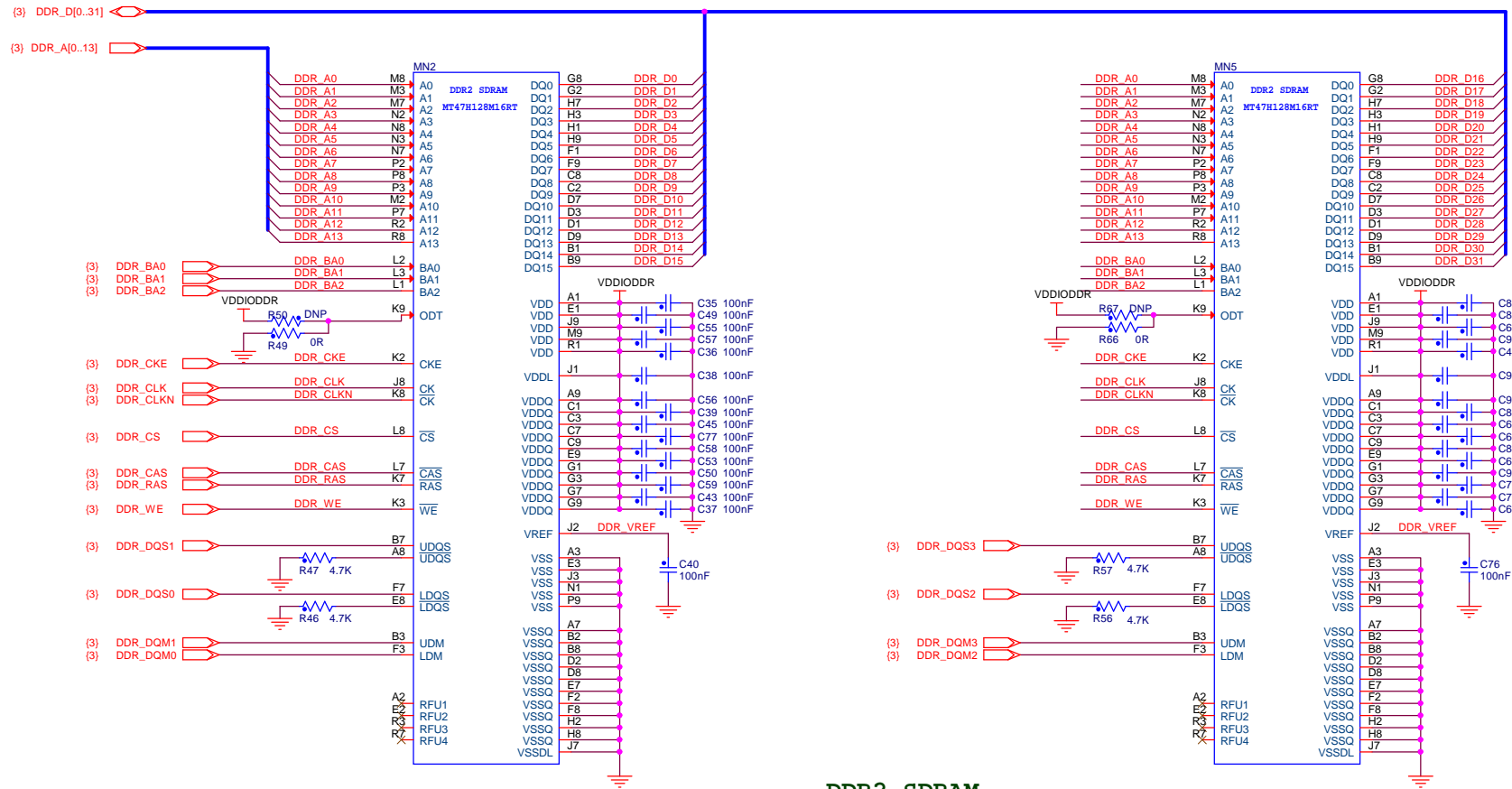
**1-WIRE EEPROM**



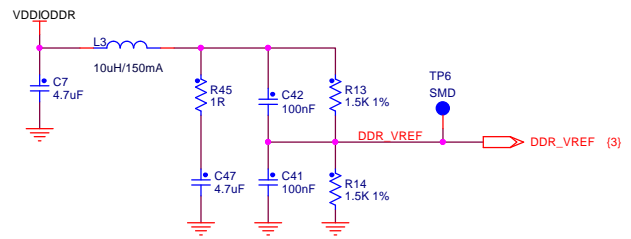
**LED**

Atmel		E	CW	15-Apr-13	
		D	CS	28-Sep-12	CW 30-Sep-12
		C	CS	15-Mar-12	CW 16-Mar-12
		B	CS	1-Feb-12	CW 3-Feb-12
		A	CS	11-Nov-11	CW 12-Nov-11
REV	MODIF.	DES.	DATE	VER.	DATE
SAMA5D3x-CM		SCALE	1/1	REV.	SHEET
SAMA5D3x-III&DATAFLASH&1-WIRE-LED				E	4/

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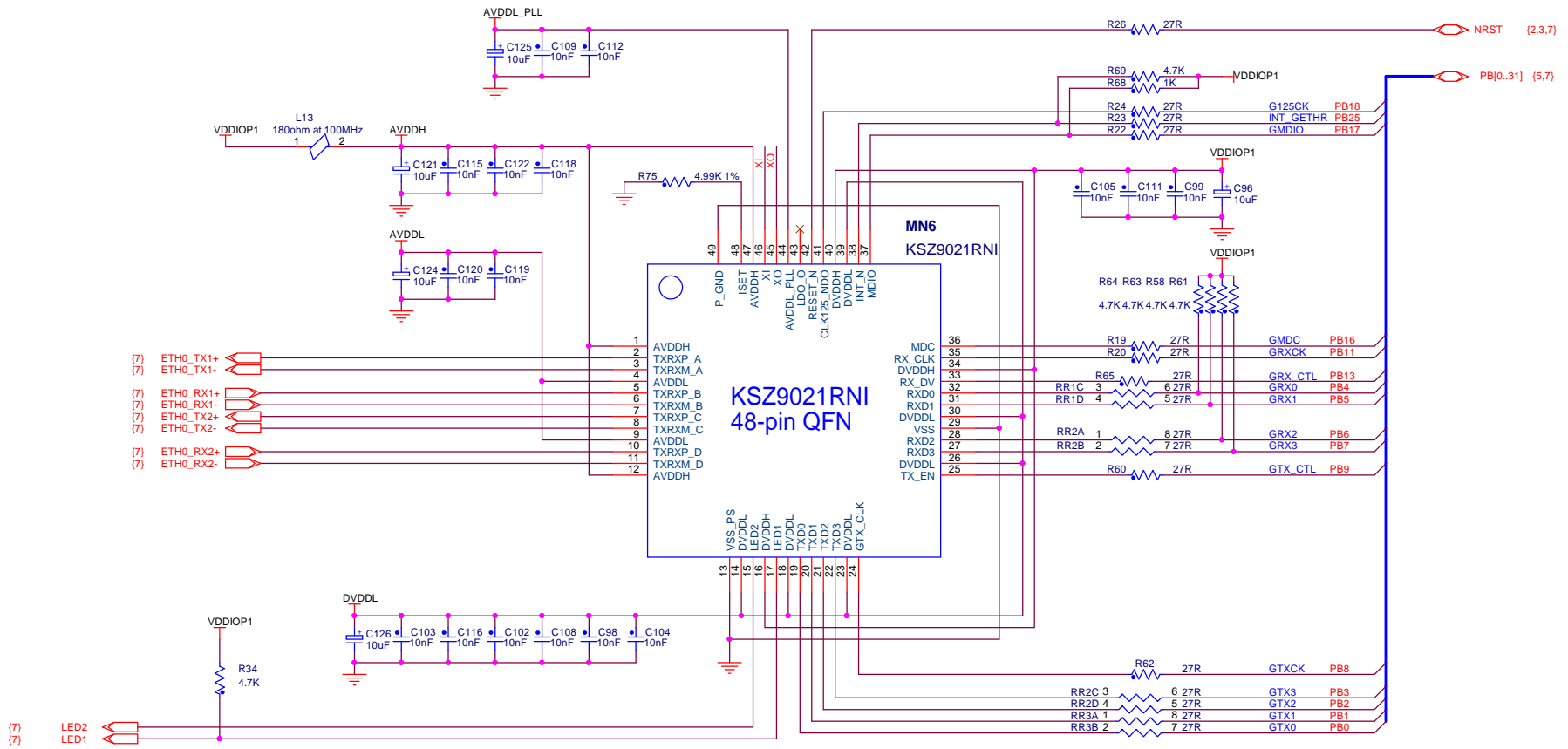
**DDR2 SDRAM**



		REV	MODIF.	DES.	DATE	REV	DATE
		A		CS	11-Nov-11	CW	12-Nov-11
SAMA5D3x-CM		SCALE	1/1		REV	SHEET	
4Gb DDR2						E	5/7

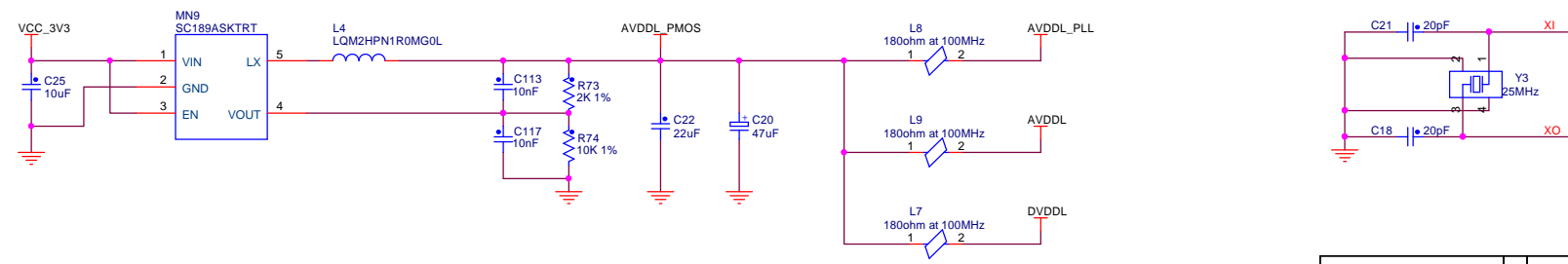
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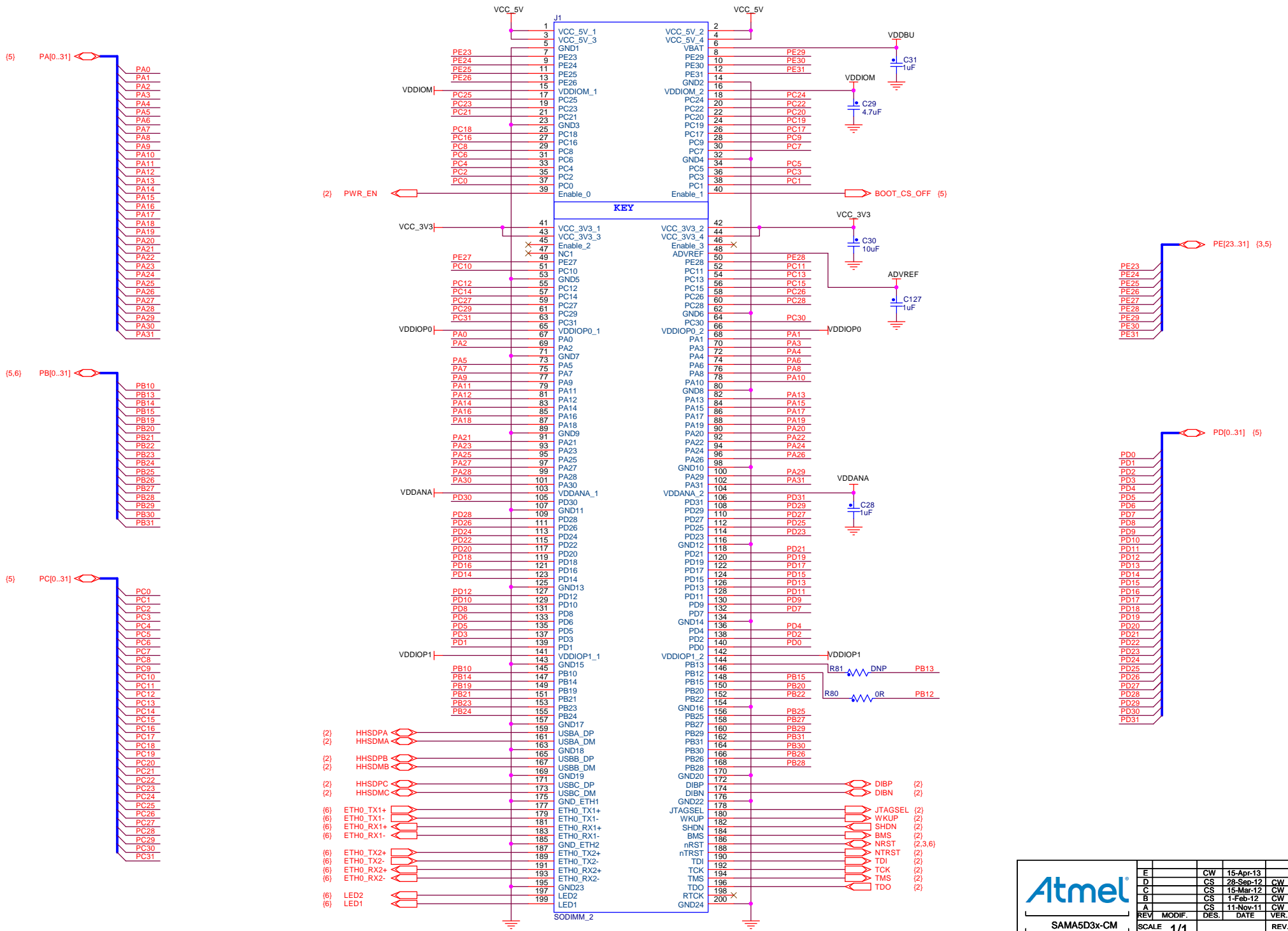
(7) LED2  
(7) LED1

(7) ETH0\_TX1+  
(7) ETH0\_TX1-  
(7) ETH0\_RX1+  
(7) ETH0\_RX1-  
(7) ETH0\_TX2+  
(7) ETH0\_TX2-  
(7) ETH0\_RX2+  
(7) ETH0\_RX2-



		E	CW	15-Apr-13			
		D	CS	28-Sep-12	CW 30-Sep-12		
<b>SAMA5D3x-CM</b> ETHERNET		C	CS	15-Mar-12	CW 16-Mar-12		
		B	CS	1-Feb-12	CW 3-Feb-12		
SCALE 1/1 		A	CS	11-Nov-11	CW 12-Nov-11		
		REV	MODIF.	DES.	DATE	VER.	DATE
		E					SHEET 6/7

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- (2) HHSDPA
- (2) HHSDMA
- (2) HHSDPB
- (2) HHSDMB
- (2) HHSDPC
- (2) HHSDMC
- (6) ETH0\_TX1+
- (6) ETH0\_TX1-
- (6) ETH0\_RX1+
- (6) ETH0\_RX1-
- (6) ETH0\_TX2+
- (6) ETH0\_TX2-
- (6) ETH0\_RX2+
- (6) ETH0\_RX2-
- (6) LED2
- (6) LED1
- USBA\_DP
- USBA\_DM
- USBS\_DP
- USBS\_DM
- USBC\_DP
- USBC\_DM
- GND\_ETH1
- ETH0\_TX1+
- ETH0\_TX1-
- ETH0\_RX1+
- ETH0\_RX1-
- GND\_ETH2
- ETH0\_TX2+
- ETH0\_TX2-
- TCK
- TMS
- TDO
- RTCK
- GND24
- JTAGSEL (2)
- WKUP (2)
- SHDN (2)
- BMS (2)
- nRST (2,3,6)
- NTRST (2)
- TDI (2)
- TCK (2)
- TMS (2)
- TDO (2)

**Atmel**  
SAMA5D3x-CM  
200-PIN SODIMM

E		CW	15-Apr-13		
D		CS	28-Sep-12	CW	30-Sep-12
C		CS	15-Mar-12	CW	16-Mar-12
B		CS	1-Feb-12	CW	3-Feb-12
A		CS	11-Nov-11	CW	12-Nov-11
REV.	MODIF.	DES.	DATE	VER.	DATE
SCALE	1/1			REV.	SHEET
				E	7/7

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## 4.5 Ronetix Schematics

This section contains the schematics for the CM board manufactured by Ronetix:

- Main sheet
- SODIMM200
- Power supply
- CPU power supply
- DDR2 interface
- FI: NAND, NOR, Serial, I2C, 1-wire
- Ethernet
- USB, JTAG, LEDs
- Bus interface



SCHEMATICS: SAMA5D3x-CM

SHEET #	SHEET NAME
1	MAIN
2	SODIM200
3	POWER SUPPLY
4	CPU-POWER SUPPLY
5	DDR2 INTERFACE
6	FI: NAND/NOR/SERIAL/I2C/1-WIRE
7	ETHERNET
8	USB/JTAG/LEDS
9	BUS INTERFACE

DATE:	DESCRIPTION	REVISION	STATUS
15.03.2012	SAMA5D3x-CM v2.0	2.0	OPEN
20.09.2012	SAMA5D3x-CM v2.0	2.0	CLOSE

Changes Rev2.0

- SoDIMM200 change:  
 \* PB13 pin 144 with 0R DNP  
 \* PB12 pin 146 with 0R populated
- VDD\_CORE from 1.20V to 1.25V
- US1 - From TPS71712DCKR to BU12TD3WG-TR and attribute DNP
- Replaced Q2 with U15 SC189ASKTRT 1V0
- Q1 from BSS138W(SOT323) to BSS138(SOT23)
- C74 - from 47uF Tant to 22uF 0805  
 Added - C128 22uF 0805  
 C78 - from 47uF Tant to 22uF 0805  
 Added - C129 22uF 0805  
 C81 - from 47uF Tant to 22uF 0805  
 Added - C130 22uF 0805  
 C75 - from 47uF Tant to 22uF 0805  
 Added - C131 22uF 0805  
 C80 - from 47uF Tant to 22uF 0805  
 Added - C132 22uF 0805  
 C92 - from 10u Tant to 10u 0805
- R4 - Changed attribute Note from DNP to "empty"
- Y1 changed to CM200C-32.768KDZF-UT
- U6 changed to EN29GL128H-70BAIP
- U8 changed to HY27UF082G2B-TPCB

Mechanical

○ Z6 Drill No plated 0.85mm	○ Z11 Passer 0.7 mm
○ Z7 Drill No plated 0.85mm	○ Z12 Passer 0.7 mm
○ Z5 Drill No plated 1.65mm	○ Z13 Passer 0.7 mm
○ Z8 Drill No plated 1.65mm	○ Z14 Passer 0.7 mm
○ Z9 Drill No plated 1.65mm	
○ Z10 Drill No plated 1.65mm	
○ Z1 Drill No plated 1.8 mm	○ Z3 Drill No plated 3.2 mm
○ Z2 Drill No plated 1.8 mm	○ Z4 Drill No plated 3.2 mm

Note: To each Signal Reference have one or more digits.  
 These are the numbers of sheets  
 to which is connected this signal.

PROJECT TITLE		SAMA5D3x-CM		SHEET NO		1 OF 9	
SHEET TITLE		MAIN		DROWN			
FILE	REV	DATE	DESCRIPTION FILE	ISSUED			
A4		20.9.2012					



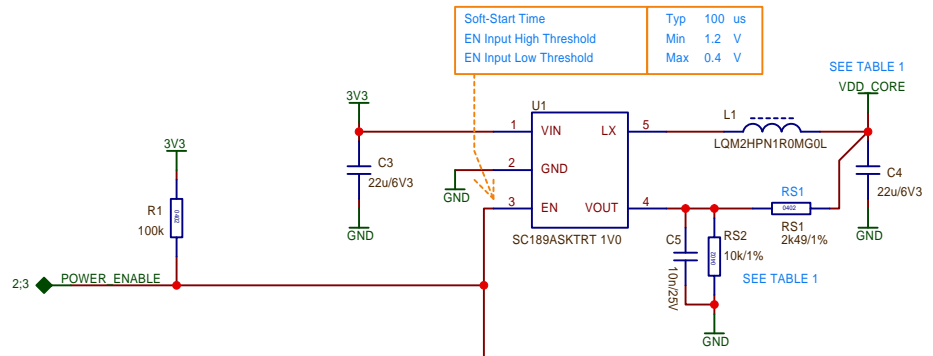


MECHANICAL KEYING SODIM200 :

- ✓ Power Supply 2.5V -> distance between pin 39 and center notch = 1.80mm
- Power Supply 1.8V -> distance between pin 39 and center notch = 2.70mm

PROJECT TITLE				SAMA5D3x-CM			
SHEET TITLE				SODIM200			
FILE	REV	DATE	DESCRIPTION	FILE	REV	DATE	DESCRIPTION
A4		20.9.2012					
SHEET NO				2 OF 9			
DROWN							
ISSUED							



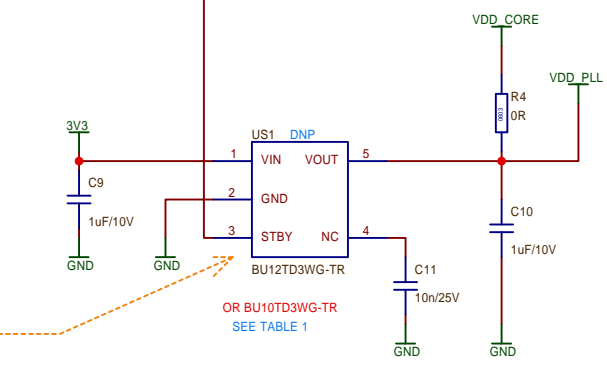
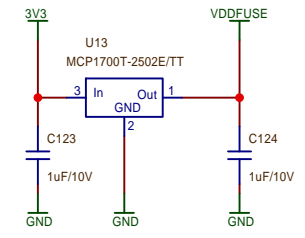
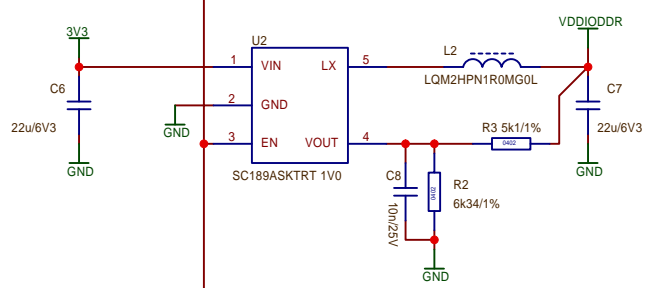


Soft-Start Time	Typ	100 us
EN Input High Threshold	Min	1.2 V
EN Input Low Threshold	Max	0.4 V

SEE TABLE 1

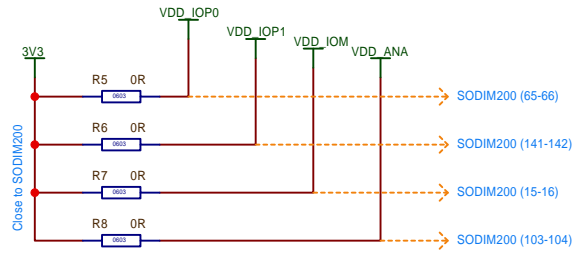
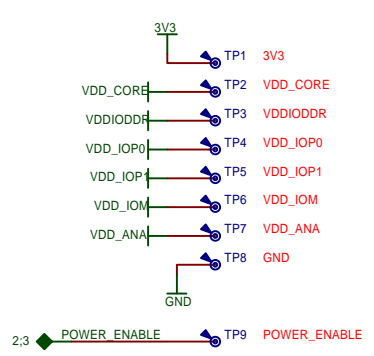
TABLE 1  $RS1=(V_{out}-1)\times RS2$

VDD_CORE	1.0V	1.2V	1.25V	
RS1	0R (JUMP)	2kOhm 1%	2k5ohm 1%	2k49ohm 1%
RS2	DNP	10kOhm 1%	10kOhm 1%	
US1	BU10TD3WG-TR	BU12TD3WG-TR		



Start Time	Typ	50 us
EN Input High Threshold	Min	1.2 V
EN Input Low Threshold	Max	0.3 V

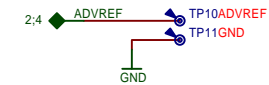
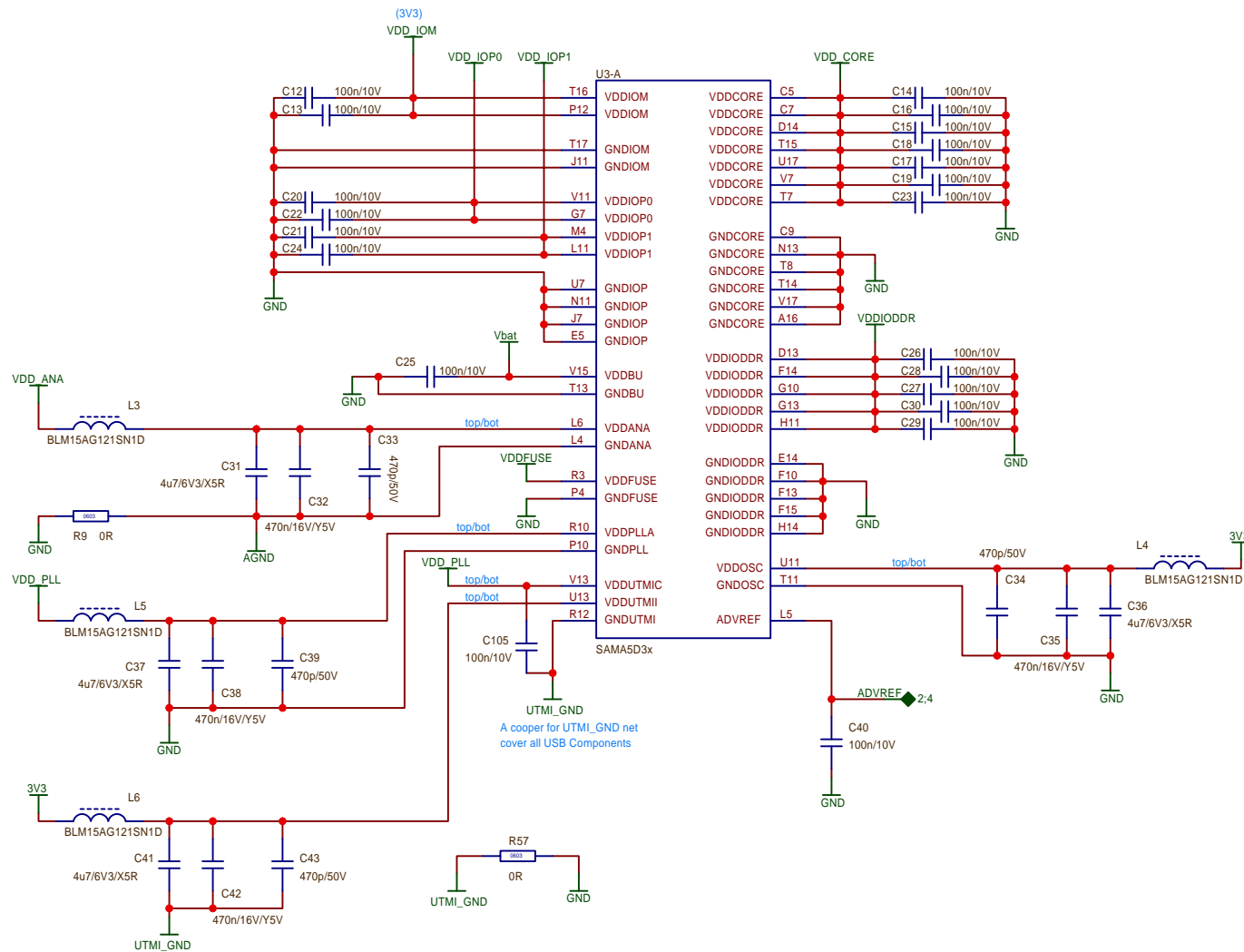
OR BU10TD3WG-TR  
SEE TABLE 1



GND pins are provided and should be connected as shortly as possible to the system ground plane.

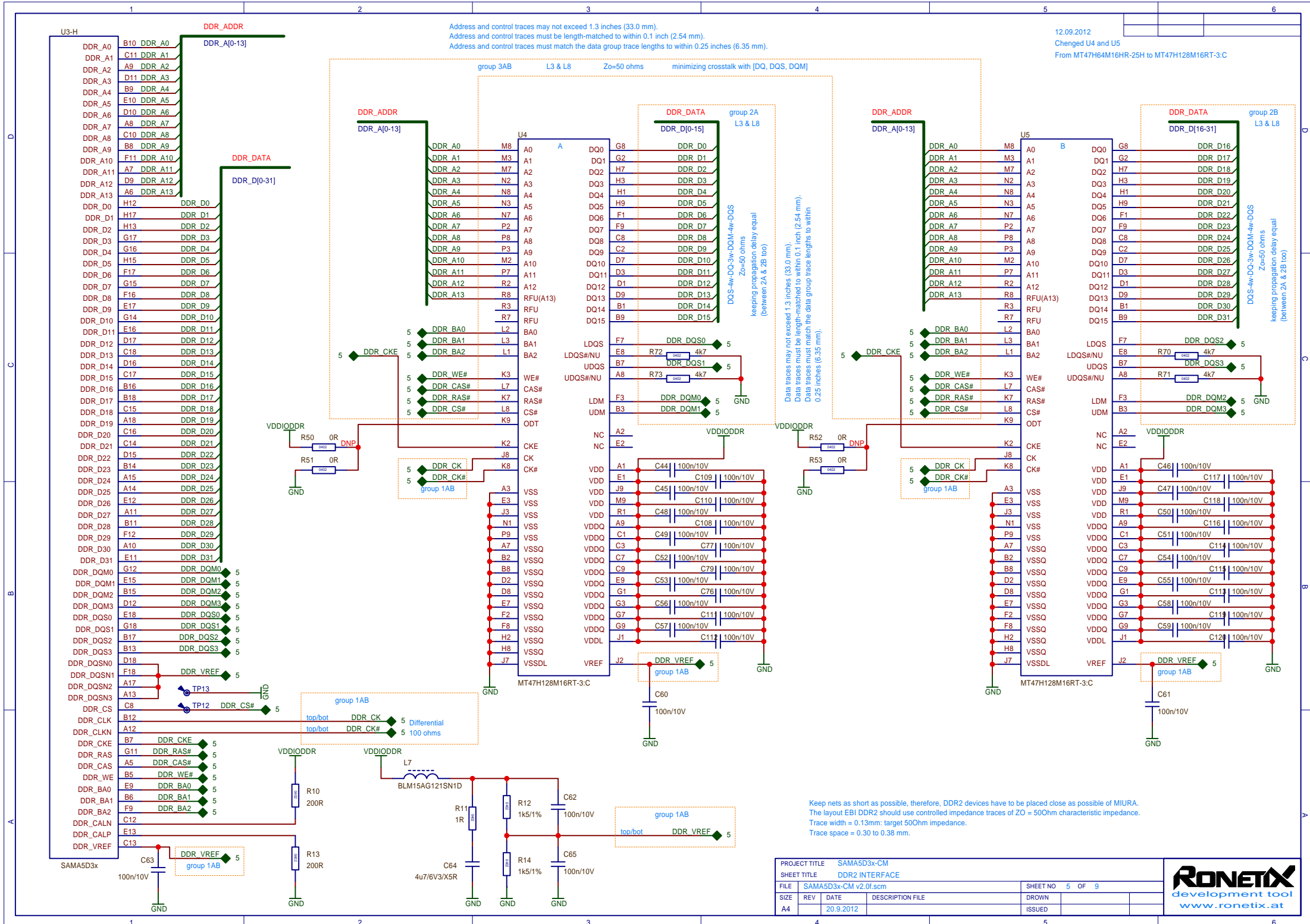
PROJECT TITLE		SAMA5D3x-CM		SHEET NO		3 OF 9	
SHEET TITLE		POWER SUPPLY		DROWN			
FILE	SAMA5D3x-CM v2.0f.scm	DATE	20.9.2012	ISSUED			
SIZE	A4	DESCRIPTION FILE					





PROJECT TITLE		SAMA5D3x-CM		SHEET NO		4 OF 9	
SHEET TITLE		CPU-POWER SUPPLY		DRAWN			
FILE	SAMA5D3x-CM v2.0f.scm			ISSUED			
SIZE	REV	DATE	DESCRIPTION FILE				
A4		20.9.2012					





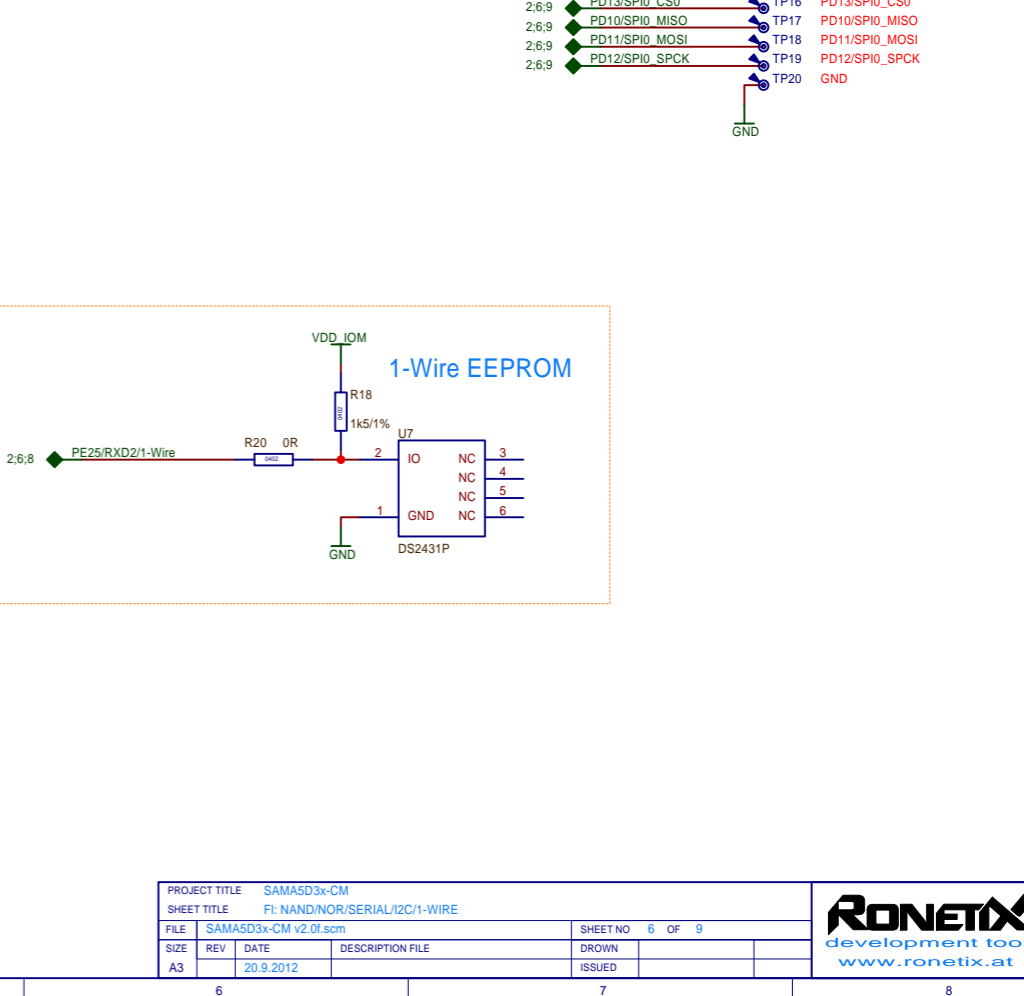
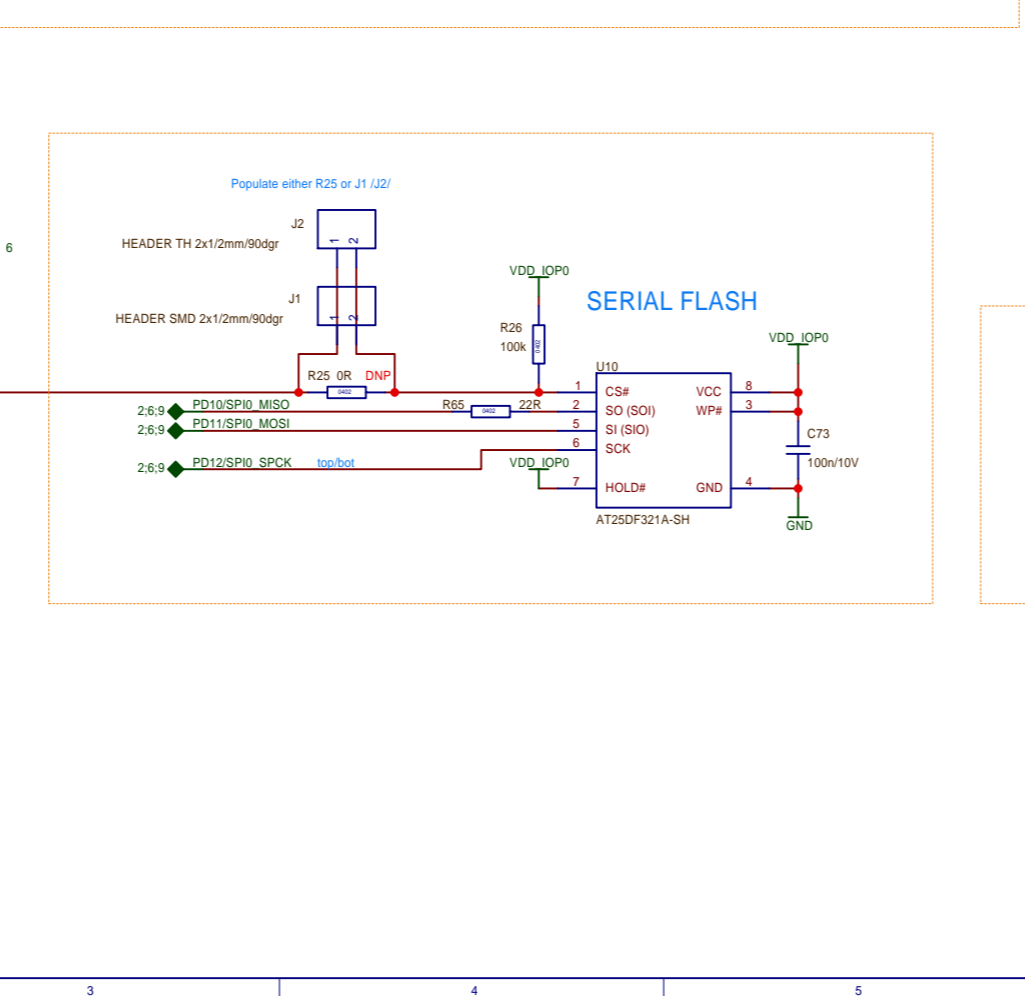
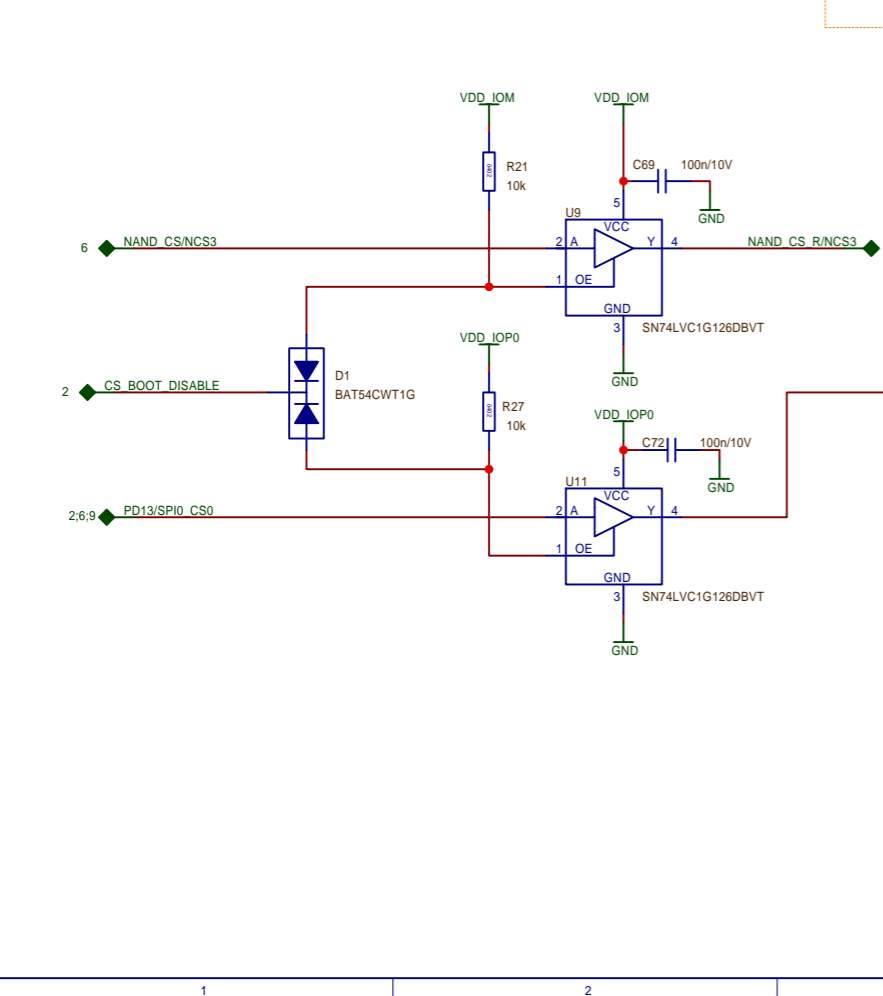
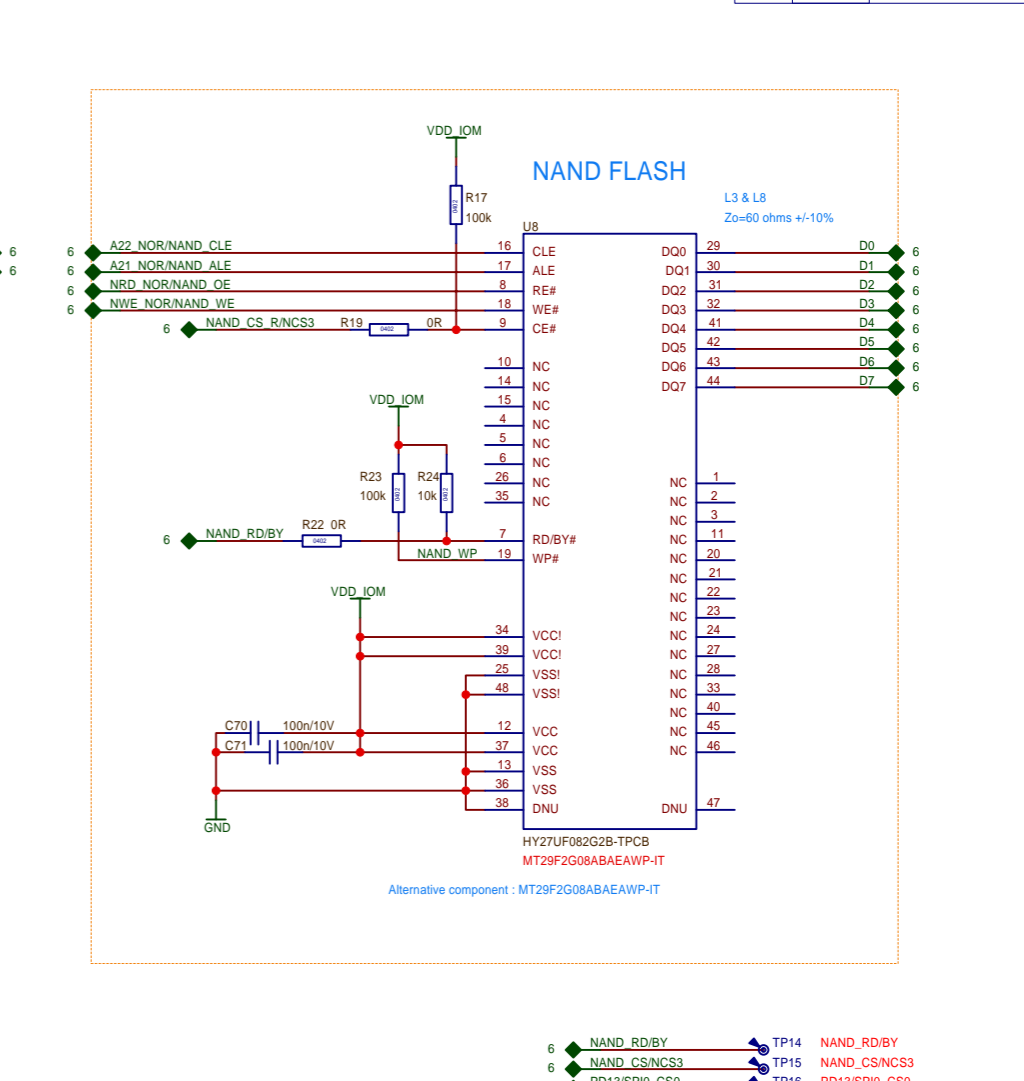
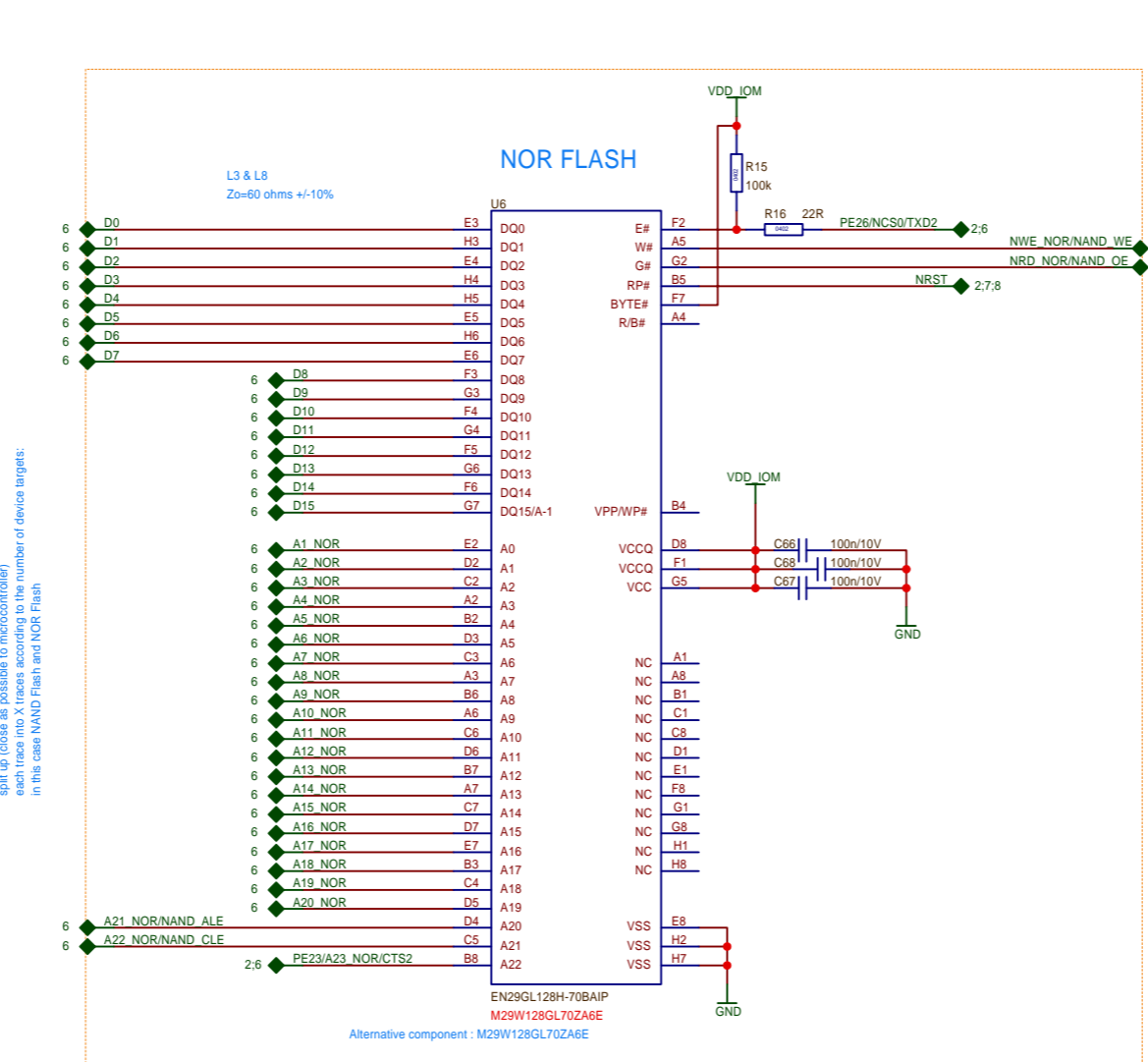
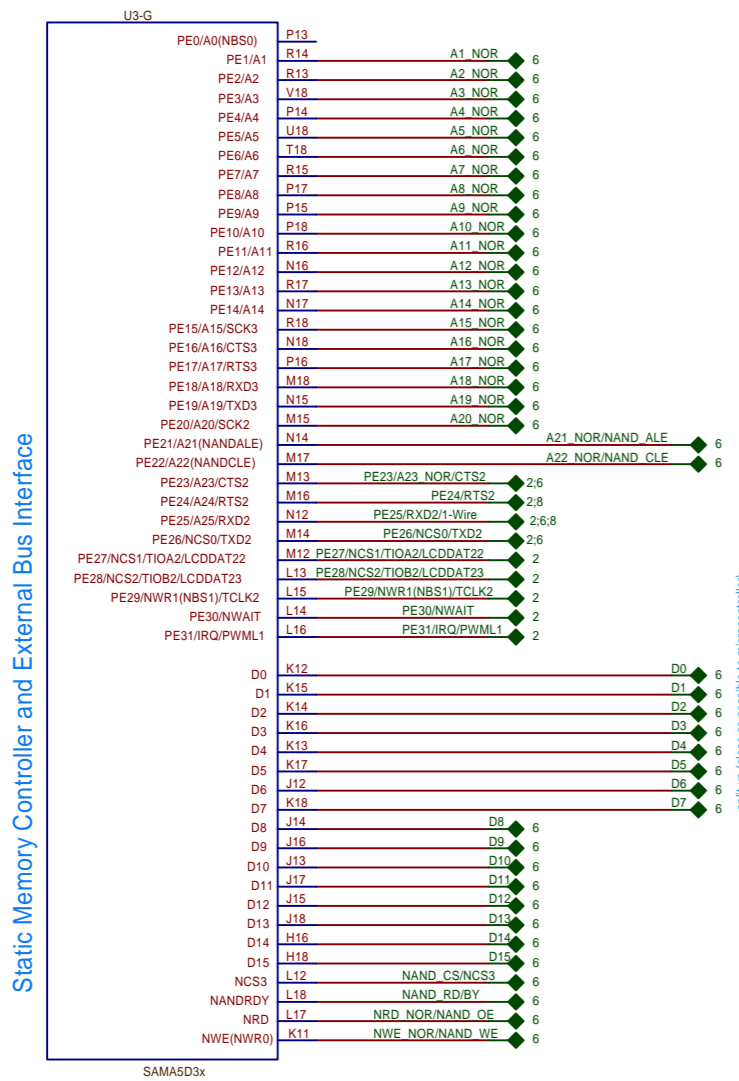
12.09.2012  
Changed U4 and U5  
From MT47H64M16HR-25H to MT47H128M16RT-3-C

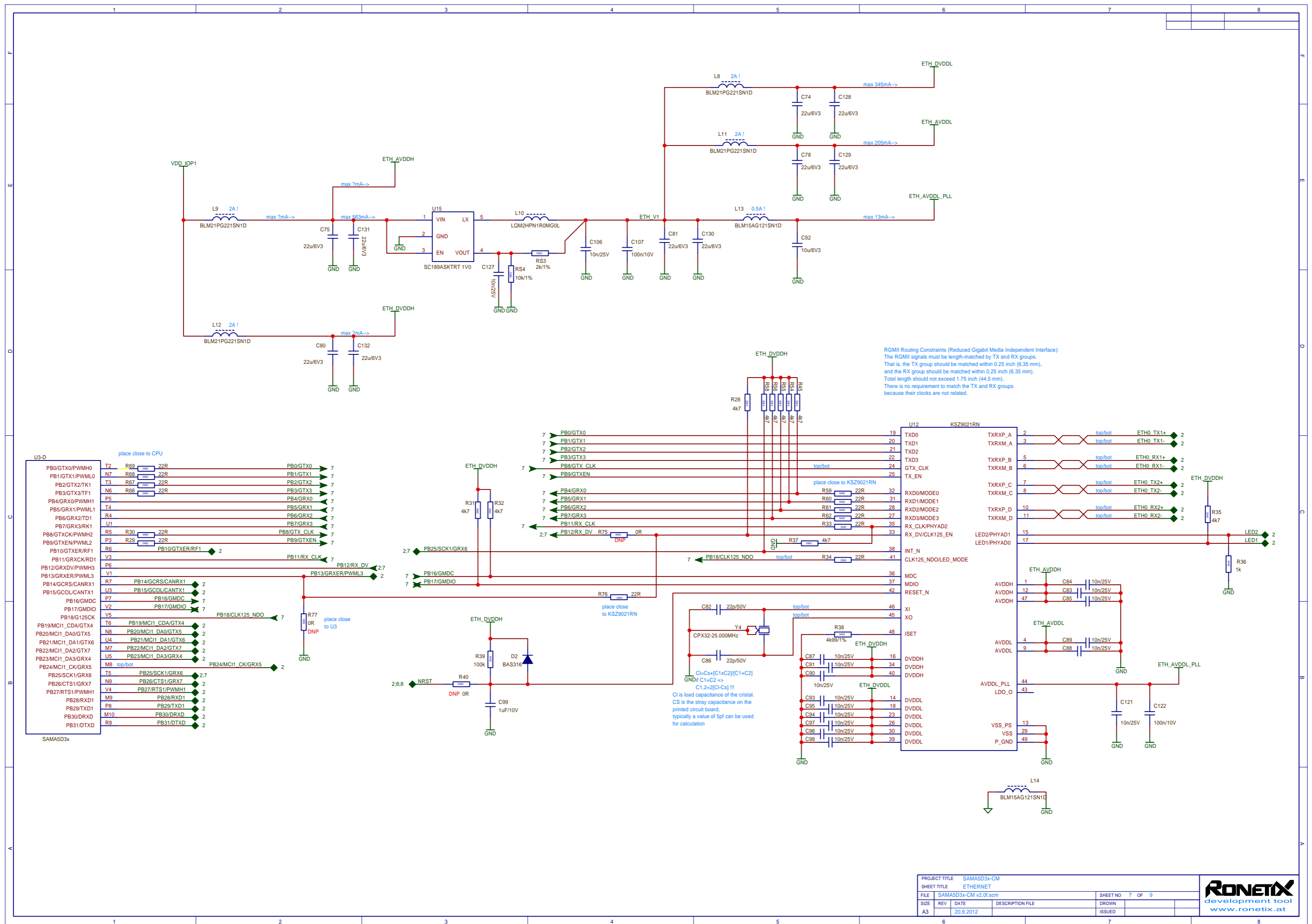
Keep nets as short as possible, therefore, DDR2 devices have to be placed close as possible of MIURA.  
The layout EBI DDR2 should use controlled impedance traces of Z0 = 50Ohm characteristic impedance.  
Trace width = 0.13mm; target 50Ohm impedance.  
Trace space = 0.30 to 0.38 mm.

PROJECT TITLE		SAMA5D3x-CM		
SHEET TITLE		DDR2 INTERFACE		
FILE	SAMA5D3x-CM v2.0f.scm	SHEET NO	5 OF 9	
SIZE	REV	DATE	DESCRIPTION	FILE
A4		20.9.2012		
DROWN		ISSUED		





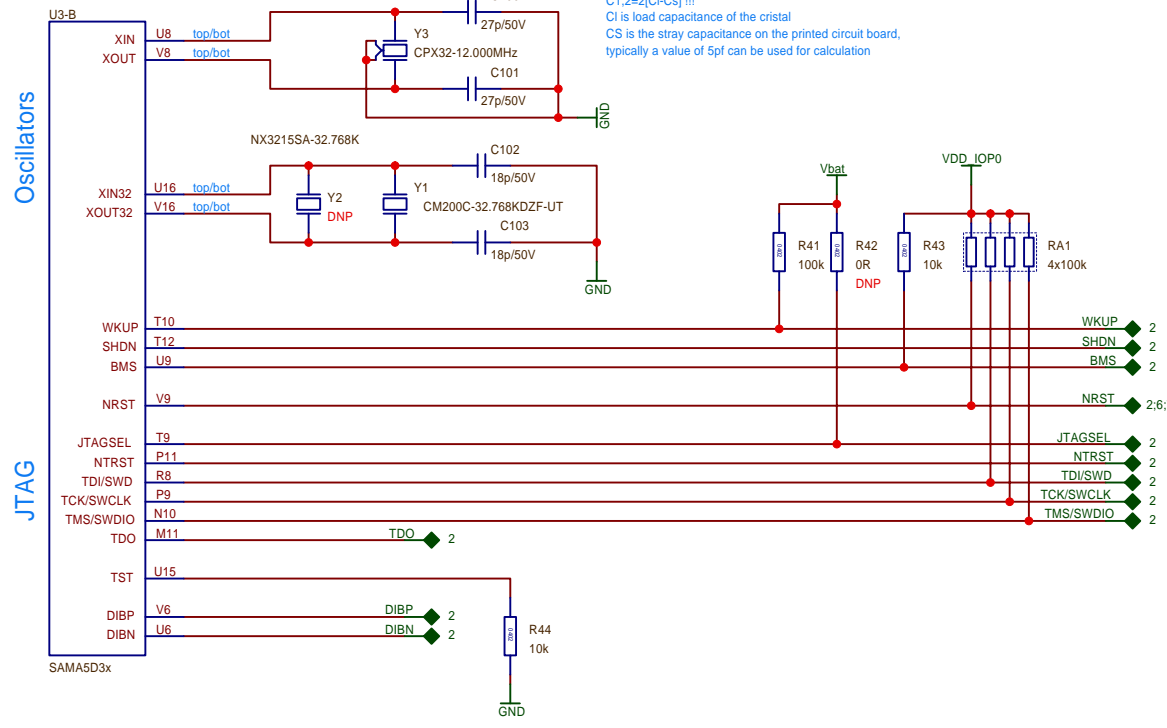




PROJECT TITLE		SAM5D3x-CM	
SHEET TITLE		ETHERNET	
FILE	SAM5D3x-CM v2.0f.scm	SHEET NO	7 OF 9
SIZE	REV	DATE	DESCRIPTION FILE
A3		20.9.2012	
		DROWN	
		ISSUED	



# SOFT MODEM



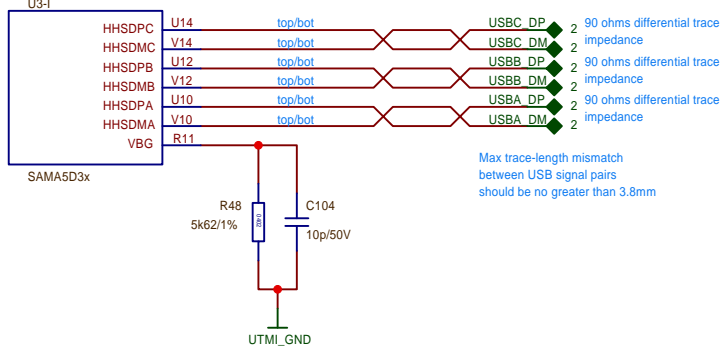
$Cl = C_s + [C1 \times C2] / [C1 + C2]$   
 if  $C1 = C2 \Rightarrow$   
 $C1,2 = 2 \times [Cl - C_s]$  !!!  
 Cl is load capacitance of the cristal  
 Cs is the stray capacitance on the printed circuit board,  
 typically a value of 5pF can be used for calculation

Oscillators

JTAG

SAMA5D3x

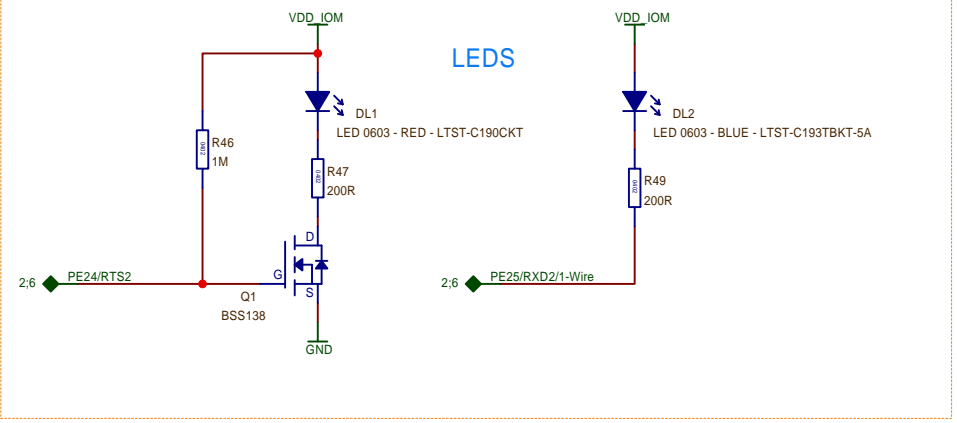
# USB



Max trace-length mismatch  
 between USB signal pairs  
 should be no greater than 3.8mm

SAMA5D3x

# LEDS



PROJECT TITLE				SAMA5D3x-CM			
SHEET TITLE				USB/JTAG/LEDS			
FILE	SAMA5D3x-CM v2.0f.scm			SHEET NO	8 OF 9		
SIZE	REV	DATE	DESCRIPTION FILE	DROWN			
A4		20.9.2012		ISSUED			



U3-C SAMA5D3x			
PA0/LCDDAT0	E3	PA0/LCDDAT0	2
PA1/LCDDAT1	F5	PA1/LCDDAT1	2
PA2/LCDDAT2	D2	PA2/LCDDAT2	2
PA3/LCDDAT3	F4	PA3/LCDDAT3	2
PA4/LCDDAT4	D1	PA4/LCDDAT4	2
PA5/LCDDAT5	J10	PA5/LCDDAT5	2
PA6/LCDDAT6	G4	PA6/LCDDAT6	2
PA7/LCDDAT7	J9	PA7/LCDDAT7	2
PA8/LCDDAT8	F3	PA8/LCDDAT8	2
PA9/LCDDAT9	J8	PA9/LCDDAT9	2
PA10/LCDDAT10	E2	PA10/LCDDAT10	2
PA11/LCDDAT11	K8	PA11/LCDDAT11	2
PA12/LCDDAT12	F2	PA12/LCDDAT12	2
PA13/LCDDAT13	G6	PA13/LCDDAT13	2
PA14/LCDDAT14	E1	PA14/LCDDAT14	2
PA15/LCDDAT15	H5	PA15/LCDDAT15	2
PA16/LCDDAT16/ISI_D0	H3	PA16/LCDDAT16/ISI_D0	2
PA17/LCDDAT17/ISI_D1	H6	PA17/LCDDAT17/ISI_D1	2
PA18/LCDDAT18/TWD2/ISI_D2	H4	PA18/LCDDAT18/TWD2/ISI_D2	2
PA19/LCDDAT19/TWCK2/ISI_D3	H7	PA19/LCDDAT19/TWCK2/ISI_D3	2
PA20/LCDDAT20/PWMH0	H2	PA20/LCDDAT20/PWMH0	2
PA21/LCDDAT21/PWML0/ISI_D5	J6	PA21/LCDDAT21/PWML0/ISI_D5	2
PA22/LCDDAT22/PWMH1	G2	PA22/LCDDAT22/PWMH1	2
PA23/LCDDAT23/PWML1/ISI_D7	J5	PA23/LCDDAT23/PWML1/ISI_D7	2
PA24/LCDPWM	F1	PA24/LCDPWM	2
PA25/LCDDISP	J4	PA25/LCDDISP	2
PA26/LCDVSYNC	G3	PA26/LCDVSYNC	2
PA27/LCDHSYNC	J3	PA27/LCDHSYNC	2
PA28/LCDPCK	G1	PA28/LCDPCK	2
PA29/LCDDEN	K4	PA29/LCDDEN	2
PA30/TWD0/URXD1/ISI_VSYNC	H1	PA30/TWD0/URXD1/ISI_VSYNC	2
PA31/TWCK0/UTXD1/ISI_HSYNC	K3	PA31/TWCK0/UTXD1/ISI_HSYNC	2

U3-F SAMA5D3x			
PD0/MCIO_CDA	K5	PD0/MCIO_CDA	2
PD1/MCIO_DA0	P1	PD1/MCIO_DA0	2
PD2/MCIO_DA1	K6	PD2/MCIO_DA1	2
PD3/MCIO_DA2	R1	PD3/MCIO_DA2	2
PD4/MCIO_DA3	L7	PD4/MCIO_DA3	2
PD5/MCIO_DA4/TIOA0/PWMH2	P2	PD5/MCIO_DA4/TIOA0/PWMH2	2
PD6/MCIO_DA5/TIOB0/PWML2	L8	PD6/MCIO_DA5/TIOB0/PWML2	2
PD7/MCIO_DA6/TCLK0/PWMH3	R2	PD7/MCIO_DA6/TCLK0/PWMH3	2
PD8/MCIO_DA7/PWML3	K7	PD8/MCIO_DA7/PWML3	2
PD9/MCIO_CK	U2	PD9/MCIO_CK	2
PD10/SPI0_MISO	K9	PD10/SPI0_MISO	2;6
PD11/SPI0_MOSI	M5	PD11/SPI0_MOSI	2;6
PD12/SPI0_SPCK	K10	PD12/SPI0_SPCK	2;6
PD13/SPI0_NPCS0	N4	PD13/SPI0_CS0	2;6
PD14/SCK0/SPI0_NPCS1/CANRX0	L9	PD14/SCK0/SPI0_NPCS1/CANRX0	2
PD15/CTS0/SPI0_NPCS2/CANTX0	N3	PD15/CTS0/SPI0_NPCS2/CANTX0	2
PD16/RTS0/SPI0_NPCS3/PWMF13	L10	PD16/RTS0/SPI0_NPCS3/PWMF13	2
PD17/RXD0	N5	PD17/RXD0	2
PD18/TXD0	M6	PD18/TXD0	2
PD19/ADTRG	T1	PD19/ADTRG	2
PD20/AD0	N2	PD20/AD0	2
PD21/AD1	M3	PD21/AD1	2
PD22/AD2	M2	PD22/AD2	2
PD23/AD3	L3	PD23/AD3	2
PD24/AD4	M1	PD24/AD4	2
PD25/AD5	N1	PD25/AD5	2
PD26/AD6	L1	PD26/AD6	2
PD27/AD7	L2	PD27/AD7	2
PD28/AD8	K1	PD28/AD8	2
PD29/AD9	K2	PD29/AD9	2
PD30/AD10	J1	PD30/AD10	2
PD31/AD11	J2	PD31/AD11	2

U3-E SAMA5D3x			
PC0/ETX0/TIOA3	D8	PC0/ETX0/TIOA3	2
PC1/ETX1/TIOB3	A4	PC1/ETX1/TIOB3	2
PC2/ERX0/TCLK3	E8	PC2/ERX0/TCLK3	2
PC3/ERX1/TIOA4	A3	PC3/ERX1/TIOA4	2
PC4/ETXEN/TIOB4	A2	PC4/ETXEN/TIOB4	2
PC5/ECRS0/TCLK4	F8	PC5/ECRS0/TCLK4	2
PC6/ERXER/TIOA5	B3	PC6/ERXER/TIOA5	2
PC7/EREFCK/TIOB5	G8	PC7/EREFCK/TIOB5	2
PC8/EMDC/TCLK5	B4	PC8/EMDC/TCLK5	2
PC9/EMDIO	F7	PC9/EMDIO	2
PC10/MCI2_CDA/LCDDAT20	A1	PC10/MCI2_CDA/LCDDAT20	2
PC11/MCI2_DA0/LCDDAT19	D7	PC11/MCI2_DA0/LCDDAT19	2
PC12/MCI2_DA1/TIOA1/LCDDAT18	C6	PC12/MCI2_DA1/TIOA1/LCDDAT18	2
PC13/MCI2_DA2/TIOB1/LCDDAT17	E7	PC13/MCI2_DA2/TIOB1/LCDDAT17	2
PC14/MCI2_DA3/TCLK1/LCDDAT16	B2	PC14/MCI2_DA3/TCLK1/LCDDAT16	2
PC15/MCI2_CK/PCK2/LCDDAT21	F6	PC15/MCI2_CK/PCK2/LCDDAT21	2
PC16/TK0	B1	PC16/TK0	2
PC17/TF0	E6	PC17/TF0	2
PC18/TD0	C3	PC18/TD0	2
PC19/RK0	D6	PC19/RK0	2
PC20/RF0	C4	PC20/RF0	2
PC21/RD0	D5	PC21/RD0	2
PC22/SPI1_MISO	C2	PC22/SPI1_MISO	2
PC23/SPI1_MOSI	G9	PC23/SPI1_MOSI	2
PC24/SPI1_SPCK	C1	PC24/SPI1_SPCK	2
PC25/SPI1_NPCS0	H10	PC25/SPI1_NPCS0	2
PC26/SPI1_NPCS1/TWD1/ISI_D11	H9	PC26/SPI1_NPCS1/TWD1/ISI_D11	2
PC27/SPI1_NPCS2/TWCK1/ISI_D10	D4	PC27/SPI1_NPCS2/TWCK1/ISI_D10	2
PC28/SPI1_NPCS3/PWMF10/ISI_D9	H8	PC28/SPI1_NPCS3/PWMF10/ISI_D9	2
PC29/URXD0/PWMF12/ISI_D8	G5	PC29/URXD0/PWMF12/ISI_D8	2
PC30/UTXD0/ISI_PCK	D3	PC30/UTXD0/ISI_PCK	2
PC31/FIQ/PWMF11	E4	PC31/FIQ/PWMF11	2

PROJECT TITLE		SAMA5D3x-CM	
SHEET TITLE		BUS INTERFACE	
FILE	SAMA5D3x-CM v2.0f.scm	SHEET NO	9 OF 9
SIZE	REV	DATE	DESCRIPTION FILE
A4		20.9.2012	
		DROWN	
		ISSUED	

## 5. Main Board (MB)

### 5.1 Main Board Overview

The SAMA5D3 series main board (MB) hosts any of the SAMA5D31/33/34/35/36 CPU module boards (CM). The main board features all necessary peripheral devices and interfaces for processor evaluation.

Figure 5-1. Main Board Top View

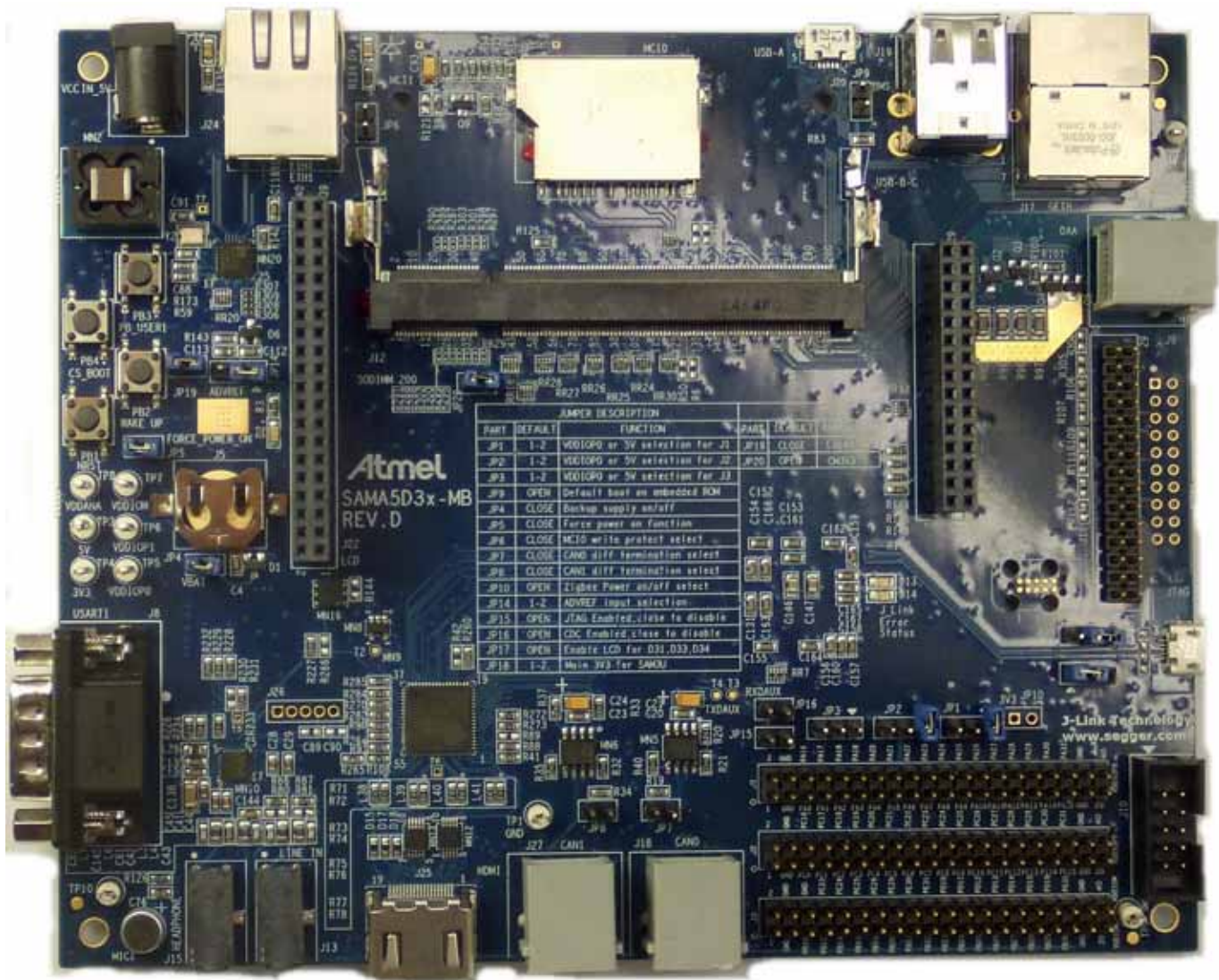
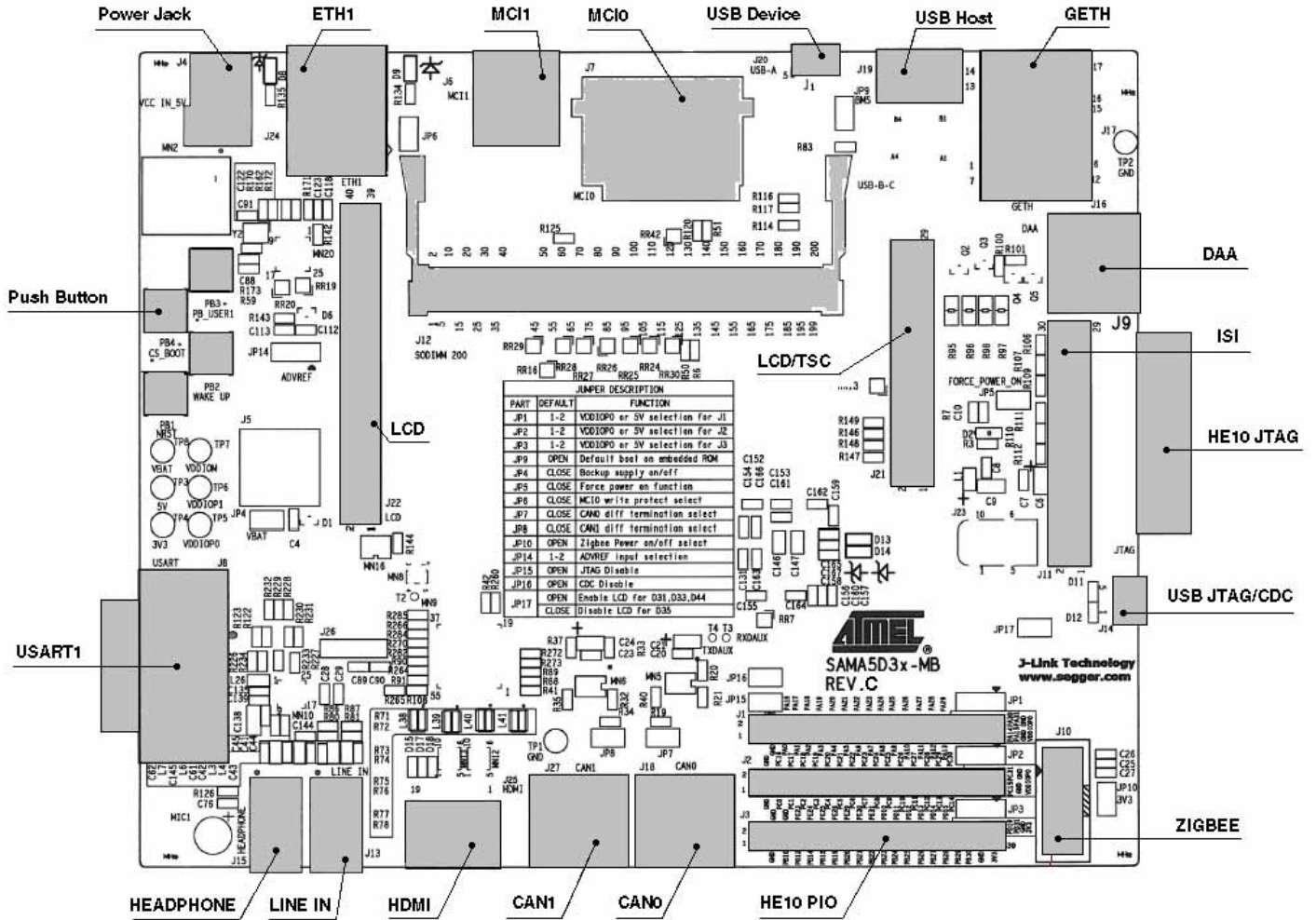


Figure 5-2. Annotated MB Layout



### 5.1.1 Equipment List

The SAMA5D3 series MB is a full-featured motherboard. It can be used with all available SAMA5D3 series CM boards.

### 5.1.2 Technical Specifications

**Table 5-1. MB Technical Specifications**

Characteristic	Specifications
Supported Module	All SAMA5D3 series computer modules
Expansion Slots	One 200-pin SODIMM socket
Mass Storage Interface	Two high-speed memory card hosts 1 x SD card slot (can also read MMC cards) 1 x micro SD card slot
I/O	3 x 20 pin header 1 x 20 + 1 x 15 pin header LCD connector 1 x 10 pin header ISI connector (Image Sensor) One 1-Wire EEPROM DS28EC20 One power LED
Communication	1 x Gigabit Ethernet 1 x 10/100 MHz Ethernet 2 x USB High-speed 2.0 Host 1 x USB High-speed 2.0 Host/Device 1 x USARTs, 1 x DBGU 2 x CAN connectors 1 x 10-pin header ZigBee connector 1 x Smart DAA (Softmodem interface)
Sound	Wolfson's 8904 Mic in, Headphone out signals
Video	1 x HDMI
LCD	LCD TFT Controller with overlay, alpha-blending, rotation, scaling and color space conversion
ISI	ITU-R BT. 601/656 Image Sensor Interface
Debug	1 x On-board SAM-ICE™ 1 x Bridge USB/UART DBGU
CMOS Battery	On-board Lithium Battery for CMOS backup
Power	System power: +5V DC +/-5% Backup: +1.65V to 3.6V DC
RoHS status	Compliant
CE and FCC Part 15 status	Compliant
Dimensions	165 * 135 * 20 mm

Note: Some of the features mentioned in the above feature summary table are optional. Check the article number of your module and compare it to the option information list on [Table 3-1 "Evaluation Kit Features"](#) of this user guide to determine which options are available with your particular module.

### 5.1.3 Devices

List of the MB board peripherals:

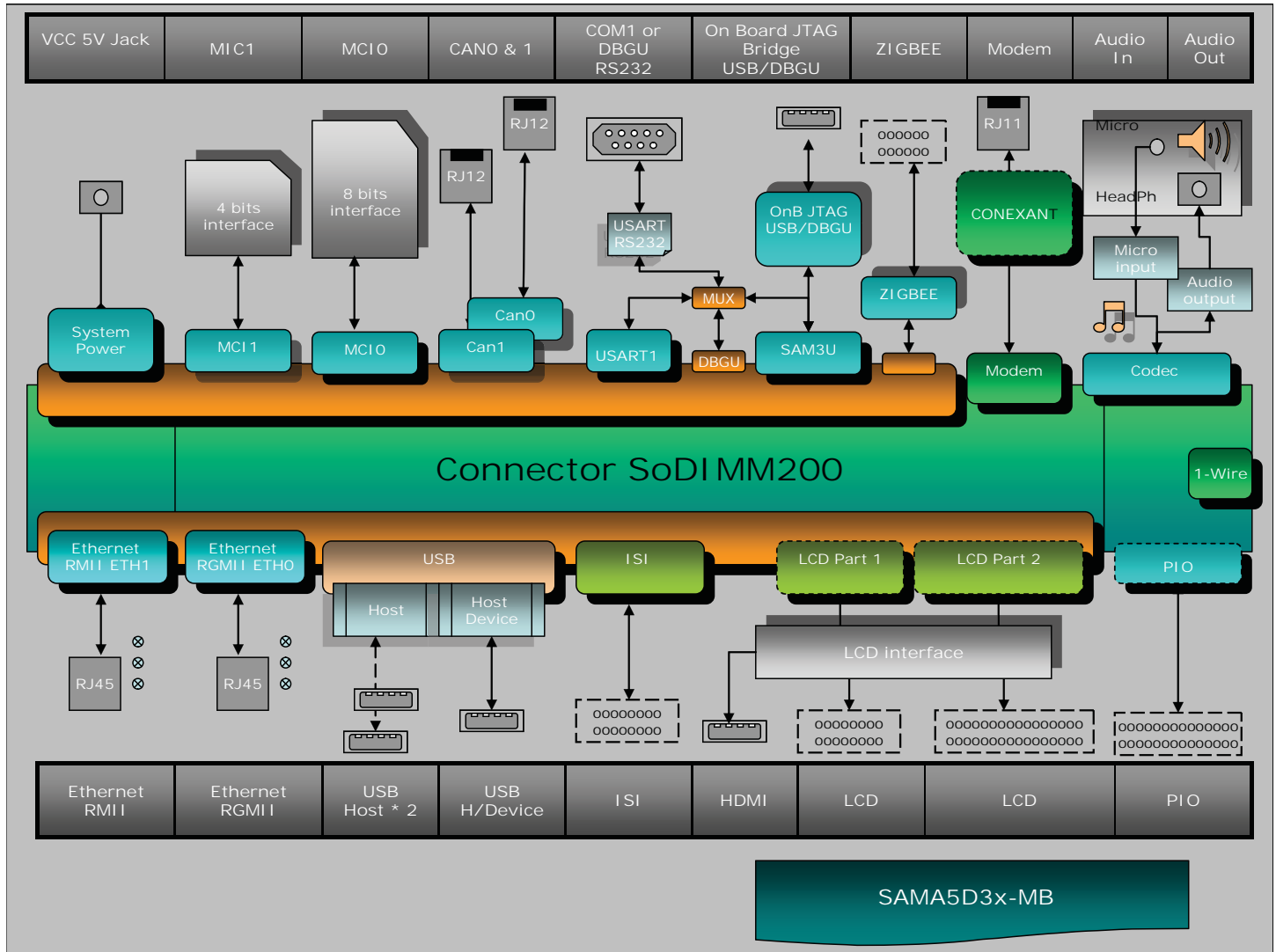
- Two EMAC PHY
- One audio CODEC
- Two high-speed MCI card interfaces
- Two CAN transceivers
- One RS232 port with level translator features USART1
- One Smart DAA port
- Two USB host ports
- One USB host/device port
- On-board power regulation
- LCD/ISI extension interface
- HDMI interface
- ZigBee® interface
- One-wire device

### 5.1.4 Board Interface Connection

- Main power supply (J4)
- 200 positions socket (as defined in SODIMM 200), 0.6mm pitch (J12)
- USB A Host/Device, support USB host/device using a micro AB connector (J20)
- USB B Host, support USB host using a type A connector (J19, upper)
- USB C Host, support USB host using a type A connector (J19, lower)
- USB-to-serial bridge on DBGU, and JTAG-OB functionality (J14)
- USART1 (RX, TX, RTS, CTS) connected to a 9-way male RS232 connector (J8)
- JTAG, 20-pin IDC connector (J9)
- MicroSD connector (J6)
- SD/MMC connector (J7)
- Gigabit Ethernet ETH0 (J17)
- Ethernet ETH1 (J24)
- Headphone (J15), line (J13)
- Image sensor connector (J11)
- HDMI connector (J25)
- Expansion connector with all LCD controller signals for DM board connection (QTouch, TFT LCD display with touchscreen and backlight (J21, J22))
- DAA connector RJ11 6P4C type (J16)
- CAN bus connectors RJ12 6P6C type (J18, J27)
- ZigBee connector (J10)
- Battery socket (J5)
- Three expansion connectors with PIO signals (J1, J2, J3)
- Test points; various test points are located throughout the board



Figure 5-3. MB Architecture

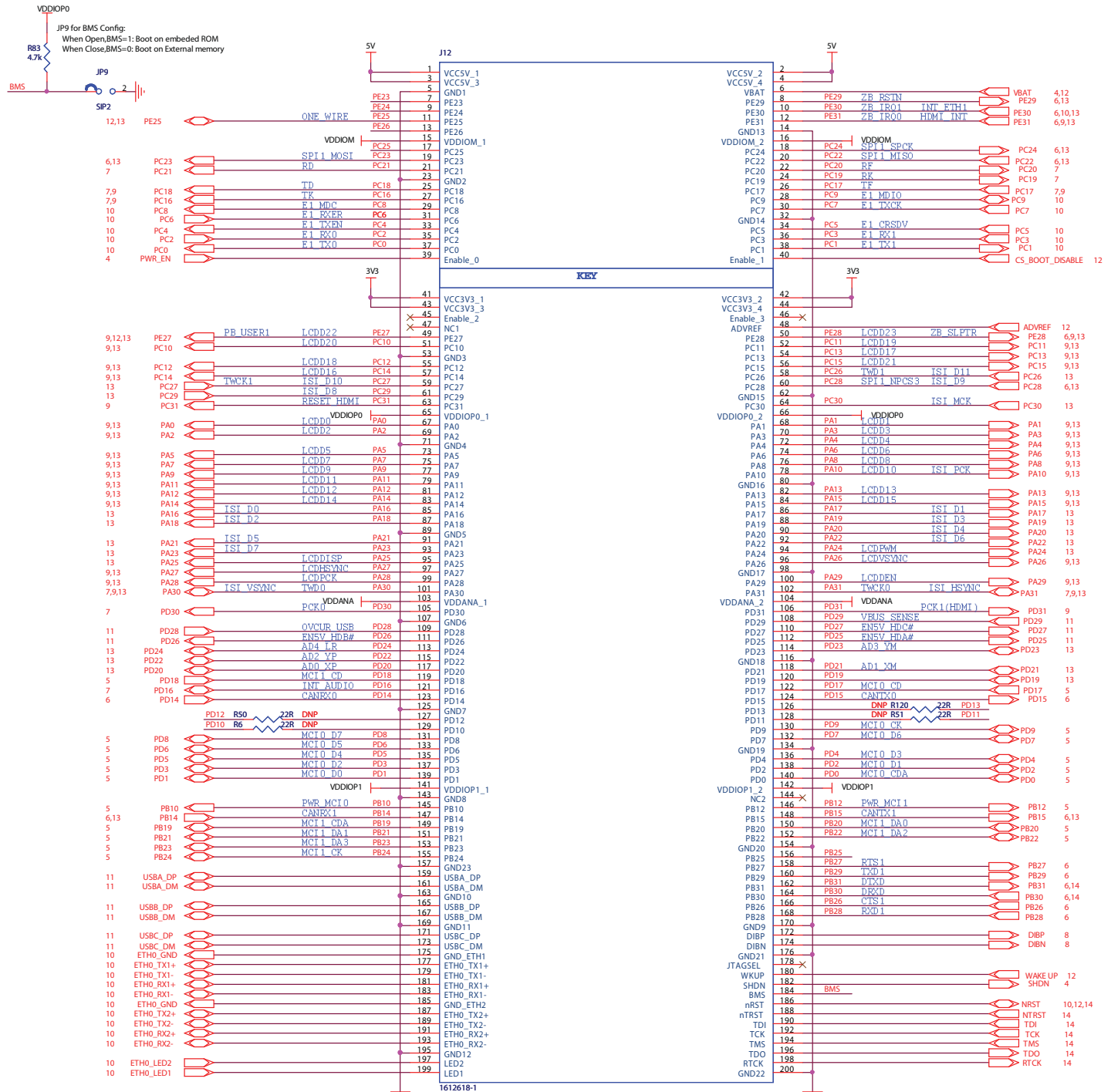


## 5.2 Function Blocks

### 5.2.1 Processor

The SAMA5D3 series MB board may be used with any of the SAMA5D31/D33/D34/D35/SAMA5D36 CPU modules.

Figure 5-4. SODIMM Interface on MB



## 5.2.2 Power Supplies

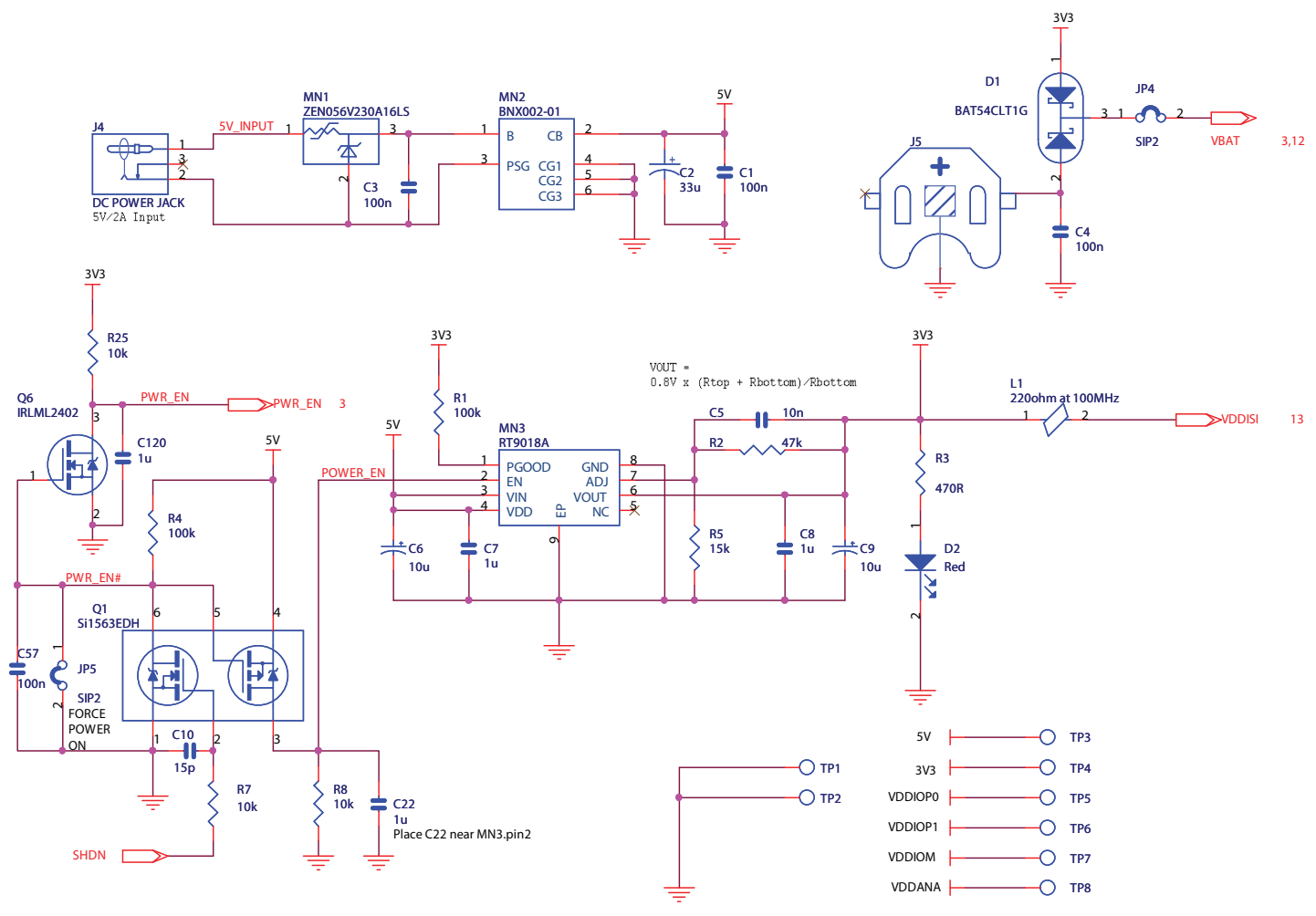
The SAMA5D3 series MB is supplied with a simple external 5 VCC power supply. The MB features one adjustable low-dropout regulator (LDO). It accepts DC in 5V power and outputs a regulated +3.3V to most other circuits on the board through four 3.3V rails.

### 5.2.2.1 Supply Group Configuration

The LDO is enabled through a dual FET scheme. The processor can assert SHDN (which is a VDDBU powered I/O) to shut down the LDO to enter backup mode. The regulators on the CM board are also shut down by the action of the SHDN signal.

If the 3V battery is mounted on J5, both the CM and the MB can be woken up by action on the BP2 button, which drives the WKUP signal that is also a VDDBU powered I/O.

Figure 5-5. MB Power Management



## 5.2.3 Debug JTAG/ICE and DBGU

The MB includes a built-in SEGGER J-Link-on-Board device. The functionality is implemented with an ATSAM3U4C microcontroller in an LQFP100 package.

The ATSAM3U4C provides the functions of JTAG and a bridge USB/Serial DBGU port.

Two LEDs D13 and D14 that are mounted on the main board signal the status of the J-Link-on-Board device.

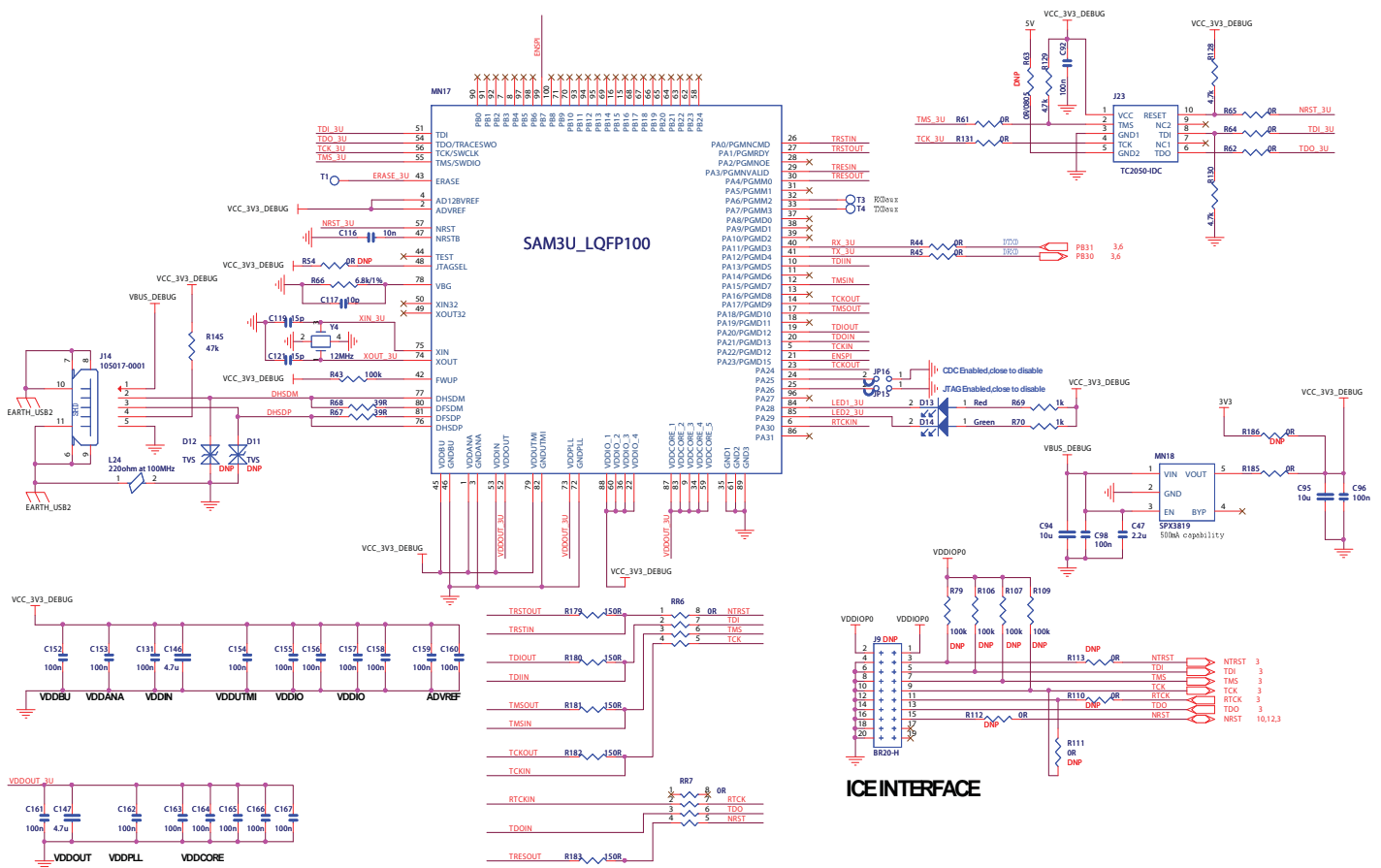
The J-Link-OB-ATSAM3U4C was designed in order to provide an efficient, on-board alternative to the general J-Link.

J-Link-OB-ATSAM3U4C supports the following target interfaces:

- JTAG
- DBGU

An optional 20-pin header is provided on the board to allow for the JTAG connection. In order to use this functionality, RR6 and RR7 must be removed and JP15 jumper must be in place.

Figure 5-6. MB JTAG-OB



### 5.2.3.1 Disabling J-Link-OB-ATSAM3U4C

Jumper JP15 disables the J-Link-OB-ATSAM3U4C JTAG functionality. When the jumper is installed, it grounds Pin 25 of the ATSAM3U4C that is normally pulled high. This signals to the microcontroller it must not provide JTAG support.

- Jumper JP15 not installed: J-Link-OB-ATSAM3U4C is enabled and fully functional
- Jumper JP15 installed: JTAG functionality is disabled

Jumper J15 disables only J-Link functionality. The debug serial port (DBGU) that is emulated through a communication device class (CDC) of the same USB connector remains operational.

The built-in JTAG controller does not have to be explicitly disabled to use an external JTAG controller through the 20-pin JTAG port. The internal J-Link-OB connects to a target only after it receives a first command; otherwise, it remains disabled.

### 5.2.3.2 Hardware UART via CDC

In addition to J-Link-OB functionality, the ATSAM3U4C microcontroller LAO provides a bridge to a debug serial port (DBGU) of the processor on a CM board. The port is made accessible over the same USB connection used by JTAG by implementing communication device class (CDC), which allows terminal communication with the target device.

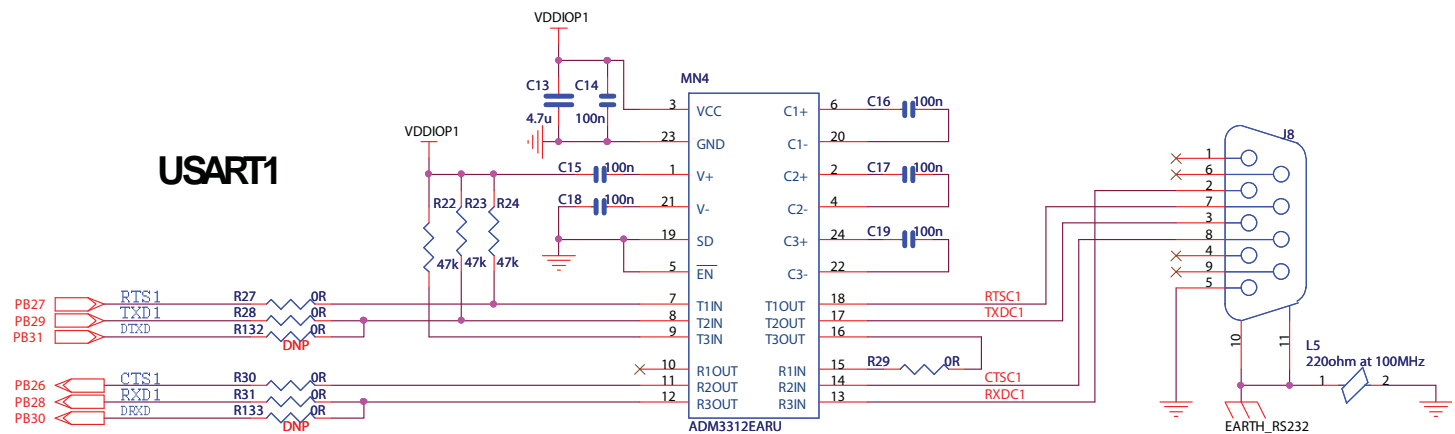
This feature is enabled only if the microcontroller Pin 24 is not grounded. The pin is normally pulled high and controlled by jumper JP16.

- Jumper JP16 not installed: the device is enabled
- Jumper JP16 installed: the CDC device is disabled

### 5.2.4 USART

The USART1 is used as a user serial communication port. This USART provides an RS-232 interface with transceiver TXD, RXD lines and hardware flow control CTS/RTS lines. The device uses a DB-9 male connector. The software must drive the appropriate PIO pins to enable the USART function.

Figure 5-7. USART1 Com Port



## 5.2.5 USB Ports

The SAMA5D3 series MB features three USB communication ports:

- Port A High-speed (EHCI) and full-speed (OHCI) host multiplexed with USB Device  
High-speed micro AB connector, J20
- Port B High-speed (EHCI) and full-speed (OHCI) host  
Standard type A connector, J19 upper port
- Port C Full-speed (OHCI) only host  
Standard type A connector, J19 lower port

All three USB host ports are equipped with 500 mA high-side power switch for self-powered and bus-powered applications. The USB device port feature VBUS insert detection function through the resistor ladder R138 and R139.

Refer to the embedded MPU product datasheet for detailed programming information, available on [www.atmel.com](http://www.atmel.com).

Figure 5-8. USB Port A

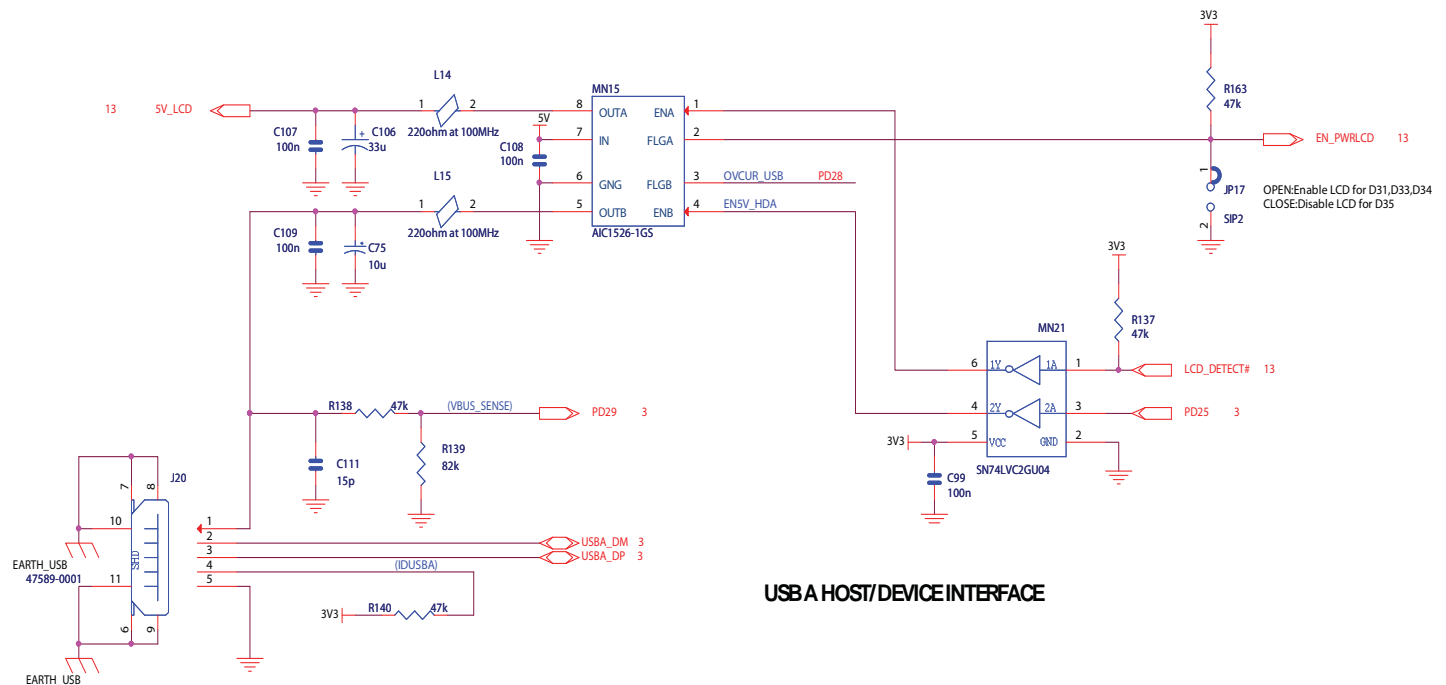
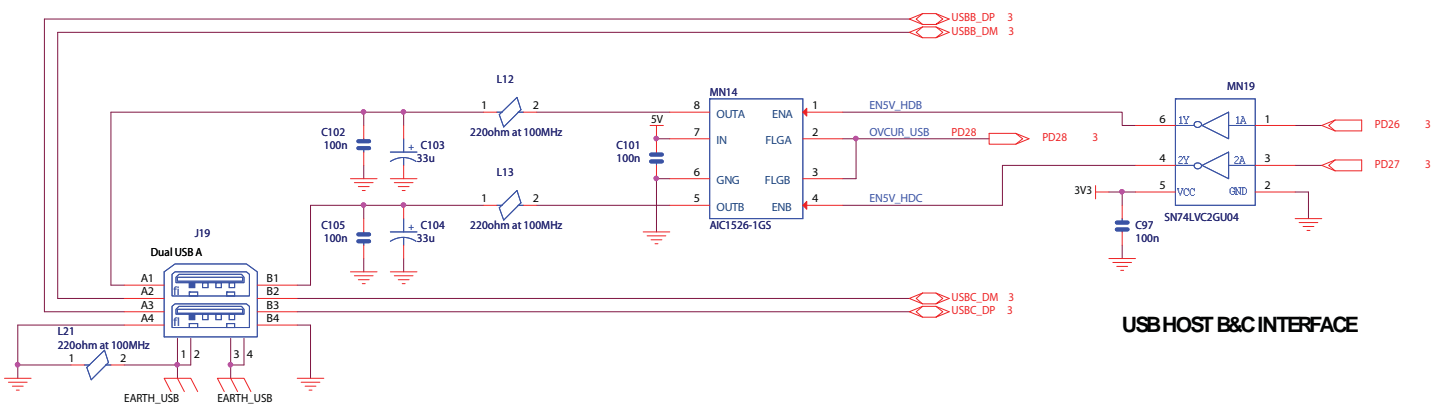


Figure 5-9. USB Ports B and C



## 5.2.6 Ethernet 10/100 (EMAC) Port

The main board contains a MICREL PHY device (KSZ8051) handling Ethernet connectivity at 10/100 Mbps. The device supports MII and RMII interface modes.

There are two independent PHY devices placed on CM and MB boards that connect to two separate RJ-45 connectors and that contain built-in magnetics and status LEDs. The LEDs are driven by PHY devices to indicate activity, link and speed status for the respective Ethernet ports.

Figure 5-10. ETH0 Port

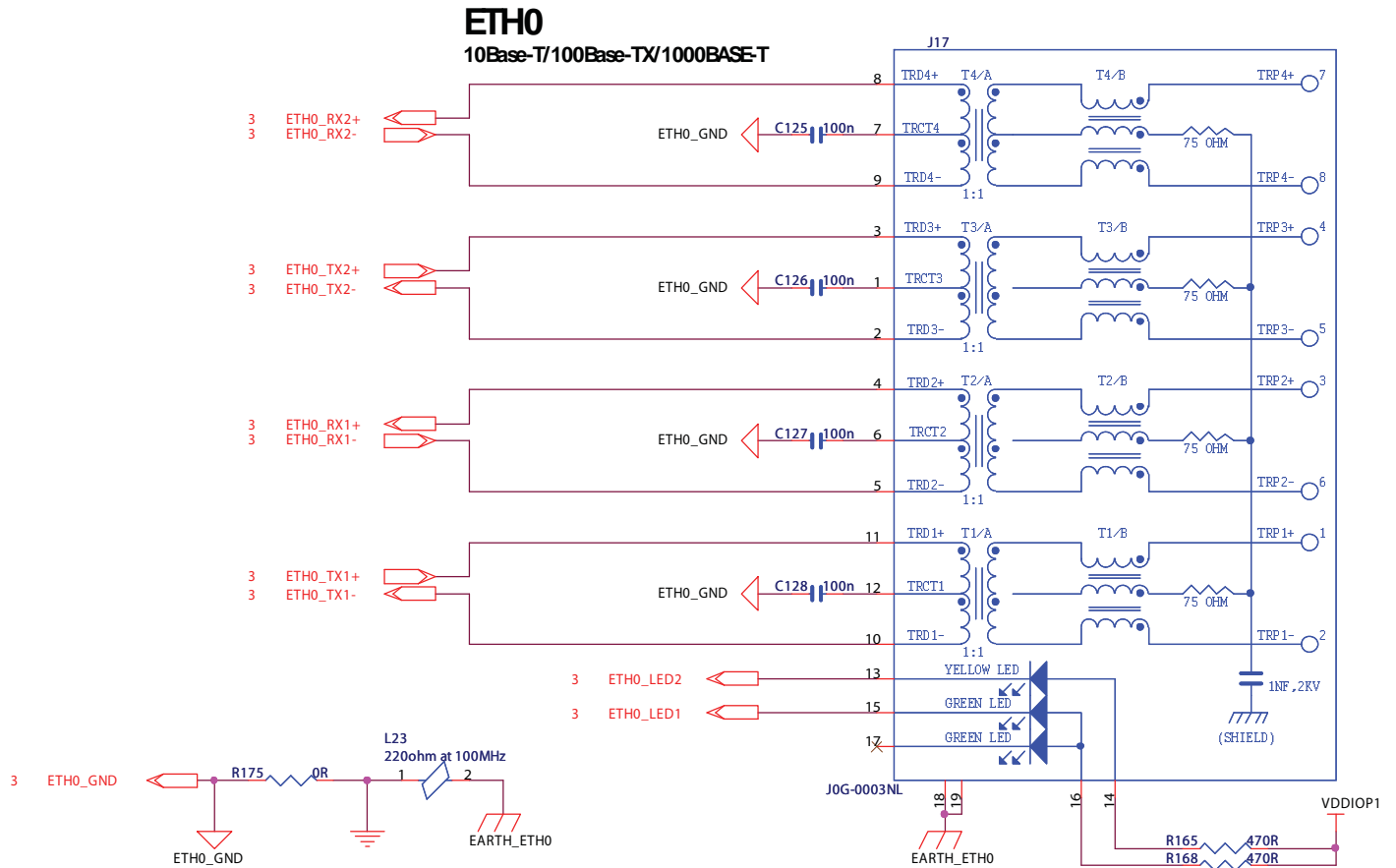
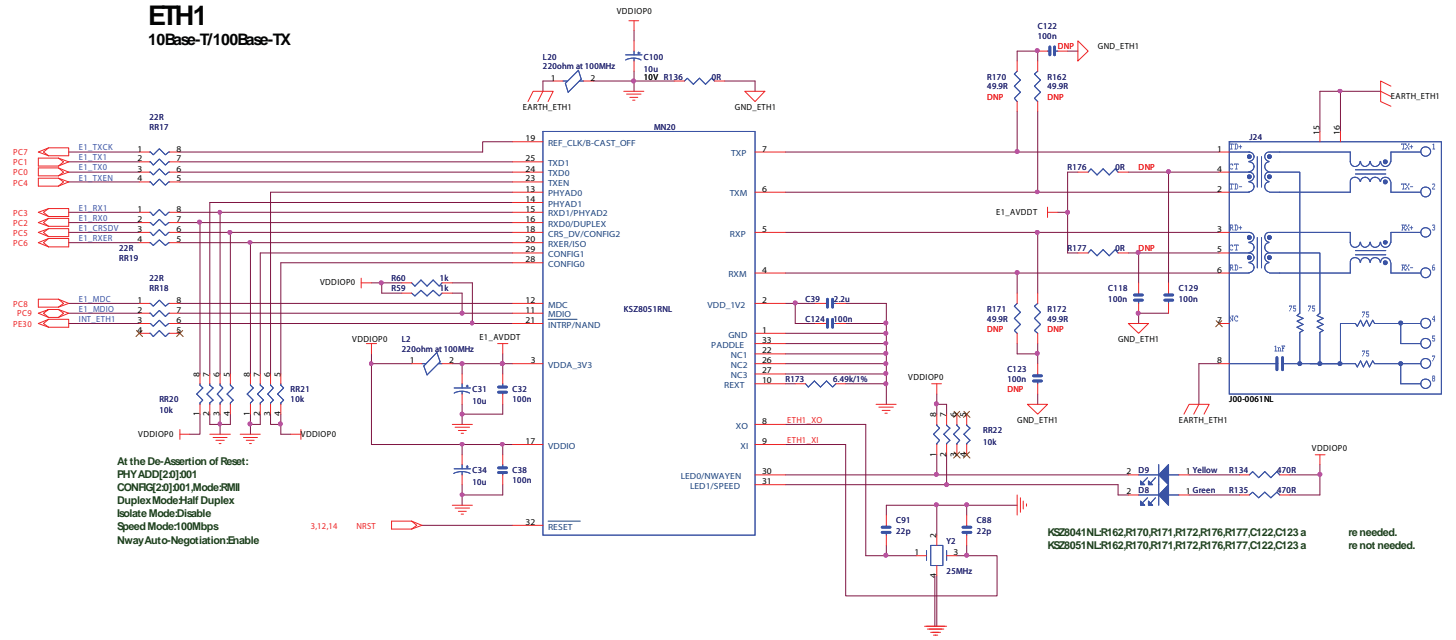


Figure 5-11. ETH1 Port





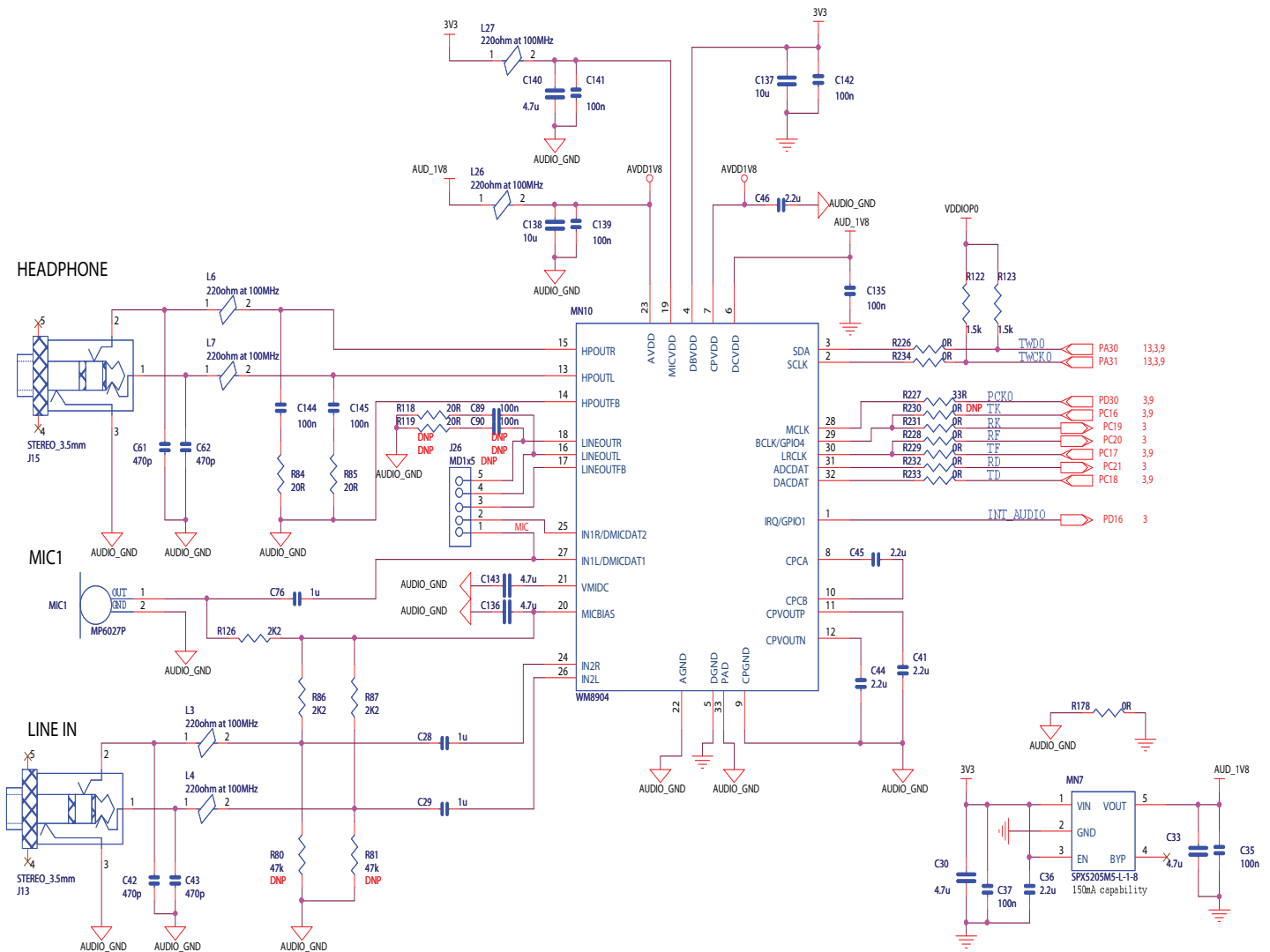
## 5.2.7 Audio

The MB includes a WM8904 CODEC that provides route to handle audio in the digital domain. The interface includes audio jacks for line input (J13) and headphone line output (J15). It also connects to an electret microphone, which is conveniently installed on the main board.

This interface can be used to play and record audio. The WM8904 chip has left and right channel line inputs, a microphone input and an on-board microphone, as well as a left and right headphone output. The line in and headphones can be connected through two 2.5 mm J13 and J15 audio jacks. A stereo microphone input (or a second left/right line input) and left/right line outputs are connected to a 5-pin header (J26). The header is not installed normally.

The SAMA5D3 series processor is configured in IIS slave mode to interface with the WM8904 CODEC.

Figure 5-12. Audio Interface



## 5.2.8 HDMI Transmitter Interface

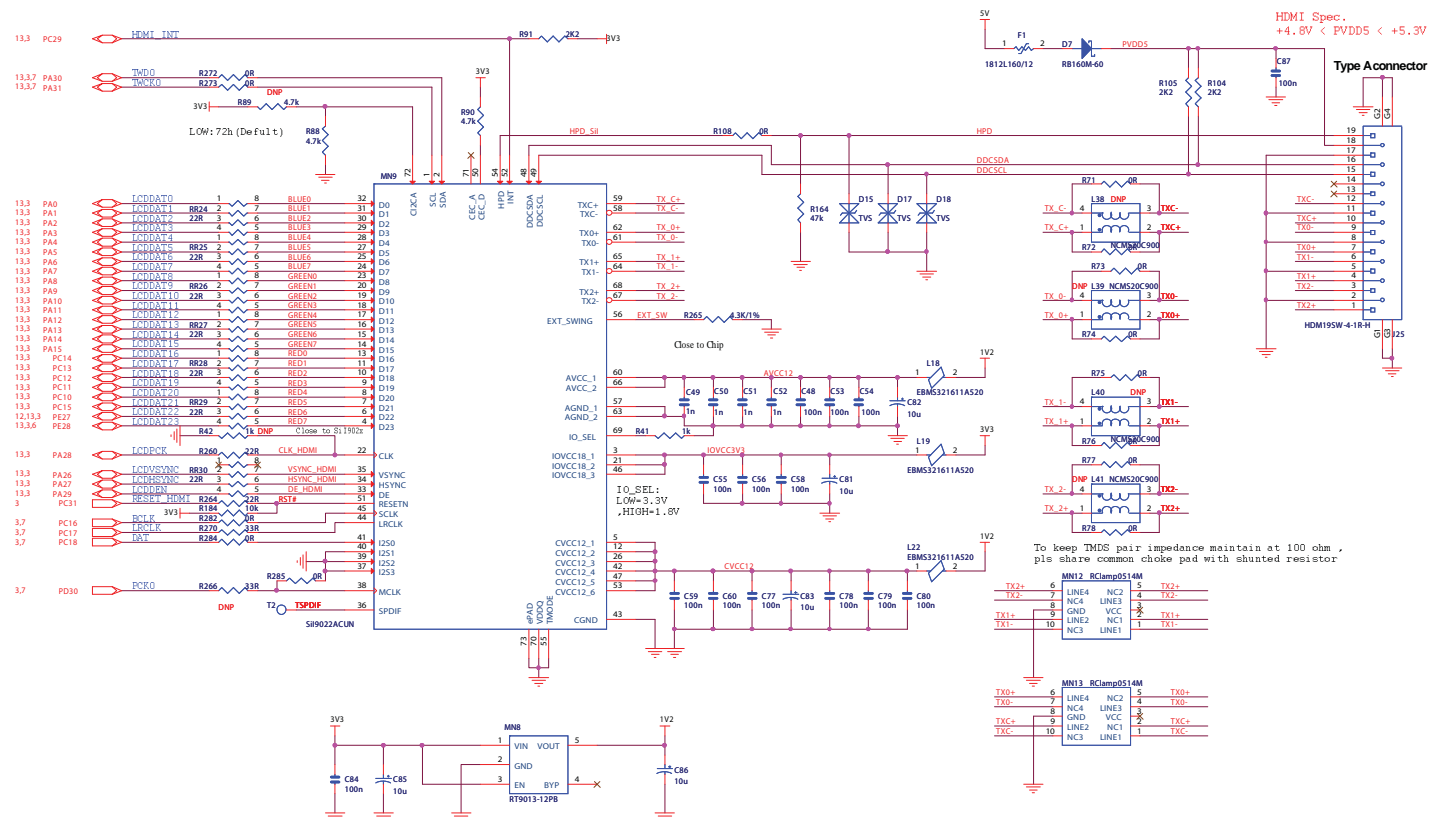
The Main Board (MB) is equipped with an HDMI transmitter interface.

The SiI9022/9024 HDMI Tx provides a complete solution for transmitting HDMI compliant digital audio/video. Specialized audio/video processing is available within the transmitter to easily and cost-effectively add HDMI capability to consumer electronics devices.

The user must use an HDMI cable to connect to a monitor. This cable is not provided with the SAMA5D3 series-EK. A standard HDMI cable can be used.

**Important:** Do not plug in the HDMI connector to a display with the evaluation kit powered on. Be certain that the EK board is not powered, plug in the cable to the display and then power on the SAMA5D3 series EK board.

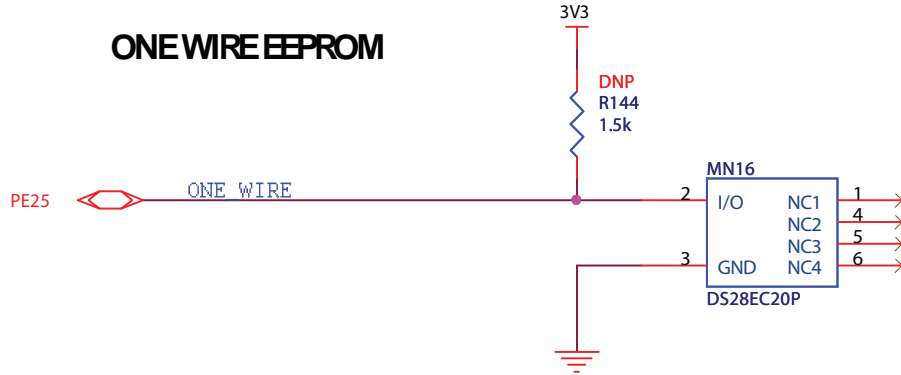
Figure 5-13. HDMI Interface



## 5.2.9 1-Wire EEPROM

The MB also features a 1-wire device as a “software identification label” to store information such as chip type, manufacture name, production date, etc.

Figure 5-14. 1-Wire on MB

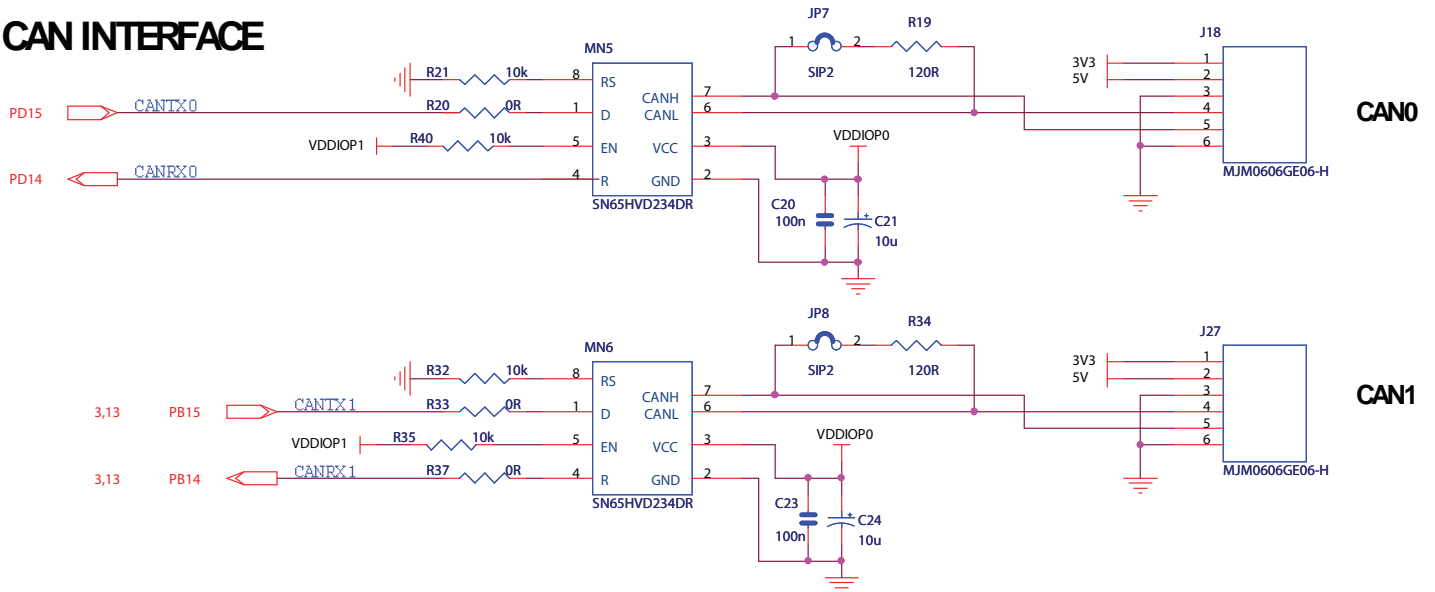


## 5.2.10 CAN Bus

The MB offers two CPU-controlled Controller Area Network (CAN) interfaces with transceivers available through connectors J18 and J27.

Figure 5-15. CAN on MB

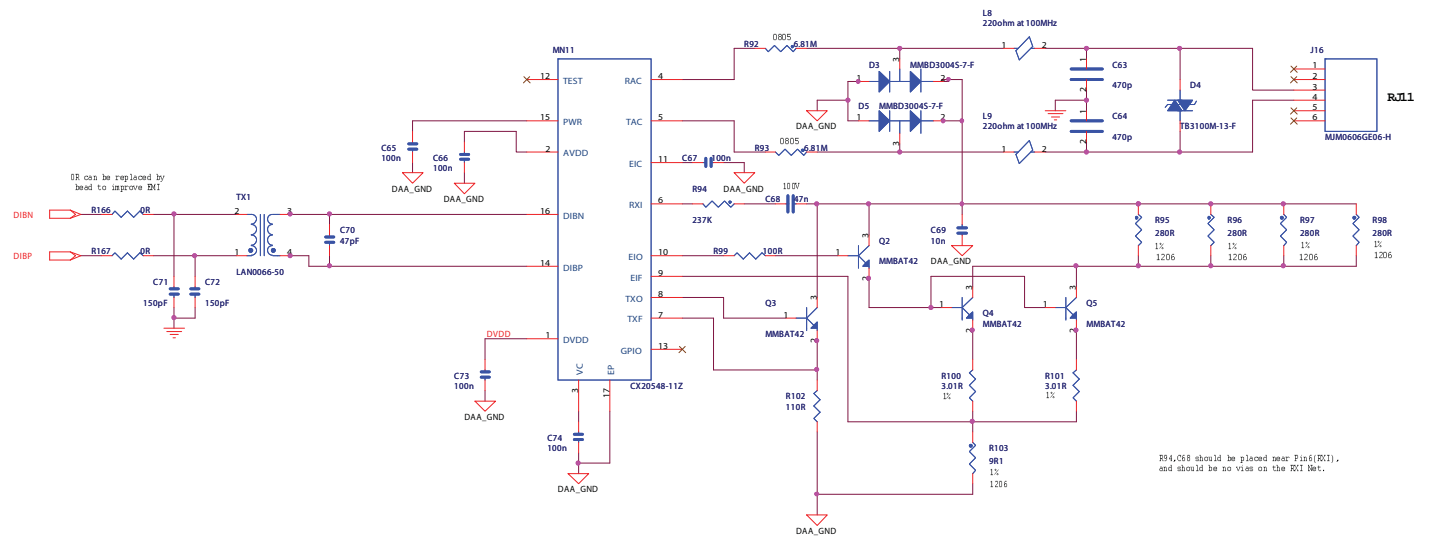
### CAN INTERFACE



## 5.2.11 Smart DAA

The SAMA5D3 series MB features a Smart DAA chip to drive an analog telephone line on RJ11 6P4C port (J16).

Figure 5-16. Smart DAA



## 5.2.12 SD/MMC Interface

SD/MMC is a standard Secure Digital/MultiMedia Card interface.

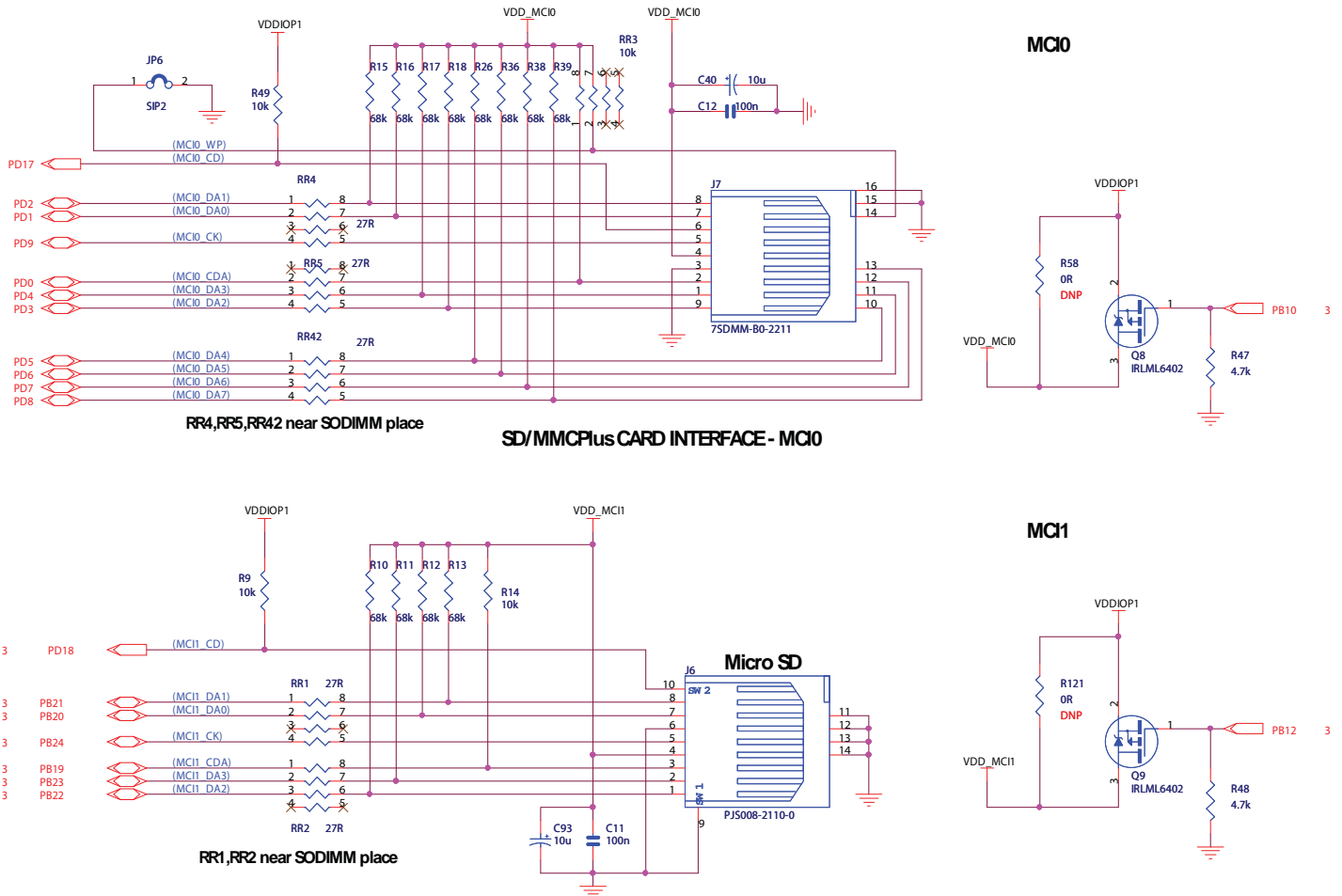
The MB has two high-speed Multimedia Card Interfaces (MCI).

- The first interface is used as an 8-bit interface (MCI0), connected to an SD/MMC card slot.
- The second interface is used as a 4-bit interface (MCI1), connected to a MicroSD card slot.

Each power line is on by default and is connected to a MOSFET controlled by a PIO to switch on or off the SD card power.

Note: The power is connected to VCC, which is 3.3V.

Figure 5-17. SD/MMC Interface



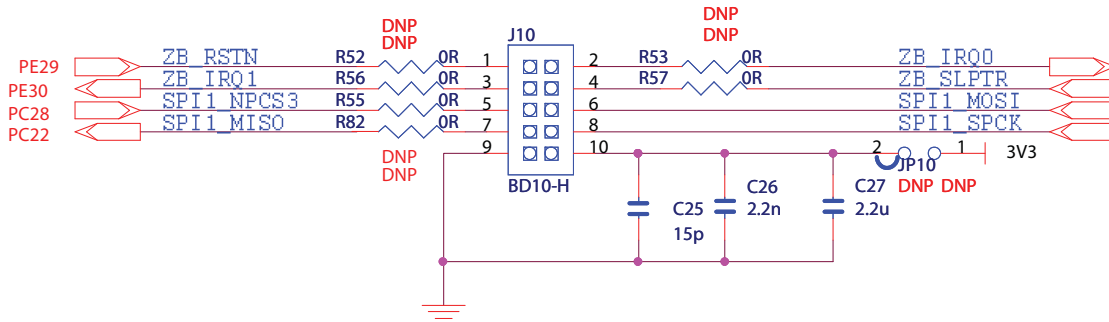
### 5.2.13 ZigBee

The MB has a 10-pin male connector for the Atmel RZ600 ZigBee module.

Not populated (DNP) 0 Ohm resistors have been implemented in series with the PIO lines that are used elsewhere in the design. This ensures that in case of a conflict in the user application, the lines can be disconnected individually.

Figure 5-18. ZigBee Interface

#### ZIGBEE INTERFACE



### 5.2.14 LED Indicators

The main board has one red LED (D2) that is on when the board is powered.

There are two additional LEDs on the main board that are associated with on-board JTAG port. See [Section 5.2.3 “Debug JTAG/ICE and DBGU”](#).

### 5.2.15 Pushbutton Switches

- One reset, board reset (BP1)
- One wake-up, pushbutton to bring the processor out of low-power mode (BP2)
- One user momentary pushbutton
- One boot memory Chip Select (CS), disabling the pushbutton (refer to [Section 4.2.4.1 “Boot Configuration”](#)).

#### 5.2.15.1 Reset

When pressed and released, this pushbutton causes a power-on reset of the SAMA5D3 series EK (MB, CM and DM boards).

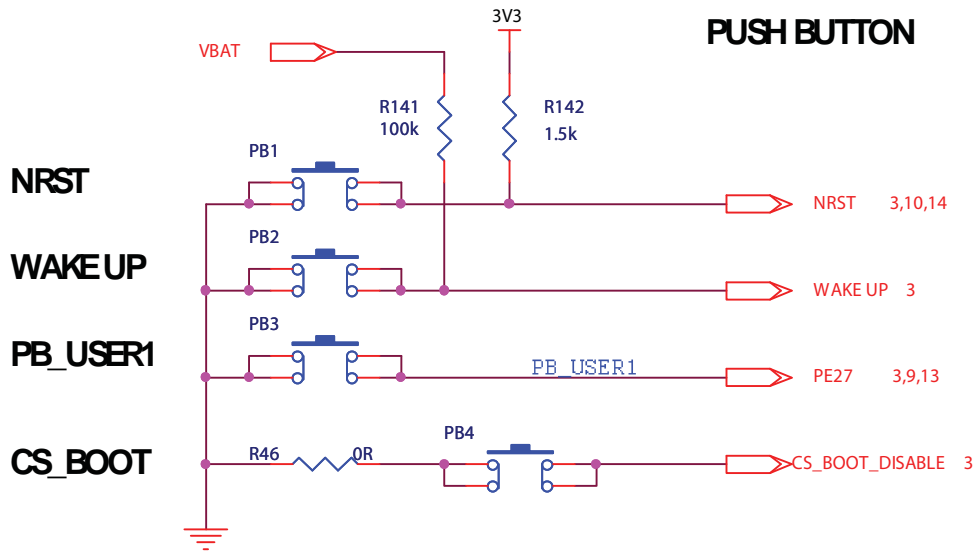
### 5.2.15.2 CS\_BOOT Button

The CS\_BOOT can be used to prevent the system from booting out of external memories (NANDFlash, SPI Flash). The purpose is mainly to execute the SAM-BA part of the ROM code.

Two methods can be used:

1. Press the CS\_BOOT and power-cycle the board.
2. Press the CS\_BOOT and then press the NRST button.

Figure 5-19. Pushbutton

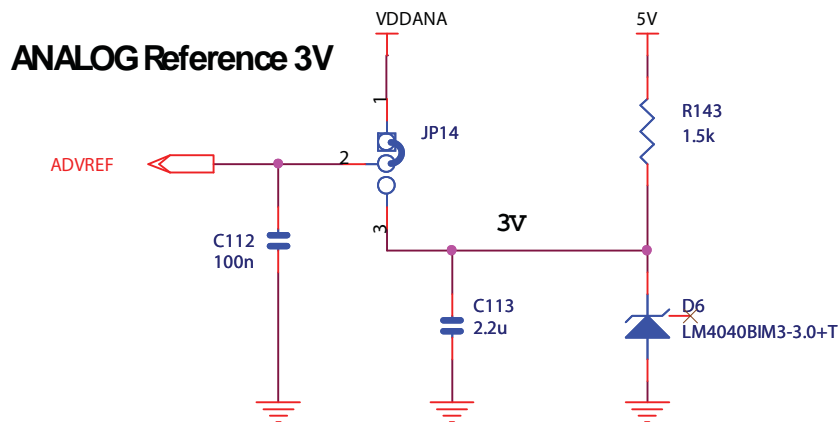


### 5.2.16 Analog Reference

The 3V voltage reference is based on an LM4040 (Precision Micropower Shunt Voltage Reference).

This ADVREF level can be set as 3V or 3.3V via the jumper JP14.

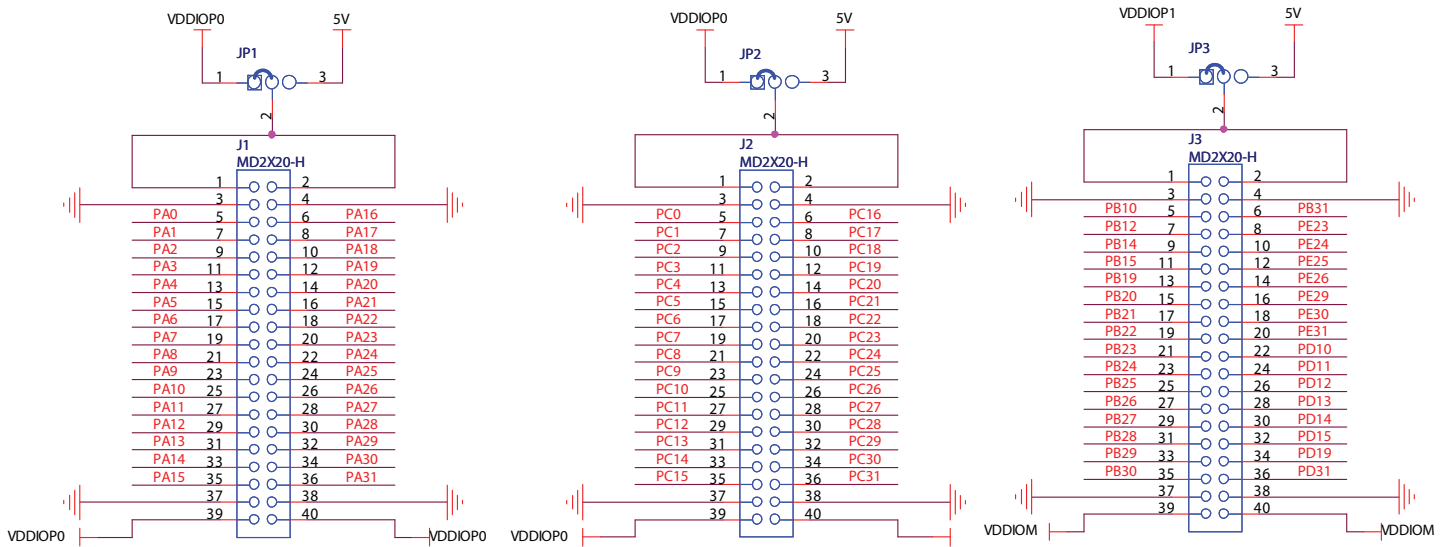
Figure 5-20. Analog Reference



## 5.2.17 Expansion Ports

Three 40-pin headers (J1, J2, J3) are provided on the board to allow for the PIO connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin.

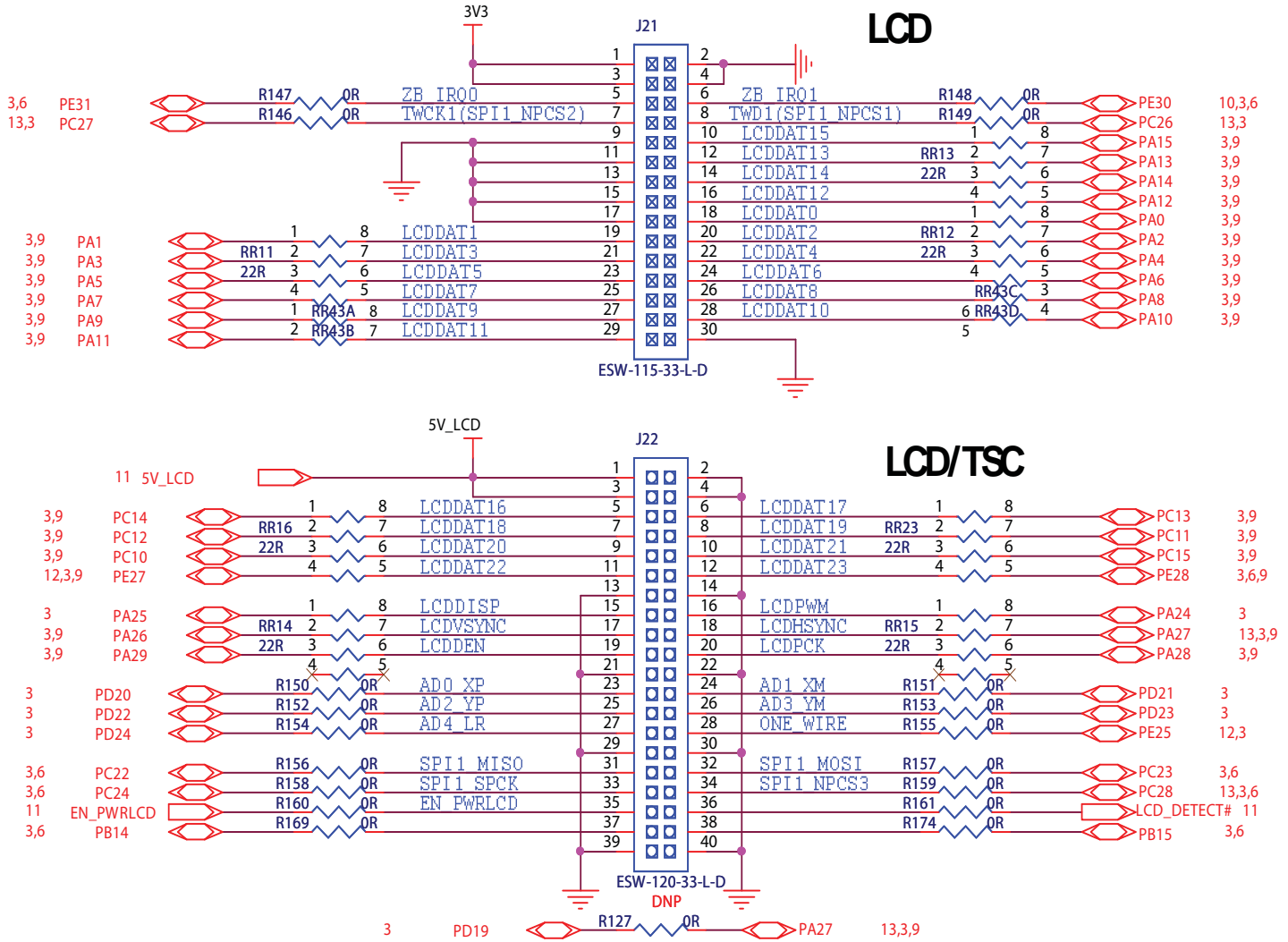
Figure 5-21. I/O Expansion



Two connectors (J21, J22) are provided on-board to interface the optional LCD and touchscreen display module (DM) board.

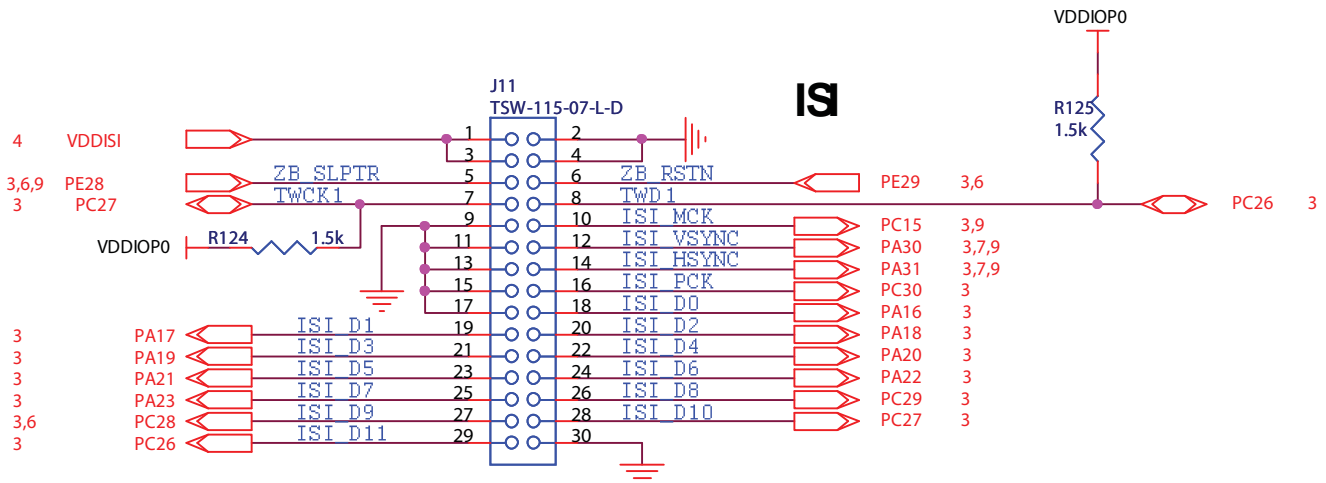


Figure 5-22. LCD Expansion



All I/Os of the SAMA5D3 series Image Sensor Interface (ISI) are routed to connectors J11.

Figure 5-23. ISI Expansion



## 5.3 Configuration

Table 5-2 describes the PIO usage, the jumpers, the test points and the solder drops of a SAMA5D3 series EK board.

**Table 5-2. Jumpers and Solderdrops**

Reference	Default	Function
JP1	1-2	VDDIOP0 or 5V selection for J1
JP2	1-2	VDDIOP0 or 5V selection for J2
JP3	1-2	VDDIOP0 or 5V selection for J3
JP4	CLOSE	Backup supply on/off
JP5	CLOSE	Force power on function
JP6	CLOSE	MCI0 write protect select
JP7	CLOSE	CAN0 diff termination select
JP8	CLOSE	CAN1 diff termination select
JP9	OPEN	Default boot on embedded ROM, close boot on external memory
JP10	OPEN	ZigBee power on/off select
JP11	—	
JP12	—	
JP13	—	
JP14	1-2	ADVREF input selection
JP15	OPEN	JTAG enable
JP16	OPEN	CDC enable
JP17	OPEN	Enable LCD for D31, D33, D34
	CLOSE	Disable LCD for D35
JP18	1-2	SAM3U powered by main 3V3

**Table 5-3. Default Not Populated Parts**

Page	Reference	Function
3	R6,R51,R50,R120	Optional PD10, PD11, PD12, PD13 from MB
5	R58	Optional for MCI0 power supply mode
	R121	Optional for MCI1 power supply mode
6	R52,R53,R55,R56,R57,R82,JP10	Optional ZigBee
	R132,R133	Debug or USART1 option
7	C89,C90,R118,R119,J26	Optional Audio Line out, MIC in
	R80,R81	Optional MIC level setting
	R230	Optional audio TK
9	L38,L39,L40,L41	Optional HDMI EMI filter
	R89	HDMI chip I2C address setting
	R266	Optional for I2S PCLK
	R42	Optional for LCD PCLK

**Table 5-3. Default Not Populated Parts**

Page	Reference	Function
10	R162,R170,R171,R172,R176,R177,C122,C123	Optional for KSZ8041NL
12	R144	Optional pull up for DS28EC20P
13	R127	Optional for ADC trigger
14	R79,R106,R107,R109,R113,R110,R112,R111,J9	Optional JTAG
	R54	SAM3U JTAG selection
	R63	5V option
	D11,D12	USB ESD protect option
	R186	Main 3V3 optional for VCC_3V3_DEBUG

## 5.4 PIO Usage and Interface Connectors Details

### 5.4.1 Power Supply

Figure 5-24. Power Supply Connector J4

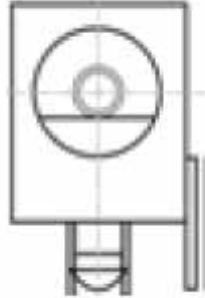


Table 5-4. Power Supply Connector J4 Signal Description

Pin	Mnemonic	Signal Description
1	Center	+5V
2		GND
3		Floating

## 5.4.2 JTAG/ICE Connector

Figure 5-25. JTAG J9

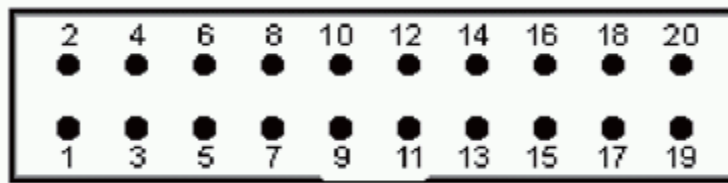


Table 5-5. JTAG/ICE Connector J9 Signal Descriptions

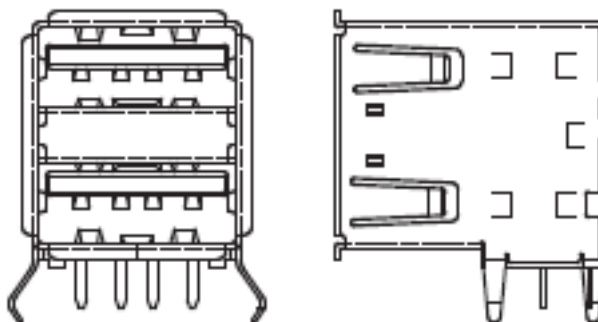
Pin	Mnemonic	Signal Description
1	VTref 3.3V power	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from VDD on the target board and must not have a series resistor.
2	Vsupply 3.3V power	This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to VDD or leave open in target system.
3	nTRST Target Reset - Active-low output signal that resets the target.	JTAG Reset. Output from SAM-ICE to the Reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled High on the target to avoid unintentional resets when there is no connection.
4	GND	Common ground
5	TDI Test Data Input - Serial data output line, sampled on the rising edge of the TCK signal.	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Common ground
7	TMS Test Mode Select.	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Common ground
9	TCK Test Clock - Output timing signal, for synchronizing test logic and control register access.	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.
10	GND	Common ground
11	RTCK - Input Return Test Clock signal from the target.	Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
12	GND	Common ground
13	TDO JTAG Test Data Output - Serial data input from the target.	JTAG data output from target CPU. Typically connected to TDO on target CPU.
14	GND	Common ground
15	nSRST RESET	Active-low reset signal. Target CPU reset signal.

**Table 5-5. JTAG/ICE Connector J9 Signal Descriptions**

Pin	Mnemonic	Signal Description
16	GND	Common ground
17	RFU	This pin is not connected in SAM-ICE.
18	GND	Common ground
19	RFU	This pin is not connected in SAM-ICE.
20	GND	Common ground

### 5.4.3 USB Type A Dual Port

**Figure 5-26. USB Type A Dual Port J19**



**Table 5-6. USB Type A Dual Port J19 Signal Descriptions**

Pin	Mnemonic	PIO	Signal Description
A1	Vbus - USB_A		5V power
A2	DM - USB_A		Data minus
A3	DP - USB_A		Data plus
A4	GND		Common ground
B1	Vbus - USB_A		5V power
B2	DM - USB_A		Data minus
B3	DP - USB_A		Data plus
B4	GND		Common ground
Mechanical pins			Shield

#### 5.4.4 USB MicroAB

Figure 5-27. USB Host/Device MicroAB Connector J20

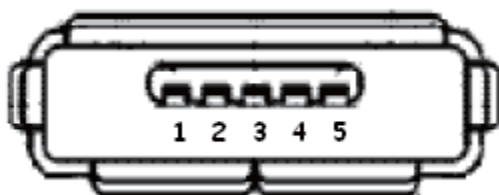


Table 5-7. USB Host/Device Micro AB Connector J20 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	Vbus		5V power
2	DM		Data minus
3	DP		Data plus
4	ID		On the Go identification
5	GND		Common ground

#### 5.4.5 JTAG OB USB MicroAB

Figure 5-28. USB JTAG OB MicroAB connector J14

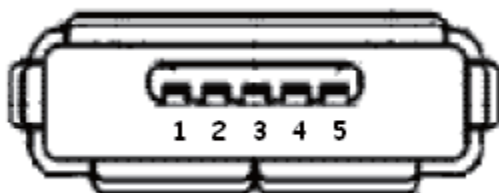


Table 5-8. USB JTAG OB MicroAB connector J14 Signal Descriptions

Pin	Mnemonic	PIO	Signal description
1	Vbus		5V power
2	DM		Data minus
3	DP		Data plus
4	ID		On the Go Identification
5	GND		Common ground

## 5.4.6 HDMI Connector

Figure 5-29. HDMI Female Type A Connector J25

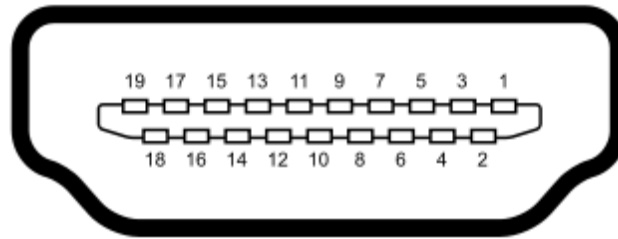


Table 5-9. HDMI Type A Female Connector J25

LCD	Pin Num		LCD
TMDS Data 2+	1	2	TMDS Data 2 Shield
TMDS Data 2-	3	4	TMDS Data 1+
TMDS Data 1 Shield	5	6	TMDS Data 1-
TMDS Data 0+	7	8	TMDS Data 0 Shield
TMDS Data 0-	9	10	TMDS Clock +
TMDS Clock Shield	11	12	TMDS Clock -
NC	13	14	NC
SCL	15	16	SDA
GND	17	18	+5V
Hot Plus Detect	19		



## 5.4.7 RS232 Connector with RTS/CTS Handshake Support

Figure 5-30. USART1 Connector J8

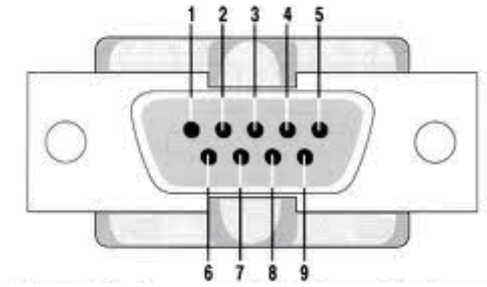
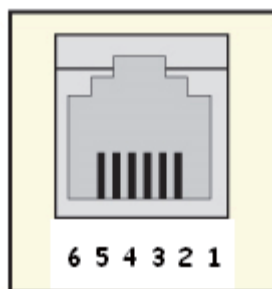


Table 5-10. USART Connector J8 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1, 4, 6, 9			No connection
2	RXD (Received Data)	PB28	RS232 serial data output signal
3	TXD (Transmitted Data)	PB29	RS232 serial data input signal
5	GND		Common ground
7	RTS (Request To Send)	PB27	Active-positive RS232 input signal
8	CTS (Clear To Send)	PB26	Active-positive RS232 output signal
Mechanical pins			Shield

## 5.4.8 DAA RJ11 Socket (6P4C)

Figure 5-31. DAA RJ11 Socket J16

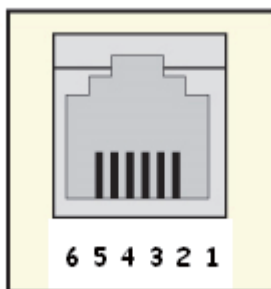


**Table 5-11. DAA RJ11 Socket J16 Signal Descriptions**

Pin	Mnemonic	Signal Description
1, 2, 5, 6		No connection
3	RAC	RING side of ordinary telephone line
4	TAC	TIP side of ordinary telephone line

#### 5.4.9 CAN RJ12 Socket (6P6C)

**Figure 5-32. CAN RJ12 Socket J18, J27**



**Table 5-12. CAN RJ12 Socket Signal Descriptions**

Pin	Mnemonic	Signal Description
1	3V3	Power pin
2	5V	Power pin
4	CANL	CAN bus differential pair
5	CANH	CAN bus differential pair
3, 6	GND	Common ground

## 5.4.10 SD/MMC Plus MCI0

Figure 5-33. SD Socket J7

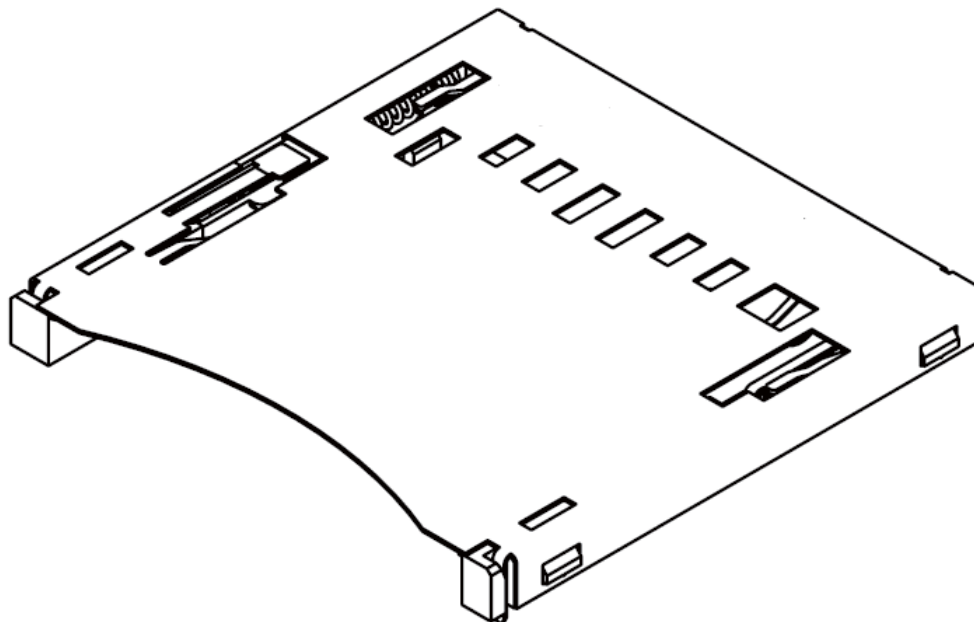


Table 5-13. MicroSD Socket J7 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT3	PD4	Data bit
2	CMD	PD0	Command line
3	VSS		Command line
4	VCC		Supply voltage 3.3V
5	CLK	PD9	Clock / command line
6	CD	PD17	Card detect
7	DAT0	PD1	Data bit
8	DAT1	PD2	Data bit
9	DAT2	PD3	Data bit
10	DAT4	PD5	Data bit
11	DAT5	PD6	Data bit
12	DAT6	PD7	Data bit
13	DAT7	PD8	Data bit
14	WP	JP6	Protect
15		VSS	Common ground
16		VSS	Common ground

## 5.4.11 MicroSD MCI1

Figure 5-34. MicroSD Socket J6

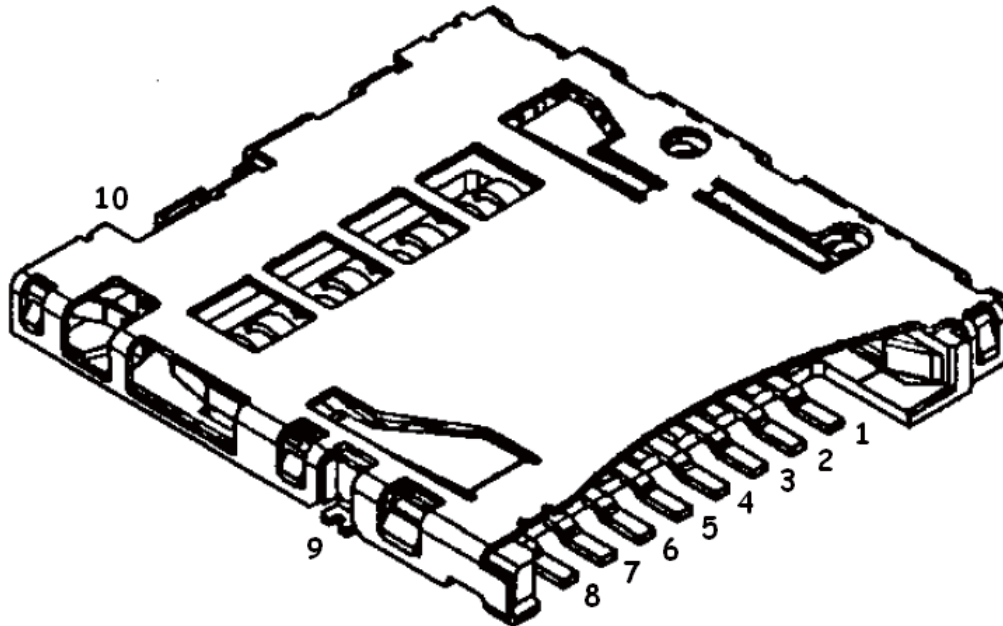
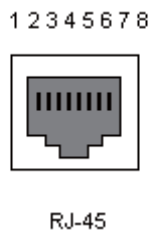


Table 5-14. MicroSD Socket J6 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT2	PB22	Data bit 2
2	CD/DAT3	PB23	Card detect / data bit 3
3	CMD	PB19	Command line
4	VCC		Supply voltage 3.3V
5	CLK	PB24	Clock / command line
6	VSS		Common ground
7	DAT0	PB20	Data bit 0
8	DAT1	PB21	Data bit 1
9	SW1		Not used, grounded
10	CARD DETECT	PD18	Card detect

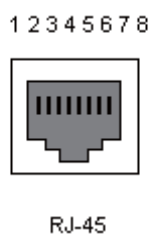
## 5.4.12 Gigabit Ethernet ETH0 RJ45 Socket J17

Figure 5-35. Gigabit Ethernet RJ45 Socket J17



## 5.4.13 Ethernet ETH1 RJ45 Socket J24

Figure 5-36. Ethernet RJ45 Socket J24



## 5.4.14 ZigBee Socket J10

Figure 5-37. ZigBee Socket J10

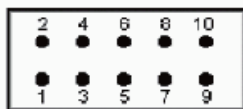


Table 5-15. ZigBee Socket J10 Signal Descriptions

Function	Signal Name	Port	Pin	Pin	Port	Signal Name	Function	Option on Misc. Port Set by OR or Solder Shunts
Reset	/RST		1	2		Misc.	EEPROM for MAC address, cap array settings and serial number TST: test mode activation CLKM: RF chip clock output	
Interrupt Request	IRQ		3	4		SLP_TR	SLP_TR	
SPI chip select	/SEL		5	6		MOSI	SPI MOSI	
SPI MISO	MISO		7	8		SCLK	SPI CLK	
Power Supply	GND	GND	9	10	VCC	VCC	VCC	Voltage range: 1.8V to 5.5V, regulated to 3.3V

## 5.4.15 LCD Socket J21

Figure 5-38. LCD Socket J21

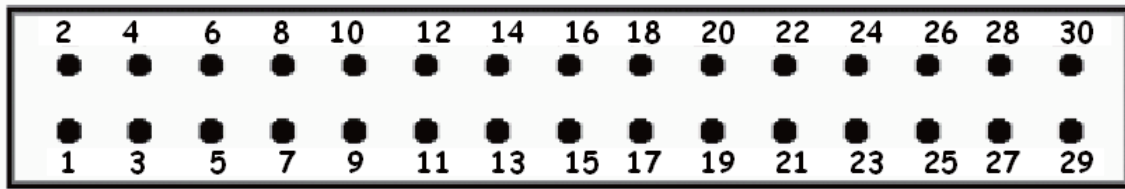


Table 5-16. LCD Socket J21 HE10 Female LCD 2\*15p

LCD	Pin Number		LCD
VDD3V3	1	2	GND
VDD3V3	3	4	GND
ZB_IRQ0	5	6	ZB_IRQ1
TWCK1	7	8	TWD1
GND	9	10	LCDDAT15
GND	11	12	LCDDAT13
GND	13	14	LCDDAT14
GND	15	16	LCDDAT12
GND	17	18	LCDDAT0
LCDDAT1	19	20	LCDDAT2
LCDDAT3	21	22	LCDDAT4
LCDDAT5	23	24	LCDDAT6
LCDDAT7	25	26	LCDDAT8
LCDDAT9	27	28	LCDDAT10
LCDDAT11	29	30	GND

## 5.4.16 LCD/TSC Socket J22

Figure 5-39. LCD/TSC Socket J22

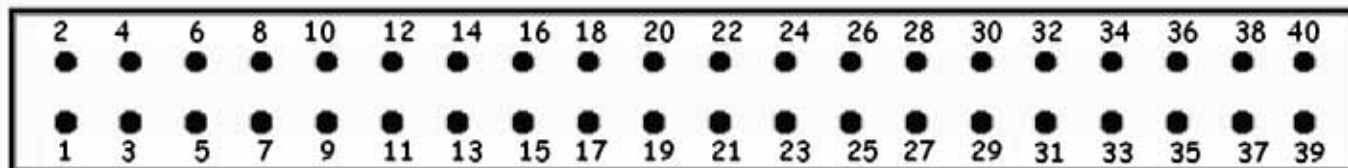


Table 5-17. LCD/TSC Socket J22 HE10 Female LCD/TSC/QT 2\*20p

LCD		Pin Number		LCD	
5V	5V_LCD	1	2	GND	GND
5V	5V_LCD	3	4	GND	GND
LCDDAT16		5	6		LCDDAT17
LCDDAT18		7	8		LCDDAT19
LCDDAT20		9	10		LCDDAT21
LCDDAT22		11	12		LCDDAT23
GND	GND	13	14	GND	GND
LCDDISP		15	16		LCDPWM
LCDCSYNC		17	18		LCDHSYNC
LCDDEN		19	20		LCDPCK
GND	GND	21	22	GND	GND
AD0_XP	TSC	23	24	TSC	AD1_XM
AD2_YP	TSC	25	26	TSC	AD3_YM
AD4_LR	TSC	27	28		ONE_WIRE
GND1	GND	29	30	GND	GND
SPI1_MISO		31	32		SPI1_MOSI
SPI1_SPCK		33	34		SPI1_NPCS3
EN_PWRLCD		35	36	LCD_DETECT	LCD_DETECT#
	PB14	37	38	PB15	
GND	GND	39	40	GND	GND

## 5.4.17 ISI Socket J11

Figure 5-40. ISI Socket J11

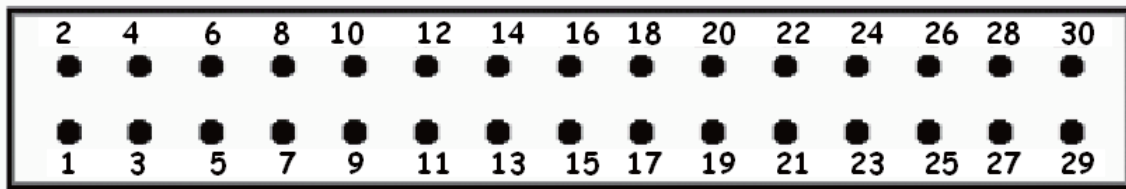


Table 5-18. ISI Socket J11 HE10 Female ISI 2\*15p

ISI	Pin Number		ISI
VDDISI	1	2	GND
VDDISI	3	4	GND
ZB_SLPTR	5	6	ZB_RST
TWCK1	7	8	TWD1
GND	9	10	ISI_MCK
GND	11	12	ISI_VSYNC
GND	13	14	ISDI_HSYNC
GND	15	16	ISI_PCK
GND	17	18	ISI_D0
ISI_D1	19	20	ISI_D2
ISI_D3	21	22	ISI_D4
ISI_D5	23	24	ISI_D6
ISI_D7	25	26	ISI_D8
ISI_D9	27	28	ISI_D10
ISI_D11	29	30	GND



## 5.4.18 PIO Usage

**Table 5-19. PIO A Pin Assignment and Signal Description**

Power Rail	Signal	Signal	Signal	Signal	SAMA5-CM	SAMA5-MB
VDDIOP0	PA0	LCDDAT0	PIO	PU	–	LCDDAT0
VDDIOP0	PA1	LCDDAT1	PIO	PU	–	LCDDAT1
VDDIOP0	PA2	LCDDAT2	PIO	PU	–	LCDDAT2
VDDIOP0	PA3	LCDDAT3	PIO	PU	–	LCDDAT3
VDDIOP0	PA4	LCDDAT4	PIO	PU	–	LCDDAT4
VDDIOP0	PA5	LCDDAT5	PIO	PU	–	LCDDAT5
VDDIOP0	PA6	LCDDAT6	PIO	PU	–	LCDDAT6
VDDIOP0	PA7	LCDDAT7	PIO	PU	–	LCDDAT7
VDDIOP0	PA8	LCDDAT8	PIO	PU	–	LCDDAT8
VDDIOP0	PA9	LCDDAT9	PIO	PU	–	LCDDAT9
VDDIOP0	PA10	LCDDAT10	PIO	PU	–	LCDDAT10
VDDIOP0	PA11	LCDDAT11	PIO	PU	–	LCDDAT11
VDDIOP0	PA12	LCDDAT12	PIO	PU	–	LCDDAT12
VDDIOP0	PA13	LCDDAT13	PIO	PU	–	LCDDAT13
VDDIOP0	PA14	LCDDAT14	PIO	PU	–	LCDDAT14
VDDIOP0	PA15	LCDDAT15	PIO	PU	–	LCDDAT15
VDDIOP0	PA16	LCDDAT16	ISI_D0	PIO	–	ISI_D0
VDDIOP0	PA17	LCDDAT17	ISI_D1	PIO	–	ISI_D1
VDDIOP0	PA18	LCDDAT18	TWD2	ISI_D2	–	ISI_D2
VDDIOP0	PA19	LCDDAT19	TWCK2	ISI_D3	–	ISI_D3
VDDIOP0	PA20	LCDDAT20	PWMH0	ISI_D4	–	ISI_D4
VDDIOP0	PA21	LCDDAT21	PWML0	ISI_D5	–	ISI_D5
VDDIOP0	PA22	LCDDAT22	PWMH1	ISI_D6	–	ISI_D6
VDDIOP0	PA23	LCDDAT23	PWML1	ISI_D7	–	ISI_D7
VDDIOP0	PA24	LCDPWM	PIO	PU	–	LCDPWM
VDDIOP0	PA25	LCDDISP	PIO	PU	–	LCDDISP
VDDIOP0	PA26	LCDVSYNC	PIO	PU	–	LCDVSYNC
VDDIOP0	PA27	LCDHSYNC	PIO	PU	–	LCDHSYNC
VDDIOP0	PA28	LCDPCK	PIO	PU	–	LCDPCK
VDDIOP0	PA29	LCDDEN	PIO	PU	–	LCDDEN
VDDIOP0	PA30	TWD0	URXD1	ISI_VSYNC	–	ISI_VSYNC
VDDIOP0	PA31	TWCK0	UTXD1	ISI_HSYNC	–	ISI_HSYNC

**Table 5-20. PIO B Pin Assignment and Signal Description**

Power Rail	Signal	Signal	Signal	Signal	SAMA5-CM	SAMA5-MB
VDDIOP1	PB0	GTX0	PWMH0	PIO	GETH CM	–
VDDIOP1	PB1	GTX1	PWML0	PIO	GETH CM	–
VDDIOP1	PB2	GTX2	TK1	PIO	GETH CM	–
VDDIOP1	PB3	GTX3	TF1	PIO	GETH CM	–
VDDIOP1	PB4	GRX0	PWMH1	PIO	GETH CM	–
VDDIOP1	PB5	GRX1	PWML1	PIO	GETH CM	–
VDDIOP1	PB6	GRX2	TD1	PIO	GETH CM	–
VDDIOP1	PB7	GRX3	RK1	PIO	GETH CM	–
VDDIOP1	PB8	GTXCK	PWMH2	PIO	GETH CM	–
VDDIOP1	PB9	GTXEN	PWML2	PIO	GETH CM	–
VDDIOP1	PB10	GTXER	RF1	PIO	–	PWR_MCI0
VDDIOP1	PB11	GRXCK	RD1	PIO	GETH CM	–
VDDIOP1	PB12	GRXDV	PWMH3	PIO	–	PWR_MCI1
VDDIOP1	PB13	GRXER	PWML3	PIO	GETH CM	RX_DV (KSZ9021)
VDDIOP1	PB14	GCRS	CANRX1	PIO	–	CANRX1
VDDIOP1	PB15	GCOL	CANTX1	PIO	–	CANTX1
VDDIOP1	PB16	GMDC	PIO	PU	GETH CM	–
VDDIOP1	PB17	GMDIO	PIO	PU	GETH CM	–
VDDIOP1	PB18	G125CK	PIO	PU	GETH CM	–
VDDIOP1	PB19	MCI1_CDA	GTX4	PIO	–	MCI1_CDA
VDDIOP1	PB20	MCI1_DA0	GTX5	PIO	–	MCI1_DA0
VDDIOP1	PB21	MCI1_DA1	GTX6	PIO	–	MCI1_DA1
VDDIOP1	PB22	MCI1_DA2	GTX7	PIO	–	MCI1_DA2
VDDIOP1	PB23	MCI1_DA3	GRX4	PIO	–	MCI1_DA3
VDDIOP1	PB24	MCI1_CK	GRX5	PIO	–	MCI1_CK
VDDIOP1	PB25	SCK1	GRX6	PIO	INT_GETH0	–
VDDIOP1	PB26	CTS1	GRX7	PIO	–	CTS1
VDDIOP1	PB27	RTS1	PWMH1	PIO	–	RTS1
VDDIOP1	PB28	RXD1	PIO	PU	–	RXD1
VDDIOP1	PB29	TXD1	PIO	PU	–	TXD1
VDDIOP0	PB30	DRXD	PIO	PU	–	DRXD (DBGU)
VDDIOP0	PB31	DTXD	PIO	PU	–	DTXD (DBGU)

**Table 5-21. PIO C Pin Assignment and Signal Description**

Power Rail	Signal	Signal	Signal	Signal	SAMA5-MB	
VDDIOP0	PC0	ETX0	TIOA3	PIO	ETX0	–
VDDIOP0	PC1	ETX1	TIOB3	PIO	ETX1	–
VDDIOP0	PC2	ERX0	TCLK3	PIO	ERX0	–
VDDIOP0	PC3	ERX1	TIOA4	PIO	ERX1	–
VDDIOP0	PC4	ETXEN	TIOB4	PIO	ETXEN	–
VDDIOP0	PC5	ECRSDV	TCLK4	PIO	ECRSDV	–
VDDIOP0	PC6	ERXER	TIOA5	PIO	ERXER	–
VDDIOP0	PC7	EREFCK	TIOB5	PIO	EREFCK	–
VDDIOP0	PC8	EMDC	TCLK5	PIO	EMDC	–
VDDIOP0	PC9	EMDIO	PIO	PU	EMDIO	–
VDDIOP0	PC10	MCI2_CDA	LCDDAT20	PIO	LCDDAT20	–
VDDIOP0	PC11	MCI2_DA0	LCDDAT19	PIO	LCDDAT19	–
VDDIOP0	PC12	MCI2_DA1	TIOA1	LCDDAT18	LCDDAT18	–
VDDIOP0	PC13	MCI2_DA2	TIOB1	LCDDAT17	LCDDAT17	–
VDDIOP0	PC14	MCI2_DA3	TCLK1	LCDDAT16	LCDDAT16	–
VDDIOP0	PC15	MCI2_CK	PCK2	LCDDAT21	LCDDAT21	ISI_MCK
VDDIOP0	PC16	TK0	PIO	PU	TK0 Audio	–
VDDIOP0	PC17	TF0	PIO	PU	TF0 Audio	–
VDDIOP0	PC18	TD0	PIO	PU	TD0 Audio	–
VDDIOP0	PC19	RK0	PIO	PU	RK0 Audio	–
VDDIOP0	PC20	RF0	PIO	PU	RF0 Audio	–
VDDIOP0	PC21	RD0	PIO	PU	RD0 Audio	–
VDDIOP0	PC22	SPI1_MISO	PIO	PU	SPI1_MISO	SPI LCD
VDDIOP0	PC23	SPI1_MOSI	PIO	PU	SPI1_MOSI	SPI LCD
VDDIOP0	PC24	SPI1_SPCK	PIO	PU	SPI1_SPCK	SPI LCD
VDDIOP0	PC25	SPI1_NPCS0	PIO	PU	SPI1_NPCS0	–
VDDIOP0	PC26	SPI1_NPCS1	TWD1	ISI_D11	ISI_D11	TWI LCD
VDDIOP0	PC27	SPI1_NPCS2	TWCK1	ISI_D10	ISI_D10	TWI LCD
VDDIOP0	PC28	SPI1_NPCS3	PWMFI0	ISI_D9	ISI_D9	SPI LCD
VDDIOP0	PC29	URXD0	PWMFI2	ISI_D8	ISI_D8	HDMI_INT
VDDIOP0	PC30	UTXD0	ISI_PCK	PIO	ISI_PCK	–
VDDIOP0	PC31	FIQ	PWMFI1	PIO	–	Reset_HDMI

**Table 5-22. PIO D Pin Assignment and Signal Description**

Power Rail	Signal	Signal	Signal	Signal	SAMA5-MB	
VDDIOP1	PD0	MCI0_CDA	PIO	PU	–	MCI0_CDA
VDDIOP1	PD1	MCI0_DA0	PIO	PU	–	MCI0_DA0
VDDIOP1	PD2	MCI0_DA1	PIO	PU	–	MCI0_DA1
VDDIOP1	PD3	MCI0_DA2	PIO	PU	–	MCI0_DA2
VDDIOP1	PD4	MCI0_DA3	PIO	PU	–	MCI0_DA3
VDDIOP1	PD5	MCI0_DA4	TIOA0	PWMH2	–	MCI0_DA4
VDDIOP1	PD6	MCI0_DA5	TIOB0	PWML2	–	MCI0_DA5
VDDIOP1	PD7	MCI0_DA6	TCLK0	PWMH3	–	MCI0_DA6
VDDIOP1	PD8	MCI0_DA7	PWML3	PIO	–	MCI0_DA7
VDDIOP1	PD9	MCI0_CK	PIO	PU	–	MCI0_CK
VDDIOP1	PD10	SPI0_MISO	PIO	PU	CM_SerFlash	–
VDDIOP1	PD11	SPI0_MOSI	PIO	PU	CM_SerFlash	–
VDDIOP1	PD12	SPI0_SPCK	PIO	PU	CM_SerFlash	–
VDDIOP1	PD13	SPI0_NPCS0	PIO	PU	CM_SerFlash	–
VDDIOP1	PD14	SCK0	SPI0_NPCS1	CANRX0	–	CANRX0
VDDIOP1	PD15	CTS0	SPI0_NPCS2	CANTX0	–	CANTX0
VDDIOP1	PD16	RTS0	SPI0_NPCS3	PWMF13	INT_AUDIO	–
VDDIOP1	PD17	RXD0	PIO	PU	–	MCI0_CD
VDDIOP1	PD18	TXD0	PIO	PU	–	MCI1_CD
VDDIOP1	PD19	ADTRG	PIO	PU	–	ADTRG (HSYNC)
VDDANA	PD20	AD0	PIO	PU	–	LCD TSC
VDDANA	PD21	AD1	PIO	PU	–	LCD TSC
VDDANA	PD22	AD2	PIO	PU	–	LCD TSC
VDDANA	PD23	AD3	PIO	PU	–	LCD TSC
VDDANA	PD24	AD4	PIO	PU	–	LCD TSC
VDDANA	PD25	AD5	PIO	PU	–	EN5V_USBA
VDDANA	PD26	AD6	PIO	PU	–	EN5V_USBB
VDDANA	PD27	AD7	PIO	PU	–	EN5V_USBC
VDDANA	PD28	AD8	PIO	PU	–	OVCUR_USB
VDDANA	PD29	AD9	PIO	PU	–	VBUS_SENSE
VDDANA	PD30	AD10	PCK0	PIO	MCLK_AUDIO	MCLK_HDMI
VDDANA	PD31	AD11	PCK1	PIO	–	ISI_MCK

**Table 5-23. PIO E Pin Assignment and Signal Description**

Power Rail	Signal	Signal	Signal	SAMA5-CM	SAMA5-MB	
VDDIOM	PE0	A0/NBS0	I		–	–
VDDIOM	PE1	A1	I	NOR	–	–
VDDIOM	PE2	A2	I	NOR	–	–
VDDIOM	PE3	A3	I	NOR	–	–
VDDIOM	PE4	A4	I	NOR	–	–
VDDIOM	PE5	A5	I	NOR	–	–
VDDIOM	PE6	A6	I	NOR	–	–
VDDIOM	PE7	A7	I	NOR	–	–
VDDIOM	PE8	A8	I	NOR	–	–
VDDIOM	PE9	A9	I	NOR	–	–
VDDIOM	PE10	A10	I	NOR	–	–
VDDIOM	PE11	A11	I	NOR	–	–
VDDIOM	PE12	A12	I	NOR	–	–
VDDIOM	PE13	A13	I	NOR	–	–
VDDIOM	PE14	A14	I	NOR	–	–
VDDIOM	PE15	A15	SCK3	NOR	–	–
VDDIOM	PE16	A16	CTS3	NOR	–	–
VDDIOM	PE17	A17	RTS3	NOR	–	–
VDDIOM	PE18	A18	RXD3	NOR	–	–
VDDIOM	PE19	A19	TXD3	NOR	–	–
VDDIOM	PE20	A20	SCK2	NOR	–	–
VDDIOM	PE21	A21/NANDALE	I	NOR / NAND	–	–
VDDIOM	PE22	A22/NANDCLE	I	NOR / NAND	–	–
VDDIOM	PE23	A23	CTS2	NOR	–	–
VDDIOM	PE24	A24	RTS2	Power LED	ISI_RST	–
VDDIOM	PE25	A25	RXD2	1-Wire / User LED	1-Wire	–
VDDIOM	PE26	NCS0	TXD2	CS NOR	–	–
VDDIOM	PE27	NCS1	TIOA2	–	PB_USER1	LCDDAT22
VDDIOM	PE28	NCS2	TIOB2	–	ZB_SLPTR	LCDDAT23
VDDIOM	PE29	NWR1/NBS1	TCLK2	–	ZB_RST	–
VDDIOM	PE30	NWAIT	I	–	ZB_IRQ1	INT_ETH1
VDDIOM	PE31	IRQ	PWML1	–	ZB_IRQ0	HDMI_INT

## 5.4.19 IO Expansion Port J1

Figure 5-41. IO Expansion Socket J1

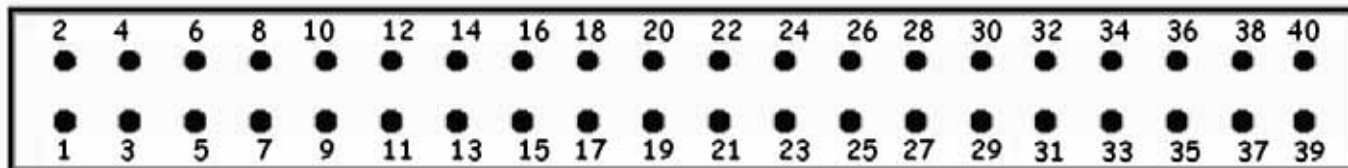


Table 5-24. IO Expansion Socket J1 HE10 Male 2\*20 Signal Descriptions

Signal	Pin Number		Signal
VDDIOP0 / 5V	1	2	VDDIOP0 / 5V
GND	3	4	GND
PA0	5	6	PA16
PA1	7	8	PA17
PA2	9	10	PA18
PA3	11	12	PA19
PA4	13	14	PA20
PA5	15	16	PA21
PA6	17	18	PA22
PA7	19	20	PA23
PA8	21	22	PA24
PA9	23	24	PA25
PA10	25	26	PA26
PA11	27	28	PA27
PA12	29	30	PA28
PA13	31	32	PA29
PA14	33	34	PA30
PA15	35	36	PA31
GND	37	38	GND
VDDIOP0	39	40	VDDIOP0

## 5.4.20 IO Expansion Port J2

Figure 5-42. IO Expansion Socket J2

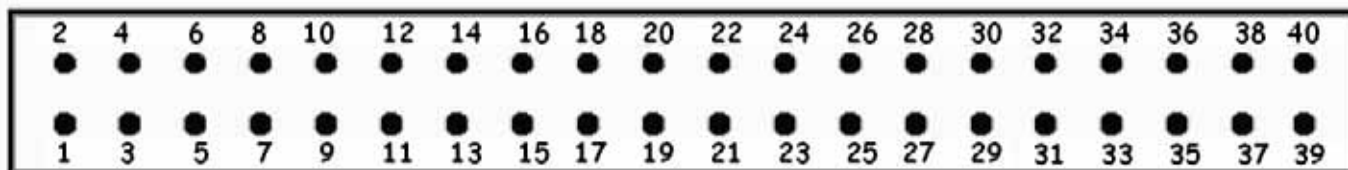


Table 5-25. Expansion Socket J2 HE10 Male 2\*20 Signal Descriptions

Signal	Pin Number		Signal
VDDIOP0 / 5V	1	2	VDDIOP0 / 5V
GND	3	4	GND
PC0	5	6	PC16
PC1	7	8	PC17
PC2	9	10	PC18
PC3	11	12	PC19
PC4	13	14	PC20
PC5	15	16	PC21
PC6	17	18	PC22
PC7	19	20	PC23
PC8	21	22	PC24
PC9	23	24	PC25
PC10	25	26	PC26
PC11	27	28	PC27
PC12	29	30	PC28
PC13	31	32	PC29
PC14	33	34	PC30
PC15	35	36	PC31
GND	37	38	GND
VDDIOP0	39	40	VDDIOP0

## 5.4.21 IO Expansion Port J3

Figure 5-43. IO Expansion Socket J3

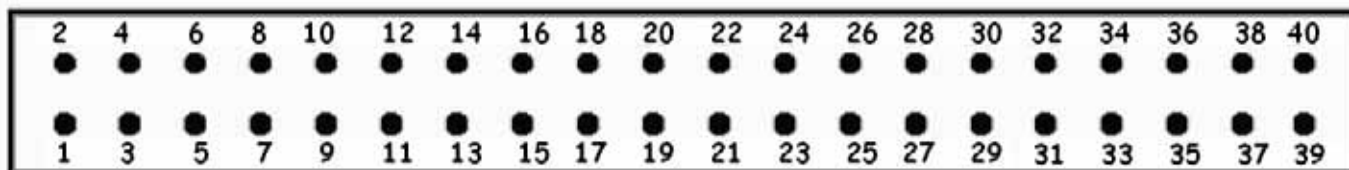


Table 5-26. Expansion Socket J3 HE10 Male 2\*20 Signal Descriptions

Signal	Pin Number		Signal
VDDIOP0 / 5V	1	2	VDDIOP0 / 5V
GND	3	4	GND
PB10	5	6	PB31
PB12	7	8	PE23
PB14	9	10	PE24
PB15	11	12	PE25
PB19	13	14	PE26
PB20	15	16	PE29
PB21	17	18	PE30
PB22	19	20	PE31
PB23	21	22	PD10
PB24	23	24	PD11
PB25	25	26	PD12
PB26	27	28	PD13
PB27	29	30	PD14
PB28	31	32	PD15
PB29	33	34	PD19
PB30	35	36	PD31
GND	37	38	GND
VDDIOP0	39	40	VDDIOP0



### 5.4.22 SODIMM Card Edge Socket

The SAMA5D3 series-EK implements a SODIMM200 standard connector for to interface to the CM board.

Note this is not an industry standard pinout and is unlikely to be compatible with off-the-shelf SODIMM.

Figure 5-44. SODIMM200 Socket CON1



**Table 5-27. SODIMM200 CON1 Signal Descriptions**

PIOC	PIOB	PIOA		SODIMM 200			PIOA	PIOB	PIOC
			Front Side	A	B	Back Side			
–	–	VCC 5V		1	2	VCC 5V		–	–
–	–	VCC 5V		3	4	VCC 5V		–	–
–	–	GND		5	6	VBAT		–	–
–	–	CTS2	PE23	7	8	PE29	NWR1/NBS1	TCLK2	–
–	–	RTS2	PE24	9	10	PE30	NWAIT	–	–
–	–	RXD2	PE25	11	12	PE31	IRQ	PWML1	–
–	–	TXD2	PE26	13	14	–	–	GND	–
–	–	VDDIOM		15	16	VDDIOM		–	–
–	–	SPI1_NPCS0	PC25	17	18	PC24	SPI1_SPCK	–	–
–	–	SPI1_MOSI	PC23	19	20	PC22	SPI1_MISO	–	–
–	–	RD0	PC21	21	22	PC20	RF0	–	–
–	–	GND		23	24	PC19	RK0	–	–
–	–	TD0	PC18	25	26	PC17	TF0	–	–
–	–	TK0	PC16	27	28	PC9	EMDIO	PIO	–
–	TCLK5	EMDC	PC8	29	30	PC7	EREFCK	TIOB5	–
–	TIOA5	ERXER	PC6	31	32	–	–	GND	–
–	TIOB4	ETXEN	PC4	33	34	PC5	ECRSDV	TCLK4	–
–	TCLK3	ERX0	PC2	35	36	PC3	ERX1	TIOA4	–
–	TIOA3	ETX0	PC0	37	38	PC1	ETX1	TIOB3	–
–	Power Enable		Enable_0	39	40	Enable_1	CS Boot Disable		–
				KEY					
–	–	VCC 3V3		41	42	VCC 3V3		–	–
–	–	VCC 3V3		43	44	VCC 3V3		–	–
–	–	NC	Enable_2	45	46	Enable_3	NC	–	–
–	–	NC	–	47	48	–	ADVREF	–	–
LCDDAT22	TIOA2	NCS1	PE27	49	50	PE28	NCS2	TIOB2	LCDDAT23
–	LCDDAT20	MCI2_CDA	PC10	51	52	PC11	MCI2_DA0	LCDDAT19	PIO
–	–	GND	–	53	54	PC13	MCI2_DA2	TIOB1	LCDDAT17
LCDDAT18	TIOA1	MCI2_DA1	PC12	55	56	PC15	MCI2_CK	PCK2	LCDDAT21
LCDDAT16	TCLK1	MCI2_DA3	PC14	57	58	PC26	SPI1_NPCS1	–	ISI_D11
ISI_D10	–	SPI1_NPCS2	PC27	59	60	PC28	SPI1_NPCS3	PWMF10	ISI_D9
ISI_D8	PWMF12	URXD0	PC29	61	62	–	GND	–	–
–	PWMF11	FIQ	PC31	63	64	PC30	UTXD0	ISI_PCK	–
VDDIOP0				65	66	VDDIOP0			
–	–	LCDDAT0	PA0	67	68	PA1	LCDDAT1	–	–

**Table 5-27. SODIMM200 CON1 Signal Descriptions**

PIOC	PIOB	PIOA		SODIMM 200			PIOA	PIOB	PIOC
–	–	LCDDAT2	PA2	69	70	PA3	LCDDAT3	–	–
–	–	GND	–	71	72	PA4	LCDDAT4	–	–
–	–	LCDDAT5	PA5	73	74	PA6	LCDDAT6	–	–
–	–	LCDDAT7	PA7	75	76	PA8	LCDDAT8	–	–
–	–	LCDDAT9	PA9	77	78	PA10	LCDDAT10	–	–
–	–	LCDDAT11	PA11	79	80		GND	–	–
–	–	LCDDAT12	PA12	81	82	PA13	LCDDAT13	–	–
–	–	LCDDAT14	PA14	83	84	PA15	LCDDAT15	–	–
–	ISI_D0	LCDDAT16	PA16	85	86	PA17	LCDDAT17	ISI_D1	–
ISI_D2	TWD2	LCDDAT18	PA18	87	88	PA19	LCDDAT19	TWCK2	ISI_D3
–	–	GND	–	89	90	PA20	LCDDAT20	PWMH0	ISI_D4
ISI_D5	PWML0	LCDDAT21	PA21	91	92	PA22	LCDDAT22	PWMH1	ISI_D6
ISI_D7	PWML1	LCDDAT23	PA23	93	94	PA24	LCDPWM	–	–
–	–	LCDDISP	PA25	95	96	PA26	LCDVSYNC	–	–
–	–	LCDHSYNC	PA27	97	98		GND	–	–
–	–	LCDPCK	PA28	99	100	PA29	LCDDEN	–	–
ISI_VSYNC	URXD1	TWD0	PA30	101	102	PA31	TWCK0	UTXD1	ISI_HSYNC
VDDANA				103	104	VDDANA			
–	PCK0	AD10	PD30	105	106	PD31	AD11	PCK1	–
–	–	GND	–	107	108	PD29	AD9	–	–
–	–	AD8	PD28	109	110	PD27	AD7	–	–
–	–	AD6	PD26	111	112	PD25	AD5	–	–
–	–	AD4	PD24	113	114	PD23	AD3	–	–
–	–	AD2	PD22	115	116		GND	–	–
–	–	AD0	PD20	117	118	PD21	AD1	–	–
–	–	TXD0	PD18	119	120	PD19	ADTRG	–	–
PWMFI3	SPI0_NPCS3	RTS0	PD16	121	122	PD17	RXD0	PIO	–
CANRX0	SPI0_NPCS1	SCK0	PD14	123	124	PD15	CTS0	SPI0_NPCS2	CANTX0
–	–	GND	–	125	126	PD13	SPI0_NPCS0	–	–
–	–	SPI0_SPCK	PD12	127	128	PD11	SPI0_MOSI	–	–
–	–	SPI0_MISO	PD10	129	130	PD9	MCIO_CK	–	–
PIO	PWML3	MCIO_DA7	PD8	131	132	PD7	MCIO_DA6	TCLK0	PWMH3
PWML2	TIOB0	MCIO_DA5	PD6	133	134		GND	–	–
PWMH2	TIOA0	MCIO_DA4	PD5	135	136	PD4	MCIO_DA3	–	–
–	–	MCIO_DA2	PD3	137	138	PD2	MCIO_DA1	–	–
–	–	MCIO_DA0	PD1	139	140	PD0	MCIO_CDA	–	–
VDDIOP1				141	142	VDDIOP1			

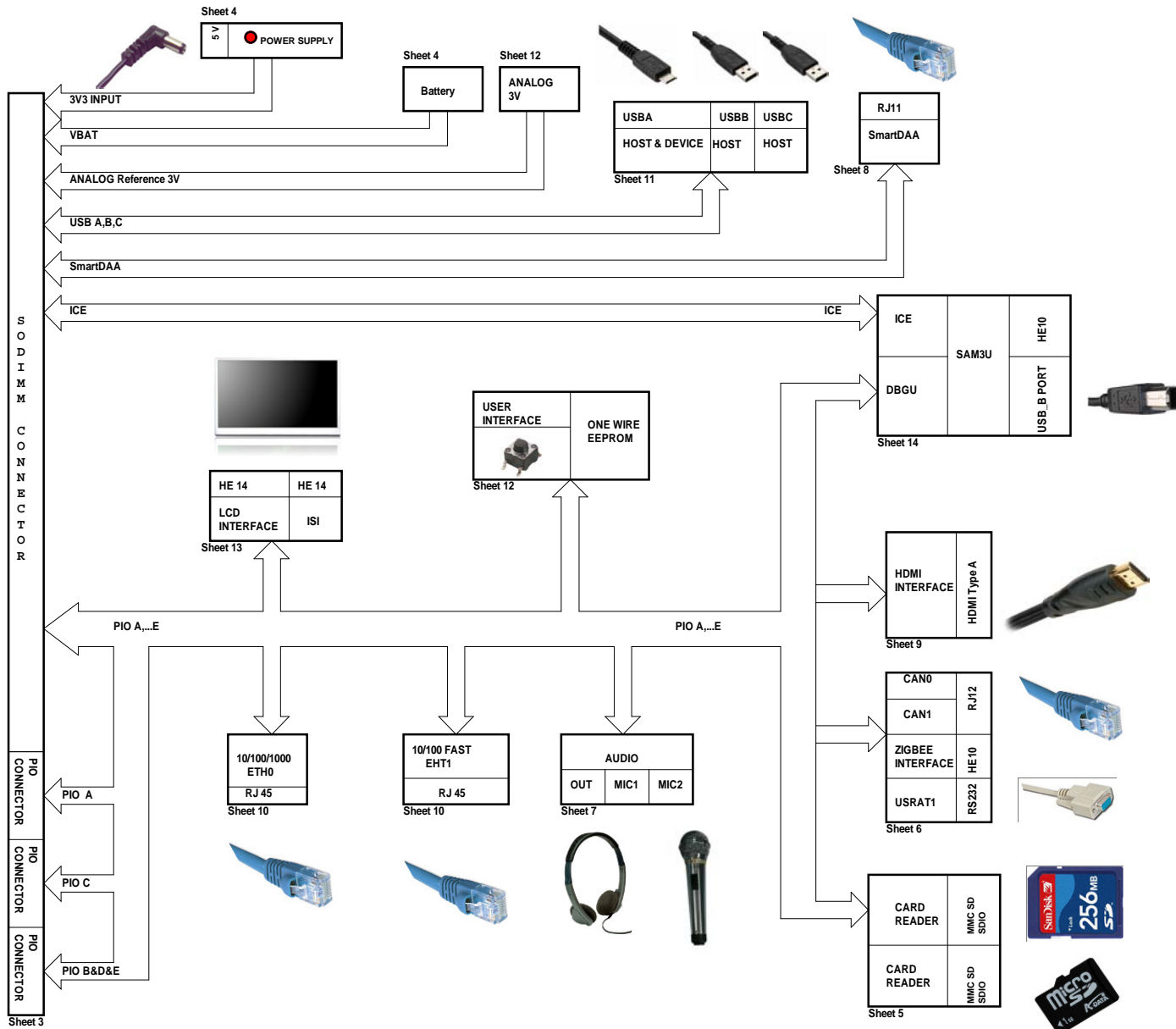
**Table 5-27. SODIMM200 CON1 Signal Descriptions**

PIOC	PIOB	PIOA		SODIMM 200			PIOA	PIOB	PIOC
–	–	GND	–	143	144	PB13	GRXER	PWML3	–
–	RF1	GTXER	PB10	145	146	PB12	GRXDV	PWMH3	–
–	CANRX1	GCRS	PB14	147	148	PB15	GCOL	CANTX1	–
–	GTX4	MCI1_CDA	PB19	149	150	PB20	MCI1_DA0	GTX5	–
–	GTX6	MCI1_DA1	PB21	151	152	PB22	MCI1_DA2	GTX7	–
–	GRX4	MCI1_DA3	PB23	153	154	–	GND	–	–
–	GRX5	MCI1_CK	PB24	155	156	PB25	SCK1	GRX6	–
–	–	GND	–	157	158	PB27	RTS1	PWMH1	–
–	USB A	USBA_DP	–	159	160	PB29	TXD1	PIO	–
–	USB A	USBA_DM	–	161	162	PB31	DTXD	–	–
–	–	GND	–	163	164	PB30	DRXD	–	–
–	USB B	USBB_DP	–	165	166	PB26	CTS1	GRX7	–
–	USB B	USBB_DM	–	167	168	PB28	RXD1	PIO	–
–	–	GND	–	169	170	–	GND	–	–
–	USB C	USBC_DP	–	171	172	DIB	DIBP	–	–
–	USB C	USBC_DM	–	173	174	DIB	DIBN	–	–
–	–	GND_ETH	–	175	176	–	GND	–	–
–	GIGA_ETH	ETH0_TX1+	–	177	178	–	JTAGSEL	SYSC	–
–	GIGA_ETH	ETH0_TX1-	–	179	180	–	WKUP	SYSC	–
–	GIGA_ETH	ETH0_RX1+	–	181	182	–	SHDN	SYSC	–
–	GIGA_ETH	ETH0_RX1-	–	183	184	–	BMS	RSTJTAG	–
–	–	GND_ETH	–	185	186	–	nRST	SYSC	–
–	GIGA_ETH	ETH0_TX2+	–	187	188	–	nTRST	RSTJTAG	–
–	GIGA_ETH	ETH0_TX2-	–	189	190	–	TDI	RSTJTAG	–
–	GIGA_ETH	ETH0_RX2+	–	191	192	–	TCK	RSTJTAG	–
–	GIGA_ETH	ETH0_RX2-	–	193	194	–	TMS	RSTJTAG	–
–	–	GND	–	195	196	–	TDO	RSTJTAG	–
–	–	LED2	–	197	198	–	RTCK	RSTJTAG	–
–	–	LED1	–	199	200	–	GND	–	–

## 5.5 Main Board Schematics

This section contains the following schematics:

- Block diagram
- General information
- SODIMM
- Power supply
- HSMCI
- CAN & ZigBee & USART1
- Audio
- Smart DAA
- HDMI
- ETH
- USB interface
- Miscellaneous
- LCD and ISI
- On-board JTAG interface



<b>AMEL</b> ROUSSET							
REV	MODIF	DES	DATE	REV	DATE	SHEET	
C		Derek	30-Sep-12	XX	XX-XXX-XX		
B		Derek	30-Mar-12	XX	XX-XXX-XX		
A		Derek	11-Nov-11	XX	XX-XXX-XX		
SCALE 1/1				REV	DATE	SHEET	
BLOCK Diagram				C		1/4	

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## REVISION HISTORY

REV	DATA	NOTE
A	2011.11	ORIGINAL RELEASED
B	2012.03	SECOND RELEASED
C	2012.10	THIRD RELEASED

## SAMA5D3x config

	SAMA5D31	SAMA5D33	SAMA5D34	SAMA5D35
CAN0			✓	✓
CAN1			✓	✓
GMAC			✓	✓
EMAC	✓	✓	✓	✓
HSMC12	✓		✓	✓
LCDC	✓	✓	✓	✓
USART0	✓			✓
USART1	✓			✓
ISI		✓	✓	✓
TC1			✓	✓

## SCHEMATICS CONVENTIONS

(1) Resistance Unit: "K" is "Kohm", "R" is "Ohm"

(2) "DNP" means the component is not populated by default

## JUMPER and SOLDERDROP

PAGE	REFERENCE	DEFAULT	FUNCTION
3	JP1	1-2	VDDIOP0 or 5V selection for J1
	JP2	1-2	VDDIOP0 or 5V selection for J2
	JP3	1-2	VDDIOP1 or 5V selection for J3
	JP9	OPEN	Default boot on embedded ROM, Close boot on external memory
4	JP4	CLOSE	Backup supply on/off
	JP5	CLOSE	Force power on function
5	JP6	CLOSE	MCIO write protect select
6	JP7	CLOSE	CAN0 diff termination select
	JP8	CLOSE	CAN1 diff termination select
	JP10	OPEN	Zigbee Power on/off select
12	JP14	1-2	ADVREF input selection
14	JP15	OPEN	JTAG Enabled, close to disable
14	JP16	OPEN	CDC Enabled, close to disable
		OPEN	Enable LCD for D31, D33, D34
11	JP17	OPEN	Enable LCD for D31, D33, D34
		CLOSE	Disable LCD for D35

## TEST POINT

PAGE	REFERENCE	FUNCTION
4	TP1, TP2	GND
4	TP3	5V
4	TP4	3V3
4	TP5	VDDIOP0
4	TP6	VDDIOP1
4	TP7	VDDIOM
4	TP8	VDDANA

## DEFAULT NO POPULATE PARTS

PAGE	REFERENCE	FUNCTION
3	R6, R51, R50, R120	Optional PD10, PD11, PD12, PD13 from MB
5	R58	Optional for MCIO Power supply mode
	R121	Optional for MCIO Power supply mode
6	R52, R53, R55, R56, R57, R82, JP10	Optional Zigbee
	R132, R133	Debug or USART1 option
7	C89, C90, R118, R119, J26	Optional Audio Line out, mic in
	R80, R81	Optional MIC level setting
	R230	Optional audio TK
9	L38, L39, L40, L41	Optional HDMI EMI filter
	R89	HDMI chip I2C address setting
	R266	Optional for I2S PCLK
	R42	Optional for LCD PCLK
10	R162, R170, R171, R172, R176, R177, C122, C123,	Optional for KSZ8041NL
12	R144	Optional pull up for DS28EC20P
13	R127	Optional for ADC trigger
14	R79, R106, R107, R109, R113, R110, R112, R111, J9	Optional JTAG
	R54	SAM3U JTAG selection
	R63	5V Option
	D11, D12	USB ESD protect option
	R186	Main 3V3 Optional for VCC_3V3_DEBUG

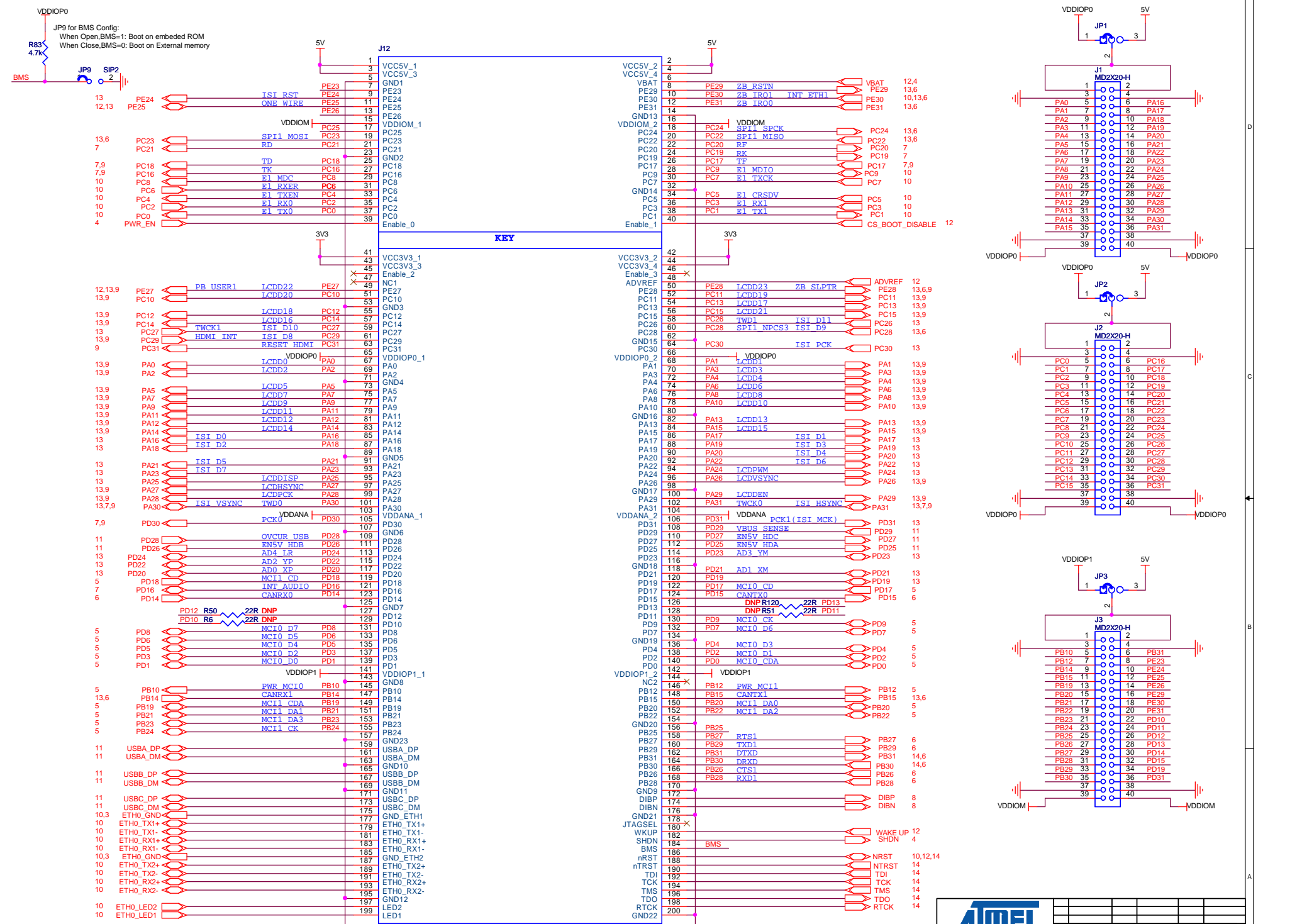
## TABLE OF CONTENTS

PAGE	DESCRIPTION
1	Block Diagram
2	Describe
3	SODIMM
4	POWER SUPPLY
5	HSMC1
6	CAN & ZIGBEE & USART1
7	AUDIO
8	SmartDAA
9	HDMI
10	ETH
11	USB Interface
12	Miscellaneous
13	LCD&ISI
14	Segger-SAM3U

## PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE	PIOD	USAGE	PIOD	USAGE	PIOE	USAGE	PIOE	USAGE
PA0	LCDD0	PA16	ISI_D0	PB0		PB16		PC0	E1_TX0	PC16	TK0	PD0	MCIO_CDA	PD16	INT_AUDIO	PE0		PE16	
PA1	LCDD1	PA17	ISI_D1	PB1		PB17		PC1	E1_TX1	PC17	TF0	PD1	MCIO_DA0	PD17	MCIO_CD	PE1		PE17	
PA2	LCDD2	PA18	ISI_D2	PB2		PB18		PC2	E1_RX0	PC18	TD0	PD2	MCIO_DA1	PD18	MCIO_CD	PE2		PE18	
PA3	LCDD3	PA19	ISI_D3	PB3		PB19	MC11_CDA	PC3	E1_RX1	PC19	RK0	PD3	MCIO_DA2	PD19	ADTRG	PE3		PE19	
PA4	LCDD4	PA20	ISI_D4	PB4		PB20	MC11_DA0	PC4	E1_TXEN	PC20	RF0	PD4	MCIO_DA3	PD20	AD0_XP	PE4		PE20	
PA5	LCDD5	PA21	ISI_D5	PB5		PB21	MC11_DA1	PC5	E1_CRSDV	PC21	RD0	PD5	MCIO_DA4	PD21	AD1_XM	PE5		PE21	
PA6	LCDD6	PA22	ISI_D6	PB6		PB22	MC11_DA2	PC6	E1_RXER	PC22	SPI1_MISO	PD6	MCIO_DA5	PD22	AD2_YP	PE6		PE22	
PA7	LCDD7	PA23	ISI_D7	PB7		PB23	MC11_DA3	PC7	E1_TXCK	PC23	SPI1_MOSI	PD7	MCIO_DA6	PD23	AD3_YM	PE7		PE23	
PA8	LCDD8	PA24	LCDPWM	PB8		PB24	MC11_CK	PC8	E1_MDC	PC24	SPI1_SPCK	PD8	MCIO_DA7	PD24	AD4_LR	PE8		PE24	ISI_RST
PA9	LCDD9	PA25	LCDDISP	PB9		PB25		PC9	E1_MDIO	PC25	SPI1_NPCS0	PD9	MCIO_CK	PD25	EN5V_HDA	PE9		PE25	ONE_WIRE
PA10	LCDD10	PA26	LCDSVSYNC	PB10	PWR_MCIO	PB26	CTS1	PC10	LCDD20	PC26	TWD1	ISI_D11	PD10		EN5V_HDB	PE10		PE26	
PA11	LCDD11	PA27	LCDSVSYNC	PB11		PB27	RTS1	PC11	LCDD19	PC27	TWCK1	ISI_D10	PD11		EN5V_HDC	PE11		PE27	PB_USER1 LCDD22
PA12	LCDD12	PA28	LCDPCK	PB12	PWR_MC11	PB28	RXD1	PC12	LCDD18	PC28	SPI1_NPCS3	ISI_D9	PD12		OVGUR_USB	PE12		PE28	ZB_SLPTR LCDD23
PA13	LCDD13	PA29	LCDDEN	PB13		PB29	TXD1	PC13	LCDD17	PC29	HDMI_INT	ISI_D8	PD13		VBUS_SENSE	PE13		PE29	ZB_RST
PA14	LCDD14	PA30	TWD0	ISI_VSYNC	PB14	CANRX1	DRXD	PC14	LCDD16	PC30		ISI_PCK	PD14	CANRX0	PCK0(Audio,HDMI)	PE14		PE30	ZB_IRQ1 INT_ETH1
PA15	LCDD15	PA31	TWCK0	ISI_HSYNC	PB15	CANTX1	DTXD	PC15	LCDD21	PC31	RESET_HDMI		PD15	CANTX0	ZB_IRQ0	PE15		PE31	ZB_IRQ0

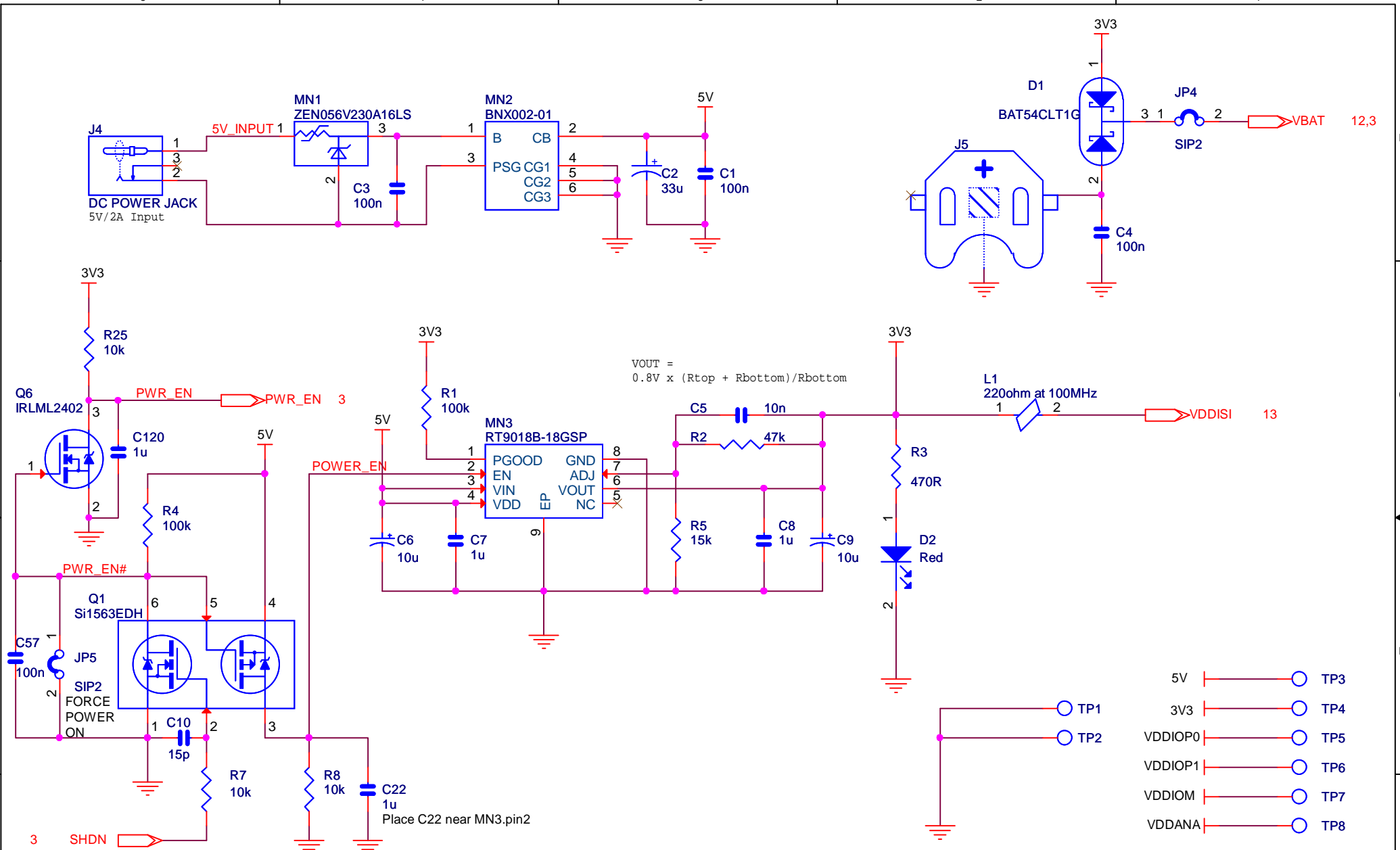
<b>ATMEL</b>					
ROUSSET					
REV	DATE	REV	DATE	REV	DATE
1.1	11-Nov-11	1.1	11-Nov-11	1.1	11-Nov-11
SAMA5D3x-MB		SCALE 1/1		REV. C	
Describe				SHEET 2/14	



<b>ATMEL</b>					
ROUSSET					
G	Derek	30-Sep-12	XX	XX-XXX-XX	
B	Derek	30-Mar-12	XX	XX-XXX-XX	
A	Derek	11-Nov-11	XX	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE
SAMA5D3x-MB		SCALE 1/1		REV. SHEET	
SODIMM				C 3/14	

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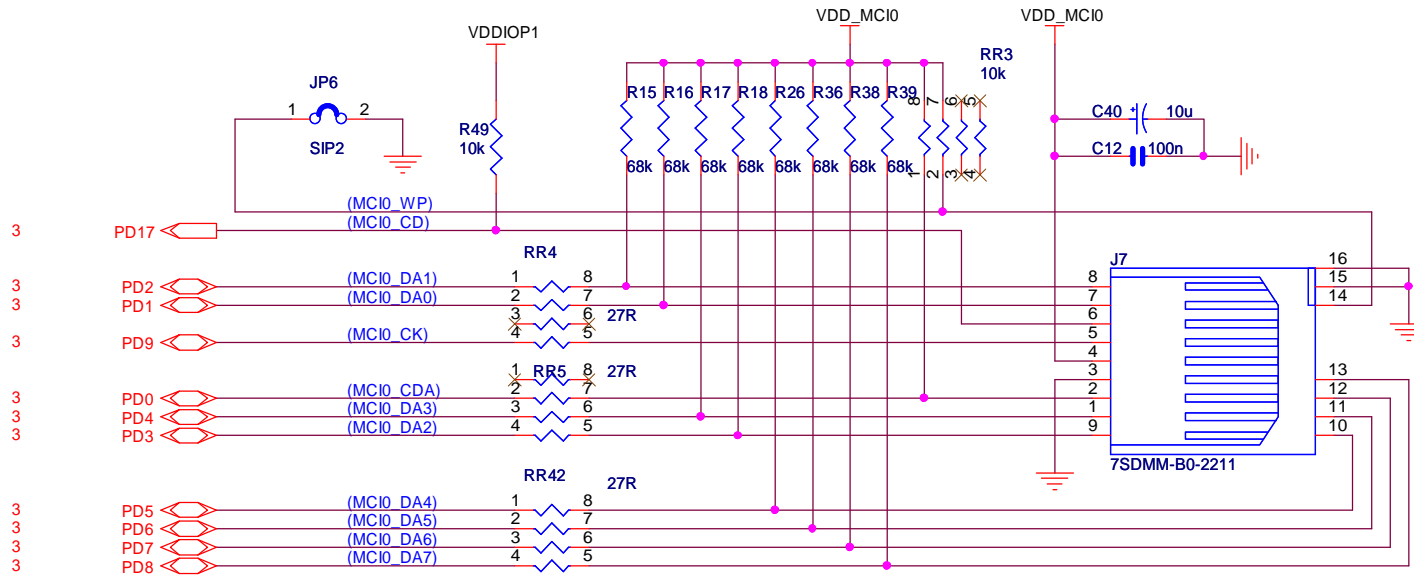


$$V_{OUT} = 0.8V \times (R_{top} + R_{bottom}) / R_{bottom}$$

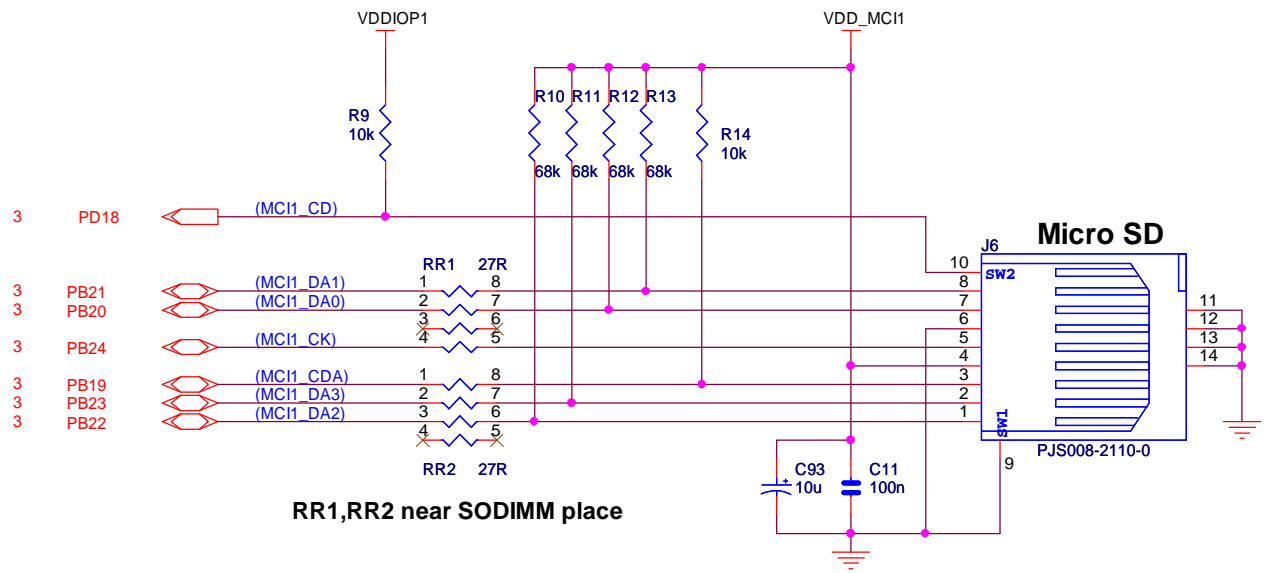
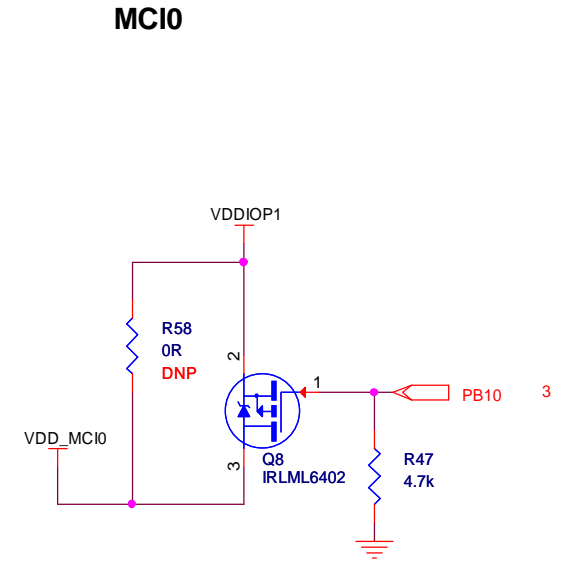
ADHESIVE FEET

- Z6 Bump
- Z7 Bump
- Z17 Bump
- Z8 Bump
- Z9 Bump

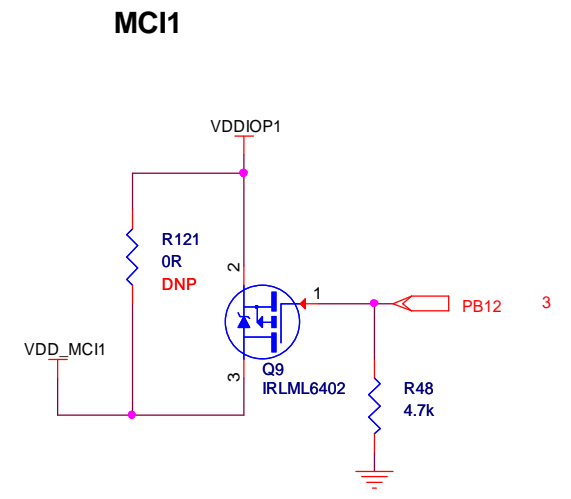
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B	Derek	30-Mar-12	X.X	XX-XXX-XX	
A	Derek	11-Nov-11	X.X	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE
SAMA5D3x-MB		SCALE 1/1		REV. C	SHEET 4/14
POWER SUPPLY					
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RR4,RR5,RR42 near SODIMM place  
SD/MMCPlus CARD INTERFACE - MCIO



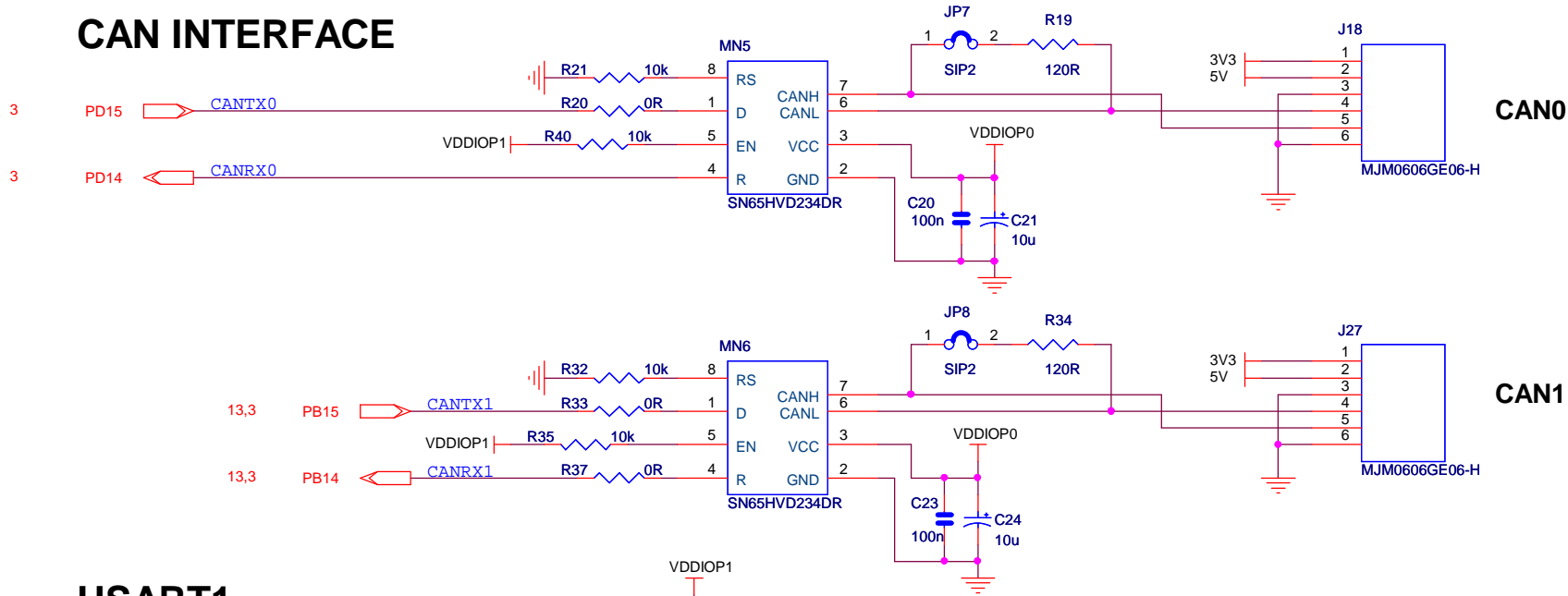
RR1,RR2 near SODIMM place



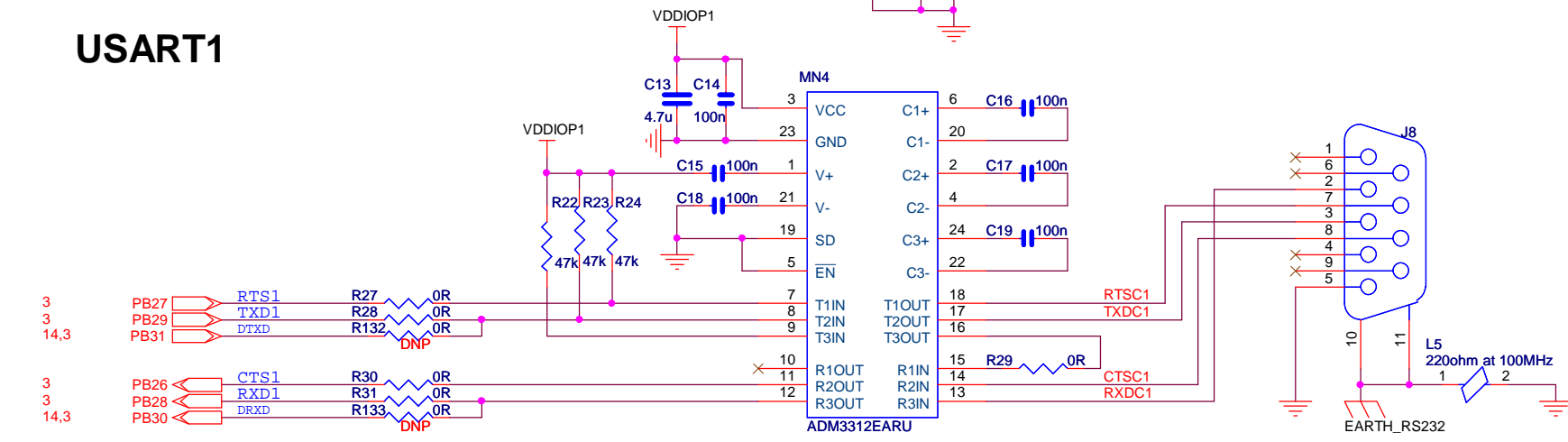
C	Derek	30-Sep-12	X.X	XX-XXX-XX	
B	Derek	30-Mar-12	X.X	XX-XXX-XX	
A	Derek	11-Nov-11	X.X	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE
SAMA5D3x-MB		SCALE 1/1		REV. C	SHEET 5/14
HSMCI					

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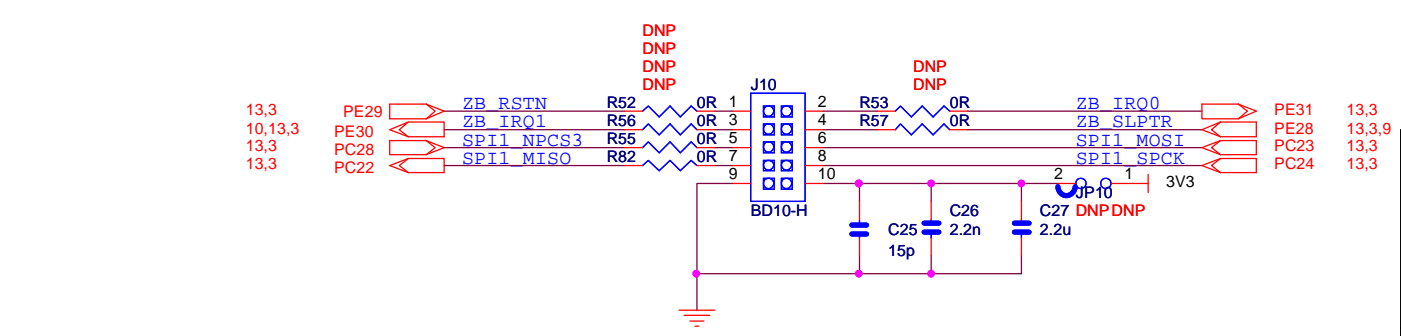
# CAN INTERFACE



# USART1

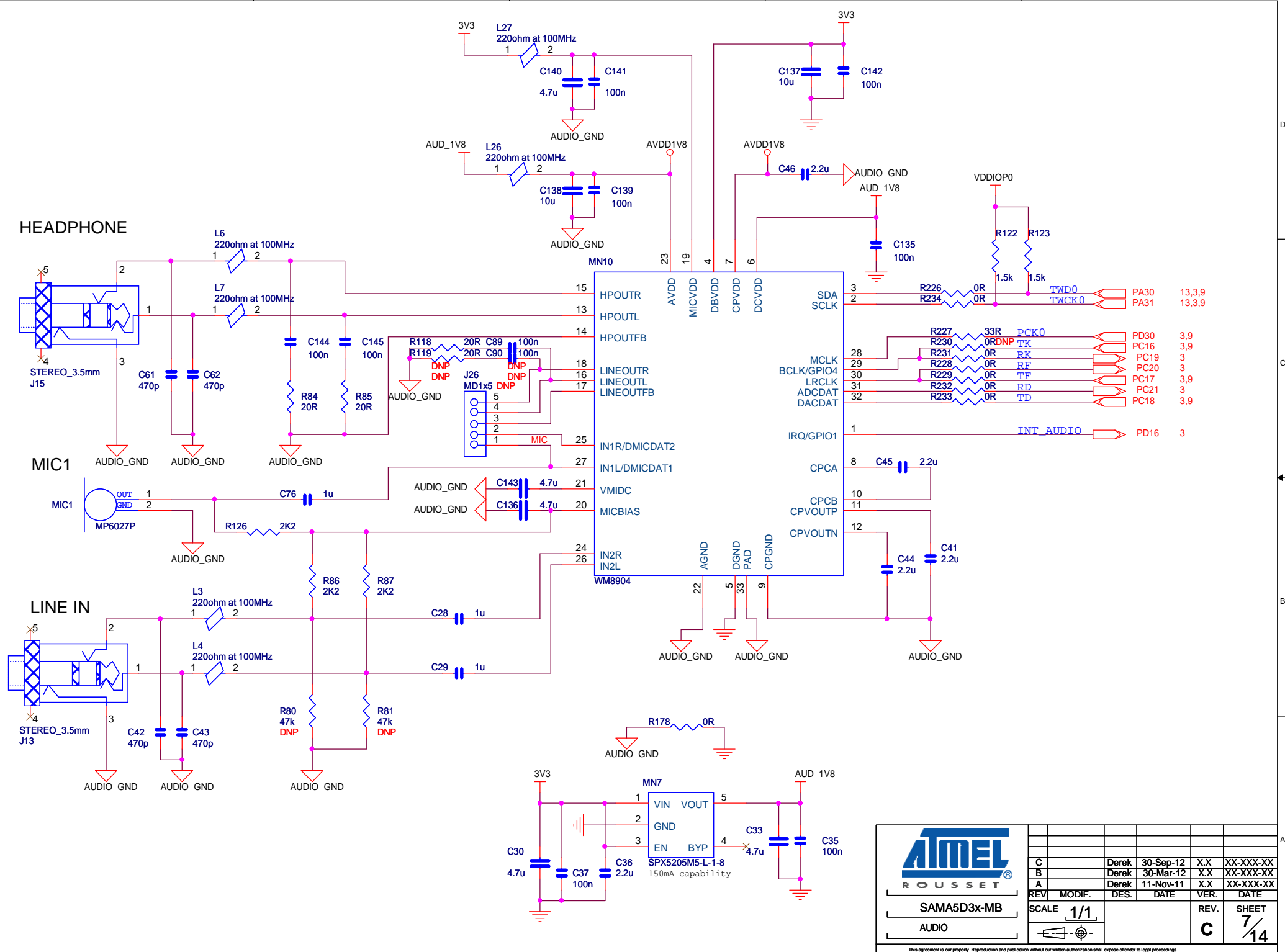


# ZIGBEE INTERFACE



		SAMA5D3x-MB			
CAN & ZIGBEE & USART1		SCALE	1/1	REV.	C
C	Derek	30-Sep-12	X.X	XX-XXX-XX	
B	Derek	30-Mar-12	X.X	XX-XXX-XX	
A	Derek	11-Nov-11	X.X	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE
					SHEET
					6/14

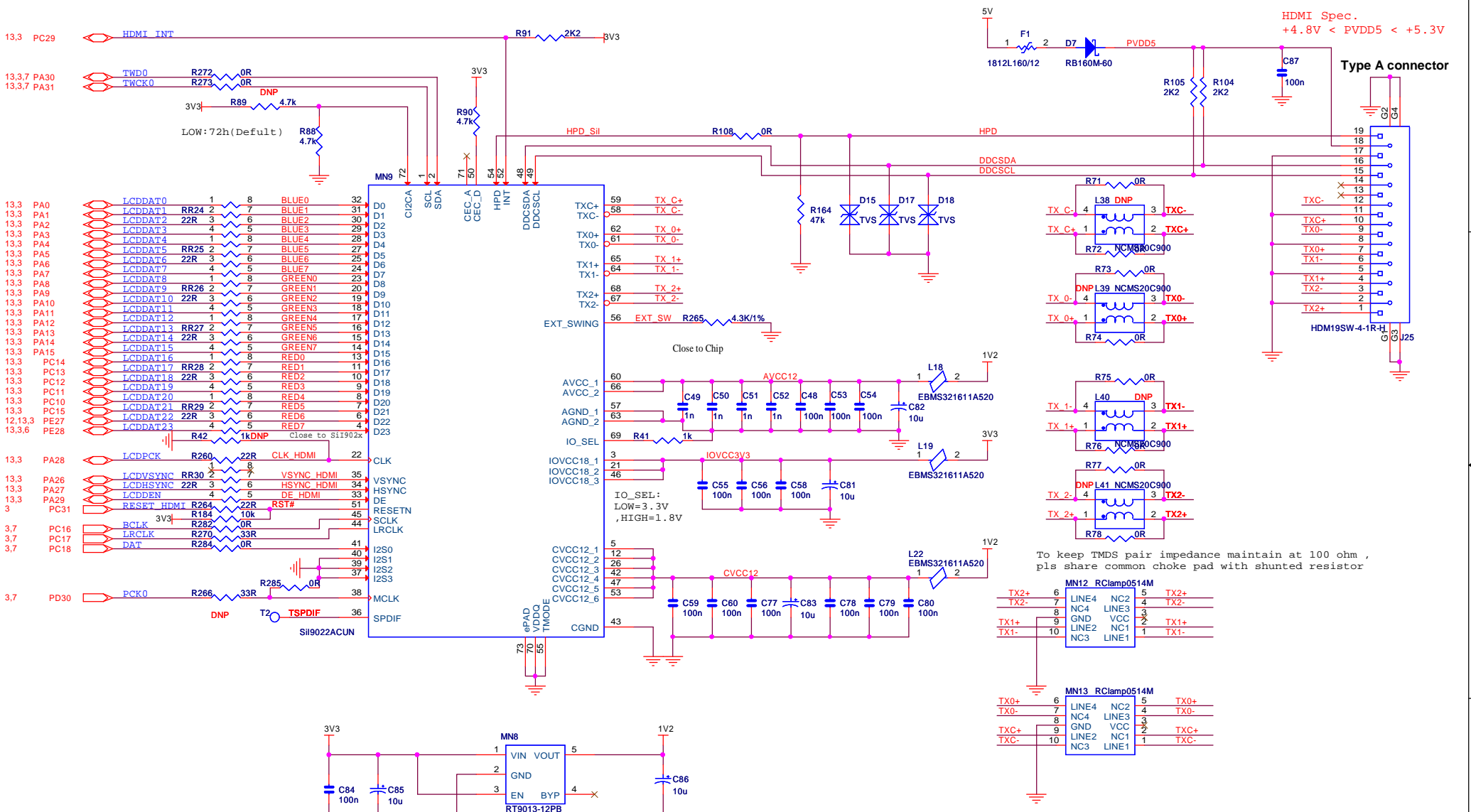
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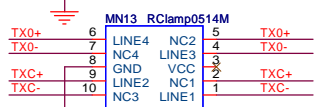
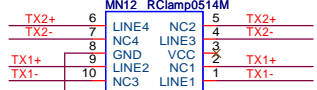
		REV	MODIF.	DES.	DATE	VER.	DATE
		C		Derek	30-Sep-12	XX	XX-XX-XX
<b>SAMA5D3x-MB</b> <b>AUDIO</b>		B		Derek	30-Mar-12	XX	XX-XX-XX
		A		Derek	11-Nov-11	XX	XX-XX-XX
SCALE <b>1/1</b>		REV. <b>C</b>		SHEET <b>7/14</b>			

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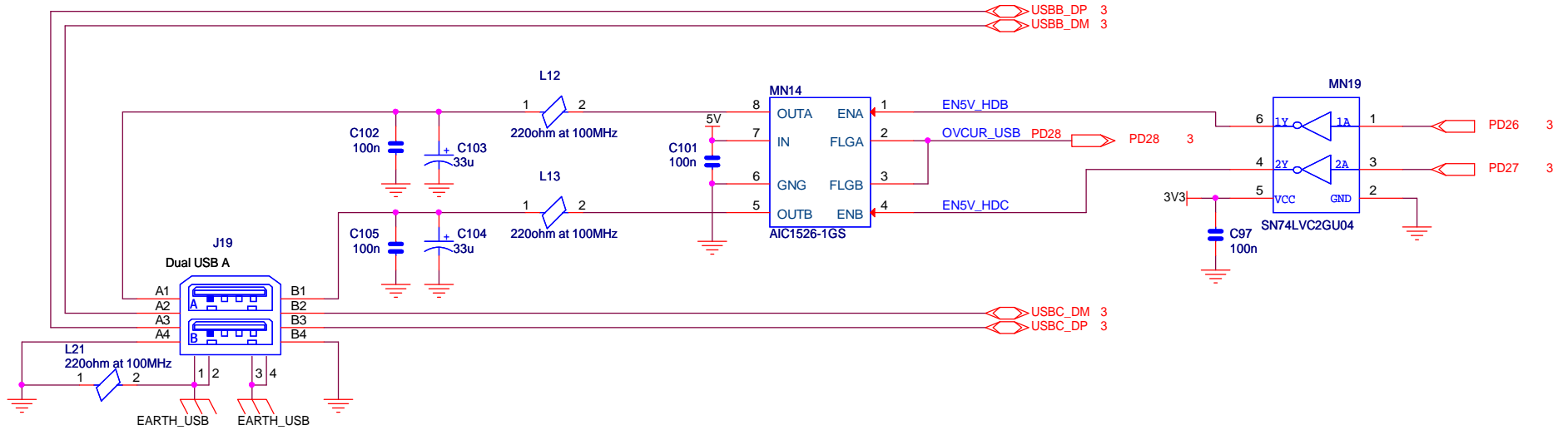
To keep TMDS pair impedance maintain at 100 ohm ,  
pls share common choke pad with shunted resistor



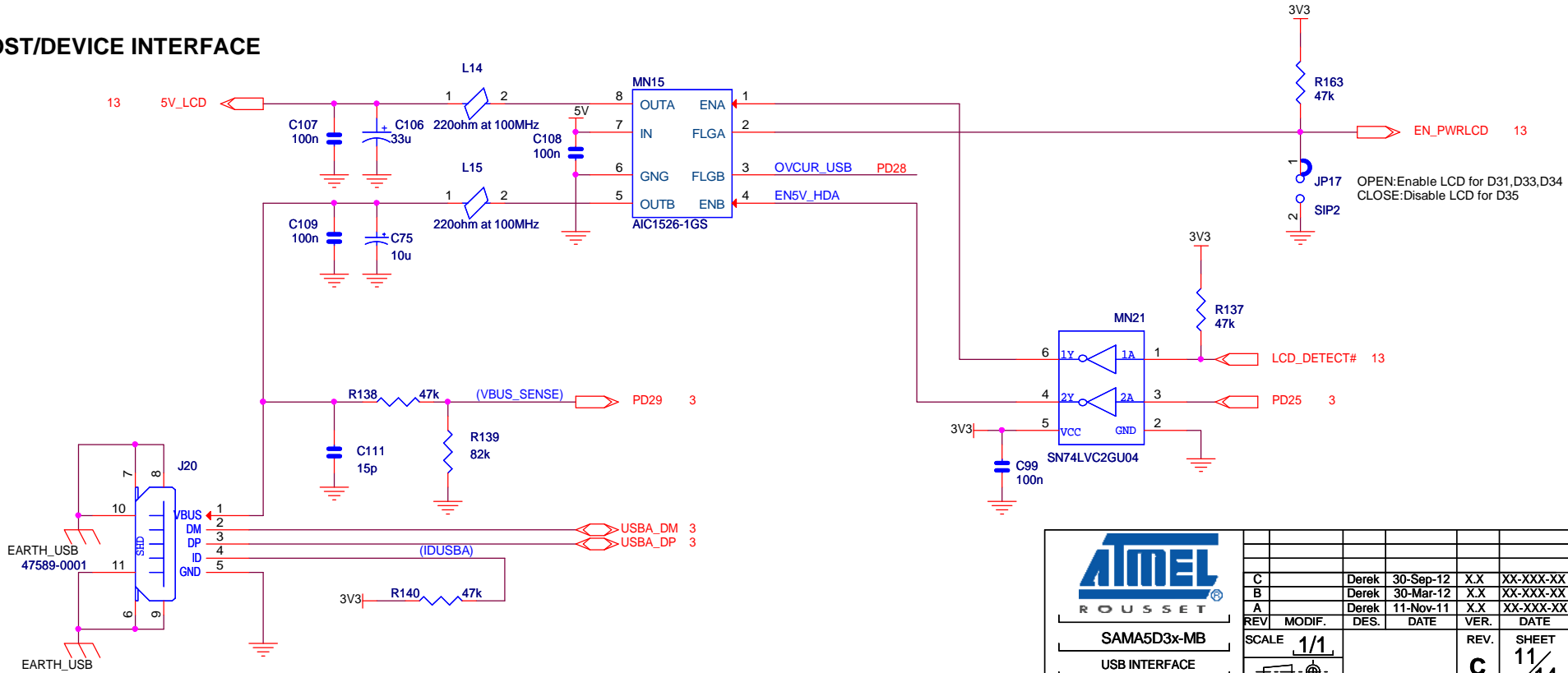
C	Derek	30-Sep-12	X.X	XX-XXX-XX	
B	Derek	30-Mar-12	X.X	XX-XXX-XX	
A	Derek	11-Nov-11	X.X	XX-XXX-XX	
REV	MODIF.	DES.	DATE	REV.	DATE
SCALE 1/1				C	9/14
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# USB HOST B&C INTERFACE



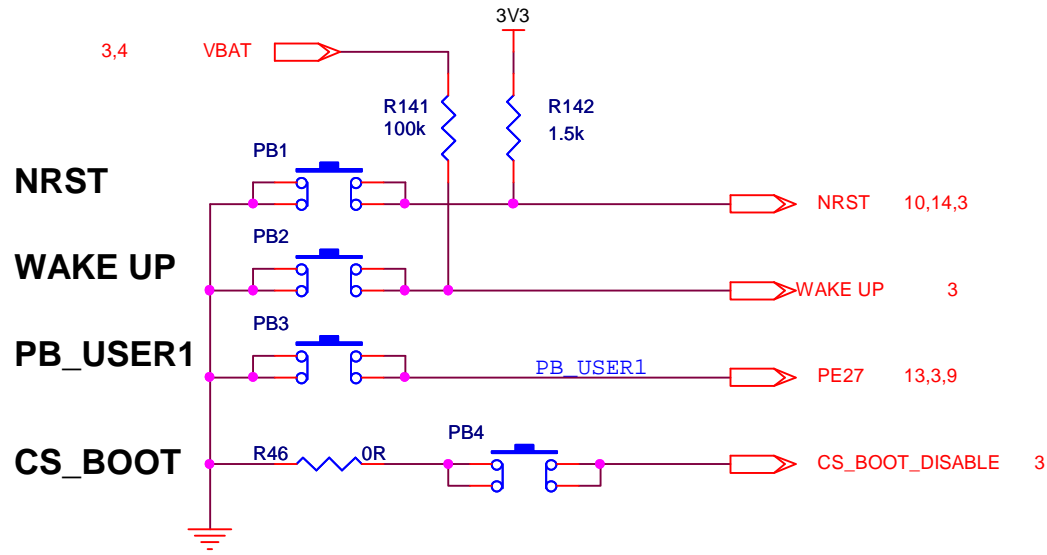
# USB A HOST/DEVICE INTERFACE



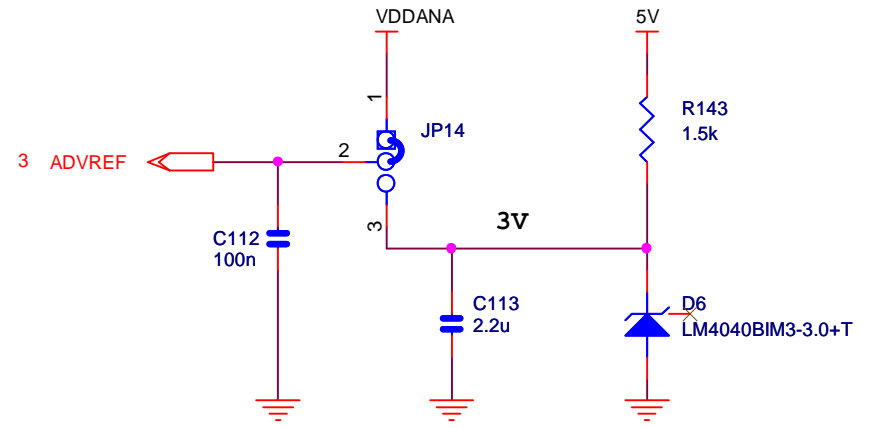
<b>ATMEL</b> ROUSSET					
REV	MODIF.	DES.	DATE	VER.	DATE
C		Derek	30-Sep-12	X.X	XX-XXX-XX
B		Derek	30-Mar-12	X.X	XX-XXX-XX
A		Derek	11-Nov-11	X.X	XX-XXX-XX
SCALE <b>1/1</b>				REV. <b>C</b>	SHEET <b>11/14</b>
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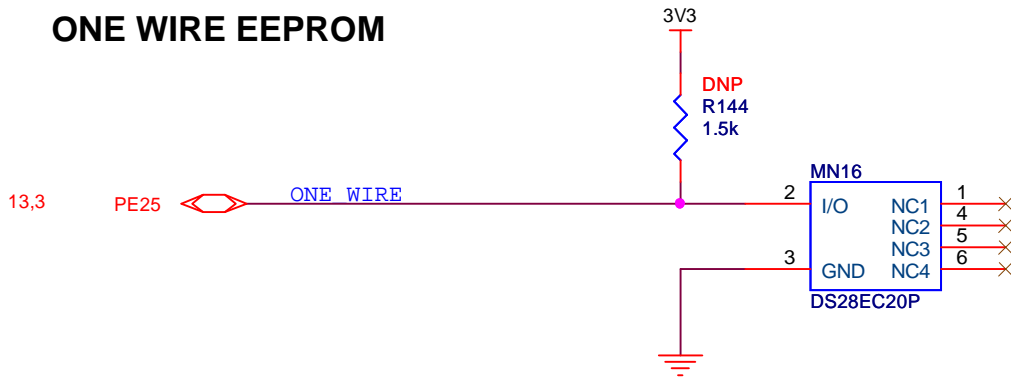
# PUSH BUTTON



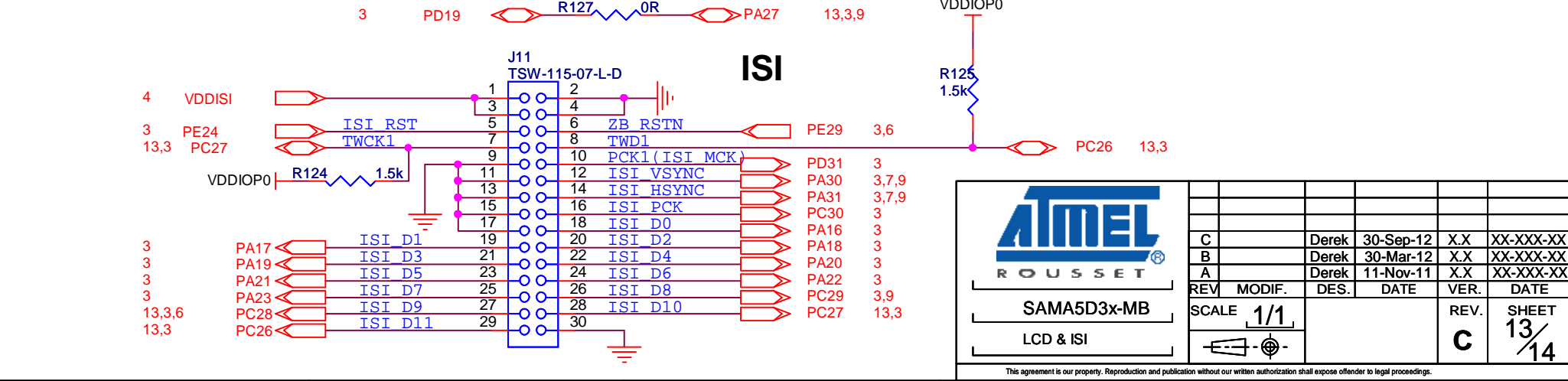
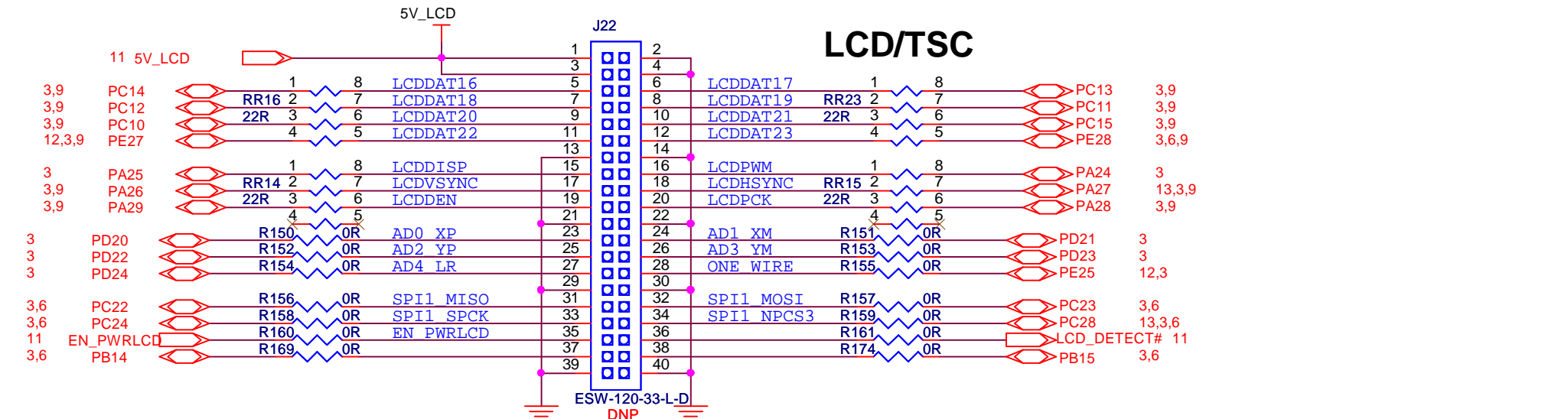
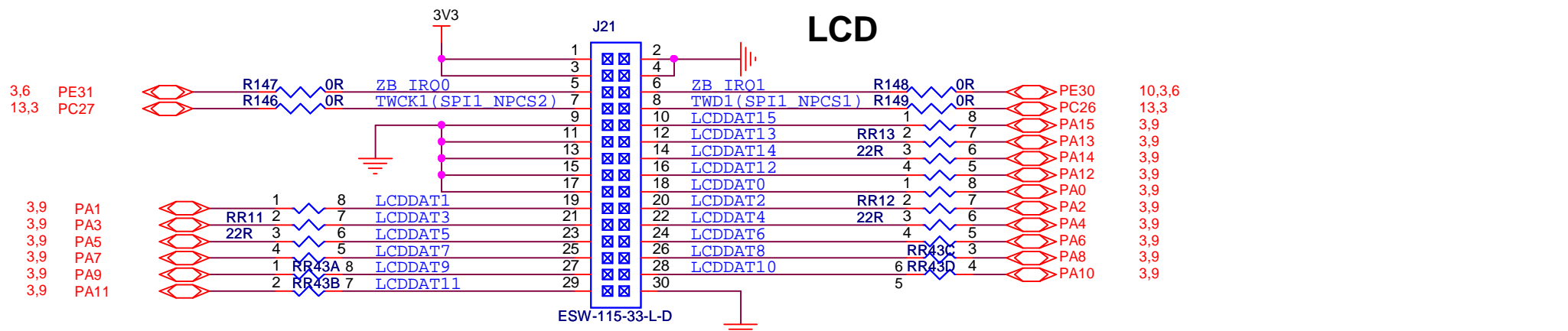
# ANALOG Reference 3V



# ONE WIRE EEPROM



C	Derek	30-Sep-12	X.X	XX-XXX-XX	
B	Derek	30-Mar-12	X.X	XX-XXX-XX	
A	Derek	11-Nov-11	X.X	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE
	SCALE 1/1			REV. C	SHEET 12/14
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**SAMA5D3x-MB**

**LCD & ISI**

C	Derek	30-Sep-12	X.X	XX-XXX-XX
B	Derek	30-Mar-12	X.X	XX-XXX-XX
A	Derek	11-Nov-11	X.X	XX-XXX-XX

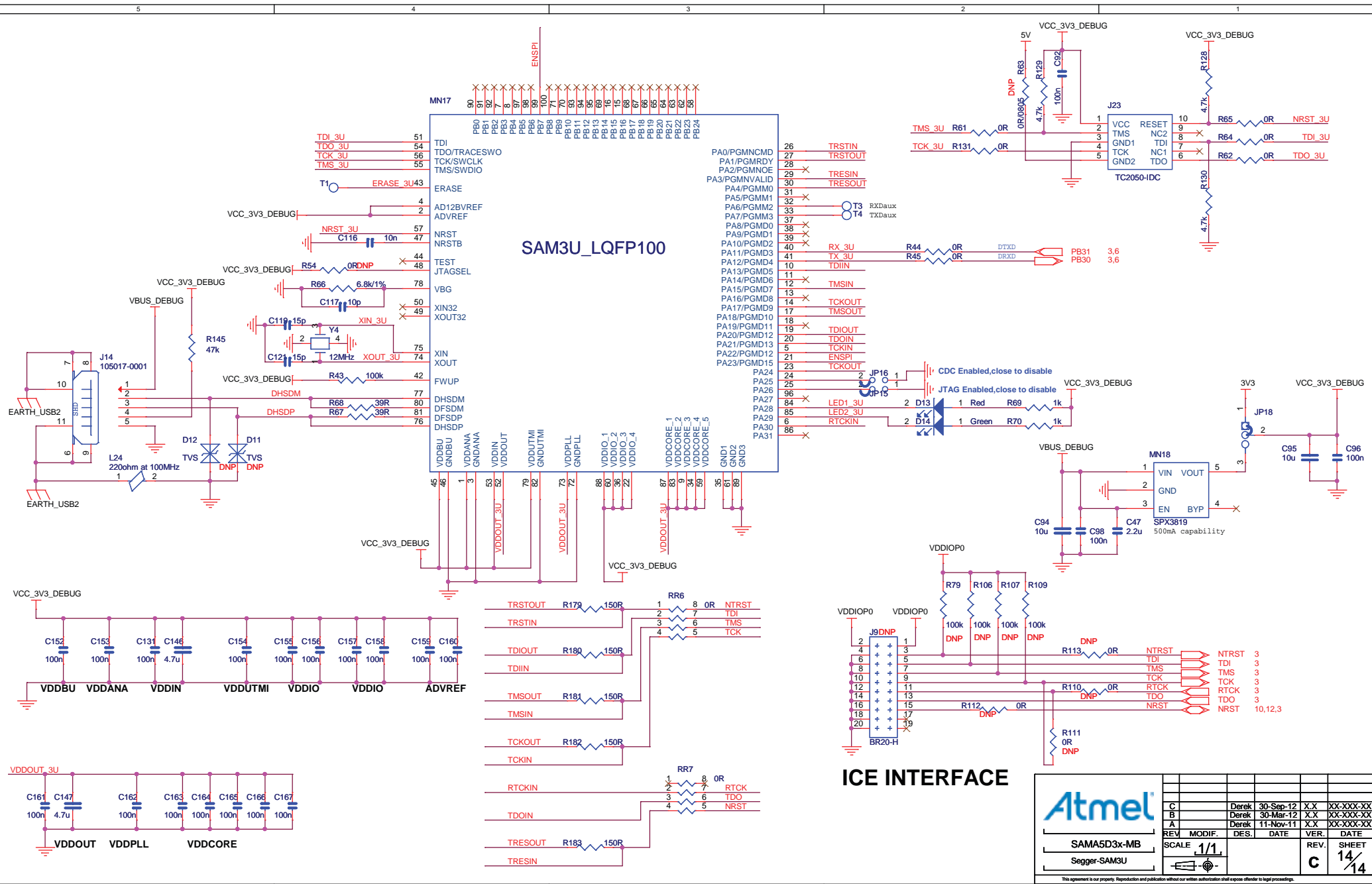
REV	MODIF.	DES.	DATE	VER.	DATE

SCALE **1/1**

REV. **C**

SHEET **13/14**

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### SAM3U\_LQFP100

### ICE INTERFACE

**Atmel**

SAMA5D3x-MB  
Segger-SAM3U

REV.	MODIF.	DES.	DATE	VER.	DATE
C	Derek	30-Sep-12	X.X	XX-XXX-XX	
B	Derek	30-Mar-12	X.X	XX-XXX-XX	
A	Derek	11-Nov-11	X.X	XX-XXX-XX	

SCALE 1/1

REV. C SHEET 14/14

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## 6. Optional Display Module (DM) Board

### 6.1 DM Board Overview

The DM board integrates a 5.0" TFT LCD module with touchscreen, as well as four QTouch pads.

Figure 6-1. DM Board



#### 6.1.1 Equipment List

The DM board components are:

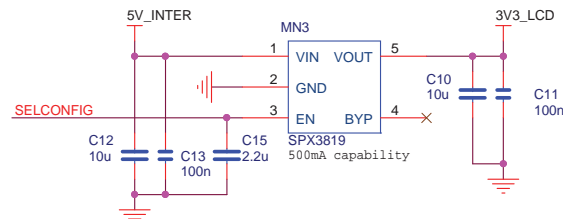
- One 5.0" TFT LCD module
- LCD back light driver
- 3.3V regulator
- QTouch device
- 1-wire device

#### 6.1.2 Function Blocks

##### 6.1.2.1 3.3V Regulator

The 5-0\_WVGA\_R\_AEA-DM Board features its own LDO for local power regulation. It accepts DC 5V power from 500 mA high-side power switch on EK and outputs a regulated +3.3V to most other circuits on the board.

Figure 6-2. DM Power Supply



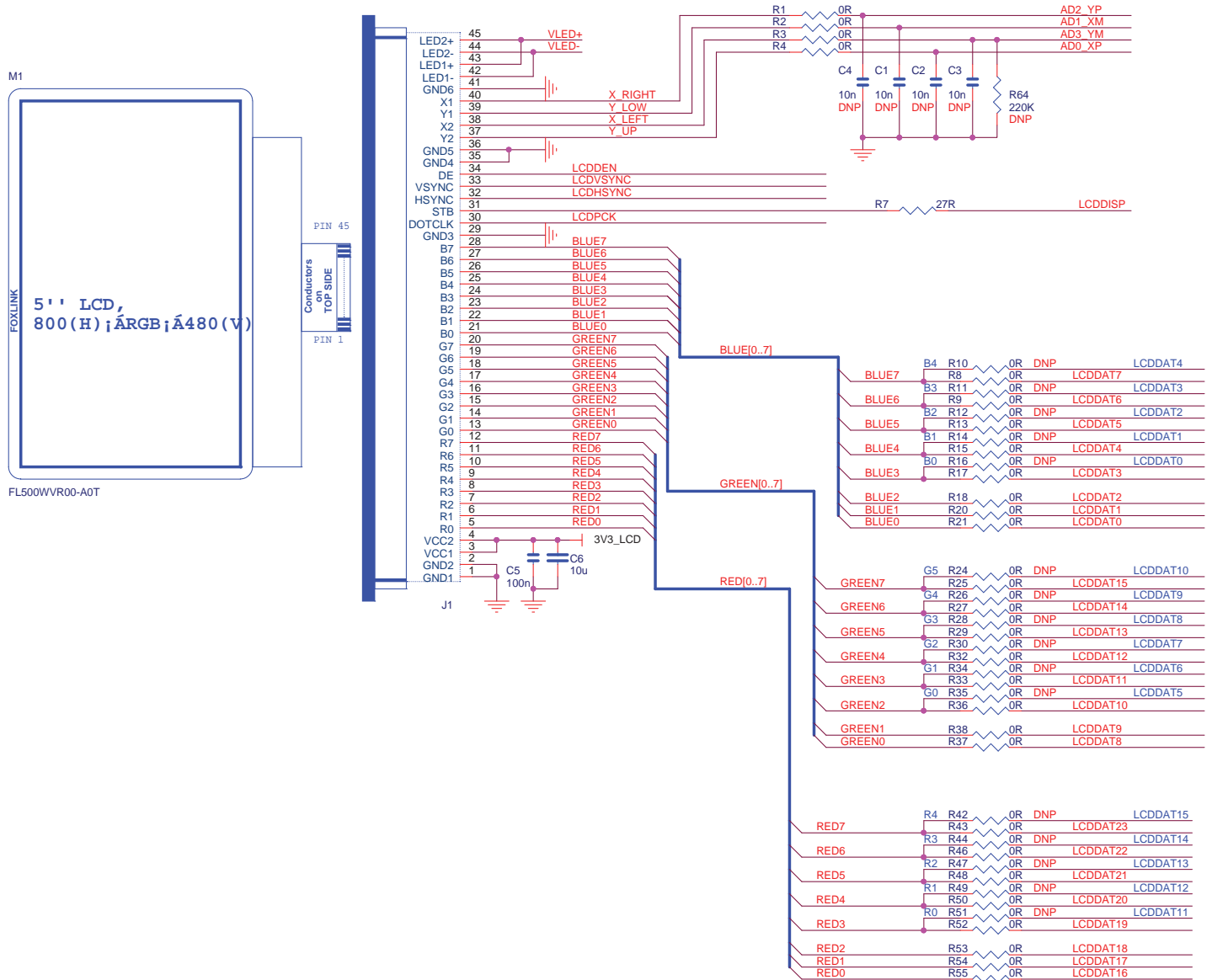
### 6.1.3 TFT LCD with Touch Panel

The 5-0\_WVGA\_R\_AEA-DM features an LCD controller. The 5" 800x480 LCD provides the DM with a low-power LCD display feature, backlight unit and a touch panel, similar to that used on commercial PDAs.

Graphics and text can be displayed on the dot matrix panel with up to 16 million colors by supplying 24-bit data signals (8bit x RGB by default) or 16-bit data signals (5+6+5bit x RGB in option). This allows the user to develop graphical user interfaces for a wide variety of applications.

**Warning:** Never connect/disconnect the LCD display from the board while the power supply is on. This can damage both boards.

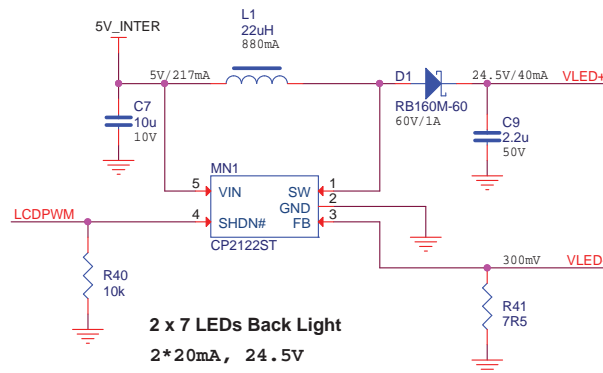
Figure 6-3. LCD with Touch Panel



### 6.1.4 Backlight

The backlight voltage is generated from a CP2122ST/CP2123ST boost converter. It is powered directly by the 5V DC from the EK board. The backlight level is controlled by a PWM signal generated from the SAMA5D3 series processor.

Figure 6-4. DM Back Light Control

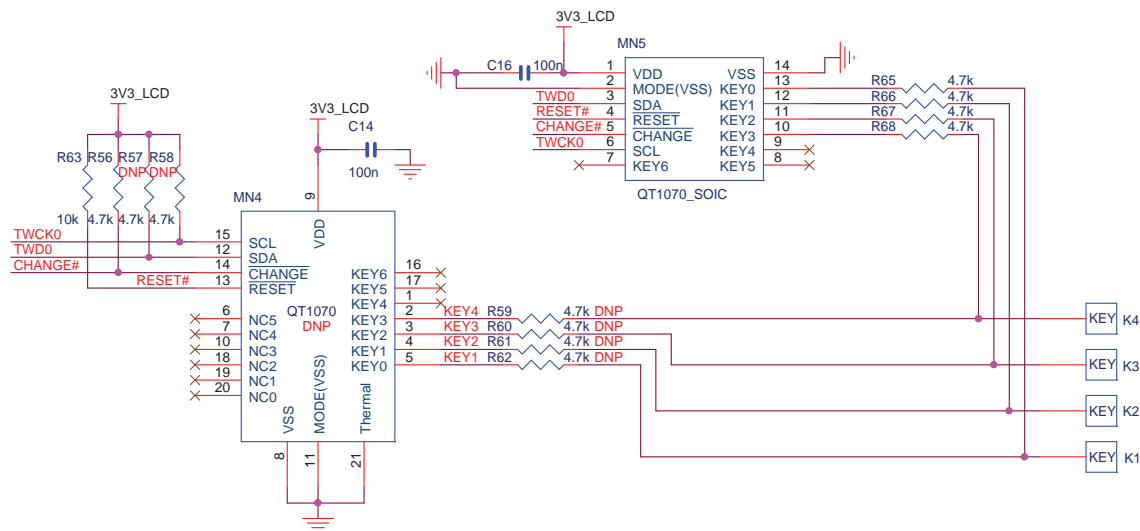


### 6.1.5 QTouch

The 5-0\_WVGA\_R\_AEA-DM board carries a QTouch device driven through a TWI interface. It manages four capacitive touch buttons directly printed on the PCB.

There is dual footprint for the QTouch device. SOIC is the default mounted one.

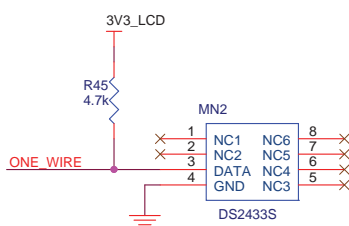
Figure 6-5. DM QTouch



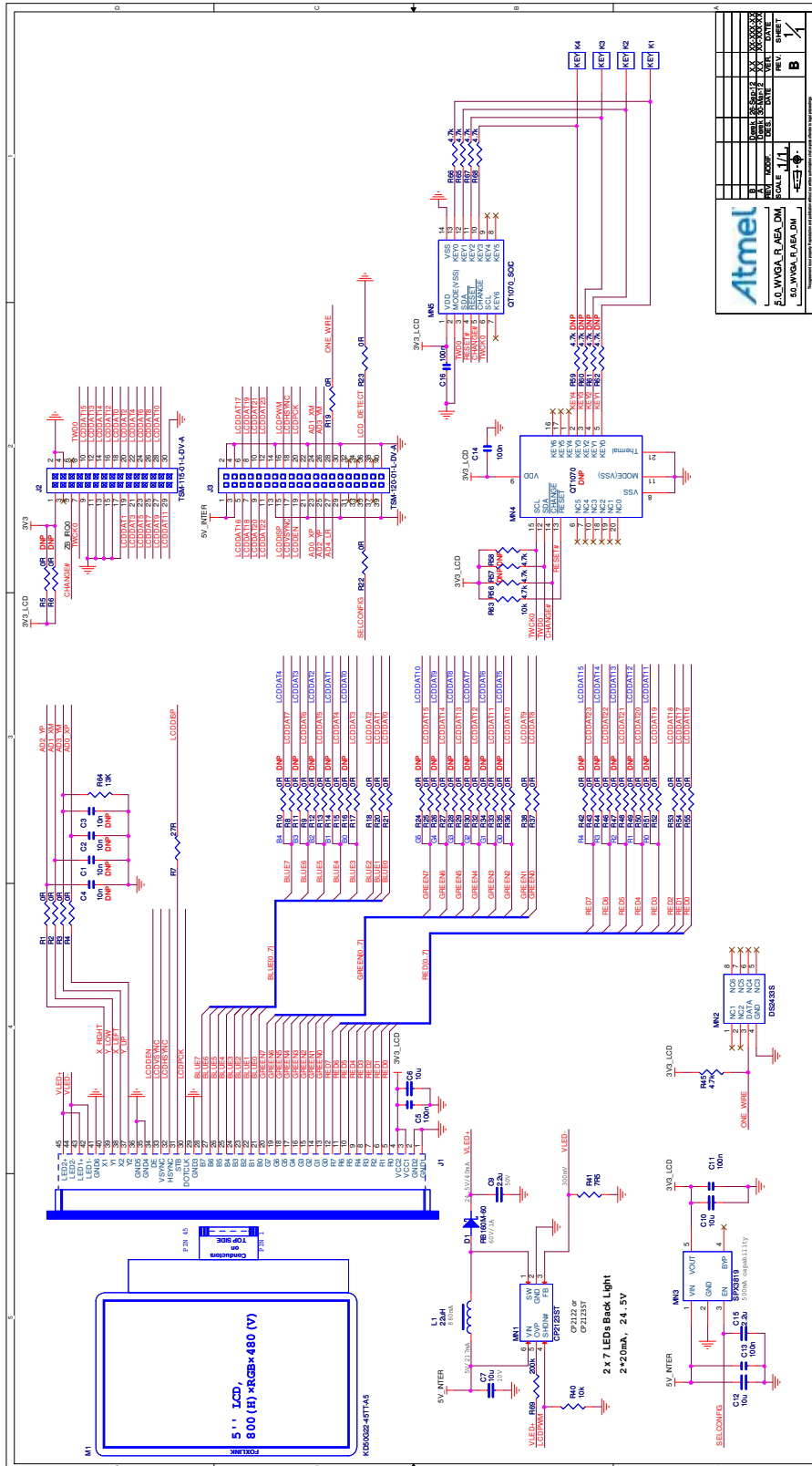
### 6.1.6 1-Wire

The 5-0\_WVGA\_R\_AEA-DM board also uses a 1-wire device as a “soft label” to store the information such as chip type, manufacture name, production date, etc.

Figure 6-6. DM 1-Wire



## 6.2 Schematics



Atmel	
5.0 WAGA R AEA DM	
5.0 WAGA P AEA DM	
SCALE	1:1
DATE	REV. DATE
REV. NO.	REV. SHEET
B	1/1

## 7. Troubleshooting and Recommendations

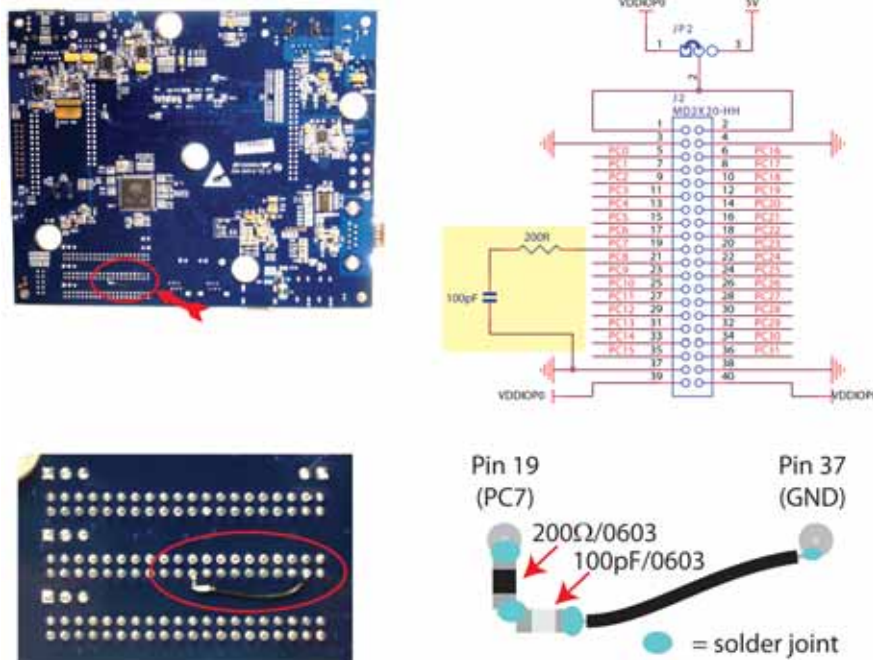
### 7.1 Errata

#### 7.1.1 Impedance Mismatch on Revision C of the SAMA5D3x Main Board

There is an impedance mismatch on the revision C of the SAMA5D3x main board, impacting the clock signal of the Ethernet PHY chip (MN20, KSZ8051RNL). This leads to a non-optimal data transmission on the ETH1 channel (J24), with timeouts and retries occurring from time to time.

**Resolution:** Add a line termination on signal PC7. Connect PC7 to ground through a 200 Ohm resistor in series with a 100pF ceramic capacitor. The connection point must be done at Pin 19 of Connector J2. [Figure 7-1](#) shows how and where to apply the fix.

Figure 7-1. Fixing An Impedance Mismatch on the Revision C of the SAMA5D3x Main Board





## 8. Revision History

Table 8-1. Revision History

Document	Comments	Change Request Ref.
11180B	Changed document layout, including section numbering. Changed Embest to Embest/Flextronics throughout document.	9364
	In <a href="#">"Introduction"</a> and <a href="#">"Contents"</a> : Added SAMA5D36, SAMA5D36-EK and SAMA5D36-CM to lists of available references and to information for display modules (DM). Also throughout document.	9364
	In <a href="#">Table 1-1 "Evaluation Kit Specifications"</a> , removed information on temperature and relative humidity. Added information on CE and FCC compliancy. Added SAMA5D36-EK.	9363
	In <a href="#">Table 4-1 "CM Board Implementation"</a> , updated boards available from manufacturers.	9360
	In <a href="#">Table 4-2 "CPU Module Specifications"</a> , removed 'optional' from details on NOR in Memory row.	9363
	In <a href="#">Section 4.2.3 "Configuration Items"</a> , removed "Dual ON/OFF switch for NAND Flash" and replaced with "One jumper for".	
	In <a href="#">Table 4-3 "Boot Options"</a> , in row BMS OPEN: Added "...followed by:" after "ROM Boot" and added SAM-BA after TWI in column Type. In column Note, changed "Default boot on embedded ROM" to "Default boot is from embedded ROM". In row BMS CLOSE, changed "Boot on external NOR Flash memory" to "Boot from external NOR Flash memory".	
	<a href="#">Section 4.2.4.1 "Boot Configuration"</a> : Revised throughout.	
	<a href="#">Section 4.3.3 "Reset Circuitry"</a> : Changed information on JTAG reset.	
	<a href="#">Section 4.3.6 "Serial Peripheral Interface Controller (SPI)"</a> : Revised throughout.	
	<a href="#">Section 4.3.9 "Indicators"</a> : Removed specific information on red and blue LEDs. Added information on control by GPIO lines.	
	Added <a href="#">Section 4.4.2 "CPU Module Revision E Schematics"</a> .	9364
	<a href="#">Table 5-1 "MB Technical Specifications"</a> , Mass Storage Interface: Updated information on all types of cards supported.	9363
	- Added information on RoHS and CE and FCC compliancy. - Removed temperature range information.	
<a href="#">Section 5.2.3 "Debug JTAG/ICE and DBGU"</a> : Modified details of ATSAM3U4C.	9360	
<a href="#">Section 5.2.3.1 "Disabling J-Link-OB-ATSAM3U4C"</a> : Revised throughout.		
<a href="#">Section 5.2.3.2 "Hardware UART via CDC"</a> : Revised throughout.		
<a href="#">Section 5.2.4 "USART"</a> : Revised throughout.		
<a href="#">Section 5.2.6 "Ethernet 10/100 (EMAC) Port"</a> : Revised throughout.		
<a href="#">Section 5.2.10 "CAN Bus"</a> : Removed mention of two ports for connector J27.		
<a href="#">Section 5.2.14 "LED Indicators"</a> : Revised throughout.		
<a href="#">Section 5.2.15 "Pushbutton Switches"</a> : Changed fourth bullet.		
Added <a href="#">Section 7.1 "Errata"</a> with <a href="#">Section 7.1.1 "Impedance Mismatch on Revision C of the SAMA5D3x Main Board"</a> .	8803	
11180A	First issue	



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