Enpirion® Power Datasheet

EN5319QI 1.5A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor

Description

The EN5319QI is a highly integrated, low profile, highly efficient, 1.5A synchronous buck power system on a chip (PowerSoC™). The device features an advance integrated inductor, integrated MOSFETs, a PWM voltage-mode controller, and internal compensation providing the smallest possible solution size.

The EN5319QI is a member of the EN53x9QI family of pin compatible and interchangeable devices. The pin compatibility enables an easy to use scalable family of products covering the load range from 1.5A up to 3A in a low profile 4mm x 6mm x 1.1mm QFN package.

The EN5319QI operates at high switching frequency and allows for the use of tiny MLCC capacitors. It also enables a very wide control loop bandwidth providing excellent transient performance and reduced output impedance. The internal compensation is designed for unconditional stability across all operating conditions.

Altera's Enpirion integrated inductor solution significantly helps to reduce noise. The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements. Altera's Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Features

- Integrated Inductor
- Solution Footprint as Small as 50 mm^2
- Low Profile, 1.1mm
- High Reliability Solution: 42,000 Years MTBF
- High Efficiency, up to 95 %
- Low Output Ripple Voltage; <4mV_{P-P} Typical
- 2.4 V to 5.5 V Input Voltage Range
- 1.5A Continuous Output Current Capability
- Output Enable and Power OK Signal
- Pin Compatible w/ EN5329QI 2A and EN5339QI 3A
- Under Voltage Lockout, Over Current, Short Circuit, and Thermal Protection
- RoHS Compliant; Halogen Free; 260°C Reflow

Applications

- Applications with Low Profile Requirement such as SSD and Embedded Computing
- SAN/NAS Accelerator Appliances
- FPGA, ASSP, PLD, ASIC, and Processors
- Noise Sensitive Applications

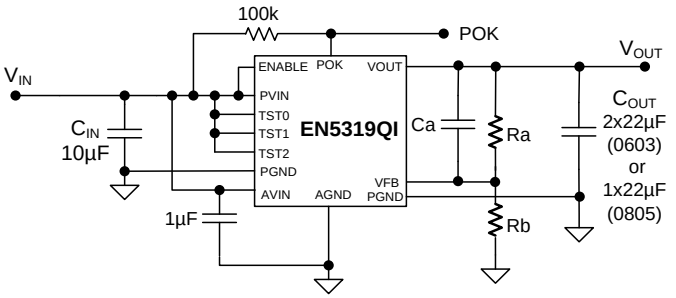


Figure 1. Simplified Applications Circuit

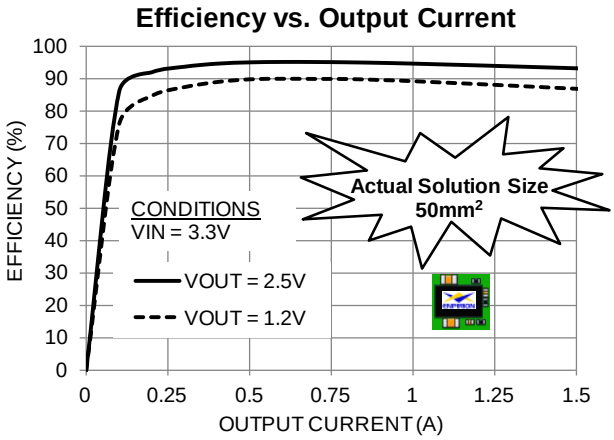


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	Temp Rating (°C)	Package Description
EN5319QI	EN5319	-40 to +85	24-pin (4mm x 6mm x 1.1mm) QFN T&R
EVB-EN5319QI	EN5319	QFN Evaluation Board	

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

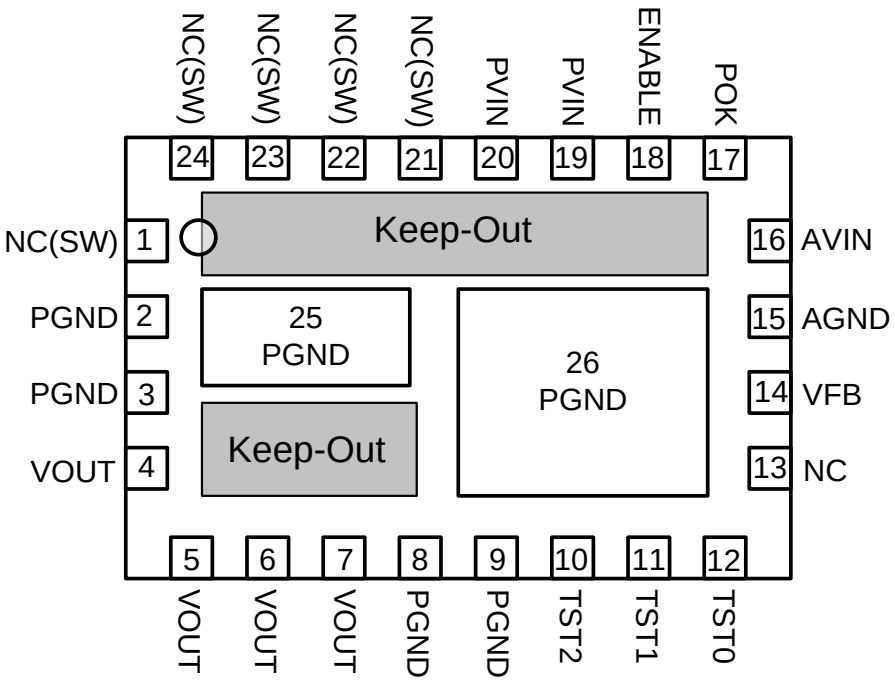


Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Grey area highlights exposed metal on the bottom of the package that is not to be mechanically or electrically connected to the PCB. There should be no traces on PCB top layer under these keep out areas.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

PIN	NAME	FUNCTION
1, 21-24	NC(SW)	NO CONNECT: These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
2-3, 8-9	PGND	Input and output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT, PVIN descriptions and Layout Recommendation for more details.
4-7	VOUT	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins 8 and 9. See layout recommendation for details
10	TST2	Test Pin. For Altera internal use only. Connect to AVIN at all times.
11	TST1	Test Pin. For Altera internal use only. Connect to AVIN at all times.

PIN	NAME	FUNCTION
12	TST0	Test Pin. For Altera internal use only. Connect to AVIN at all times.
13	NC	NO CONNECT: This pin must be soldered to PCB but not electrically connected to any other pin or to any external signal, voltage, or ground. This pin may be connected internally. Failure to follow this guideline may result in device damage.
14	VFB	This is the external feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor is required parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage equal to 0.600V.
15	AGND	The quiet ground for the control circuits. Connect to the ground plane with a via right next to the pin.
16	AVIN	Analog input voltage for the control circuits. Connect this pin to the input power supply (PVIN) at a quiet point. Decouple with a 1uF capacitor to AGND.
17	POK	POK is an open drain output. Refer to Power OK section for details. Leave POK open if unused.
18	ENABLE	Output Enable. A logic high level on this pin enables the output and initiates a soft-start. A logic low signal disables the output and discharges the output to GND. This pin must not be left floating.
19-20	PVIN	Input power supply. Connect to input power supply and place input filter capacitor(s) between these pins and PGND pins 2 to 3.
25,26	PGND	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes. See Layout Recommendation section.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on : PVIN, AVIN, VOUT		-0.3	6.5	V
Voltages on: ENABLE, POK, TST0, TST1, TST2		-0.3	V_{IN}+0.3	V
Voltages on: VFB		-0.3	2.7	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (Human Body Model)			2000	V
ESD Rating (Charge Device Model)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range (Note 1)	V_{OUT}	0.6	$V_{IN} - V_{DO}$	V
Output Current	I_{OUT}	0	1.5	A
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (Note 2)	θ_{JA}	36	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	6	°C/W
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	15	°C

Note 1: V_{DO} (dropout voltage) is defined as (I_{LOAD} x Dropout Resistance). Please see Electrical Characteristics Table.

Note 2: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: VIN = 5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

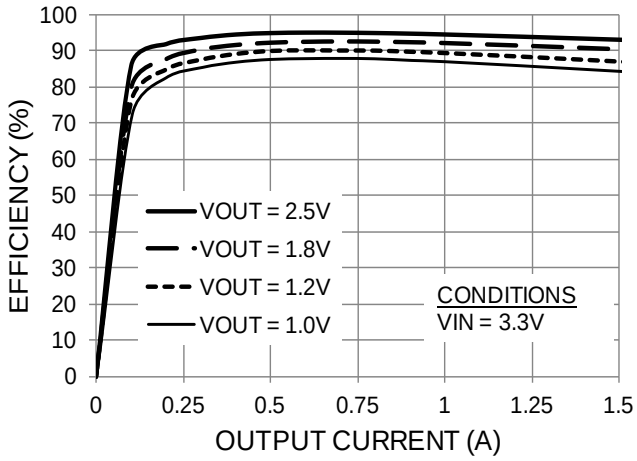
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Feedback Node Initial Accuracy	V_{VFB}	T_A = 25°C; V_{IN} = 5V I_{LOAD} = 100 mA	0.588	0.600	0.612	V
Output Variation (Note 3) (Line, Load, Temperature)	V_{OUT}	2.4V ≤ V_{IN} ≤ 5.5V 0 ≤ I_{LOAD} ≤ 1.5A	-3		+3	%
VFB, ENABLE, TST0/1/2 Pin Input Current (Note 4)					+/-40	nA
Shutdown Current		ENABLE Low		20		µA
Under Voltage Lock-out – V_{IN} Rising	V_{UVLOR}	Voltage Above Which UVLO is Not Asserted		2.2		V
Under Voltage Lock-out – t_{VIN} Falling	V_{UVLOF}	Voltage Below Which UVLO is Asserted		2.1		V
Soft-start Time		Time from Enable High (Note 4)	0.91	1.40	1.89	ms
Dropout Resistance				150	300	mΩ
ENABLE Voltage Threshold		Logic Low Logic High	0.0 1.4		0.4 V_{IN}	V
POK Threshold		V_{OUT} Rising		92		%
POK Threshold		V_{OUT} Falling		90		%
POK Low Voltage		I_{SINK} = 1 mA		0.15	0.4	V
POK Pin V_{OH} Leakage Current		POK High		0.5	2	µA
Current Limit Threshold		2.4V ≤ V_{IN} ≤ 5.5V	3.5	5		A
Operating Frequency	F_{OSC}			3.2		MHz
Output Ripple Voltage	V_{RIPPLE}	C_{OUT} = 2 x 22 µF 0603 X5R MLCC, V_{OUT} = 3.3 V, I_{LOAD} = 1.5A		4		mV_{P-P}
		C_{OUT} = 2 x 22 µF 0603 X5R MLCC, V_{OUT} = 1.8 V, I_{LOAD} = 1.5A		4		mV_{P-P}

Note 3: Output voltage variation is based on using 0.1% accuracy resistor values.

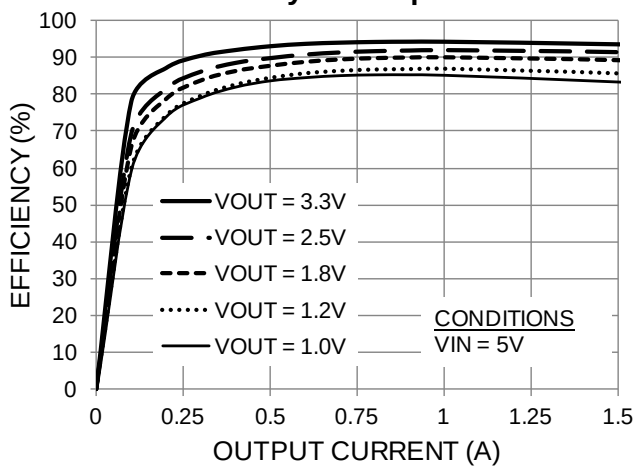
Note 4: Parameter not production tested but is guaranteed by design.

Typical Performance Curves

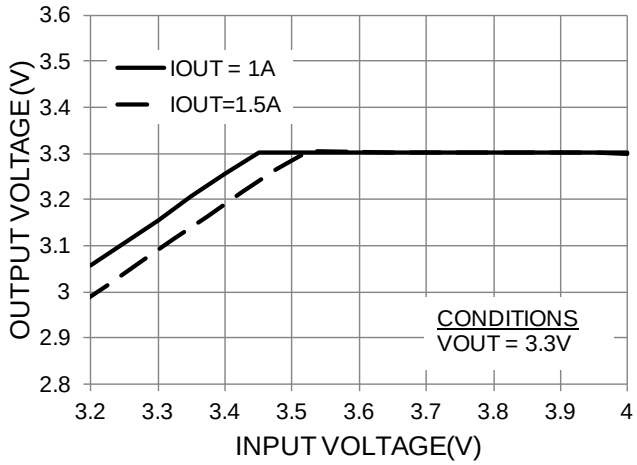
Efficiency vs. Output Current



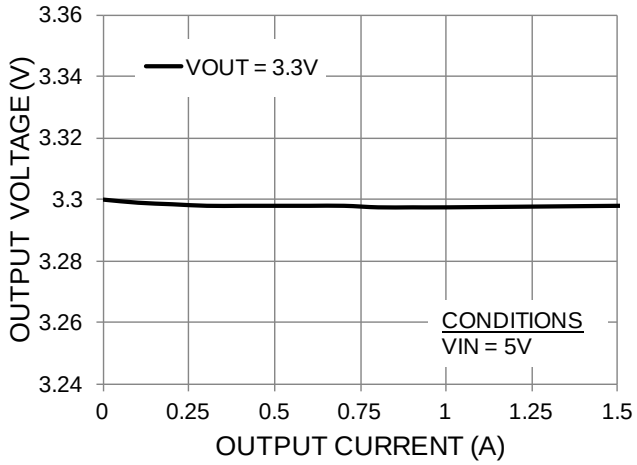
Efficiency vs. Output Current



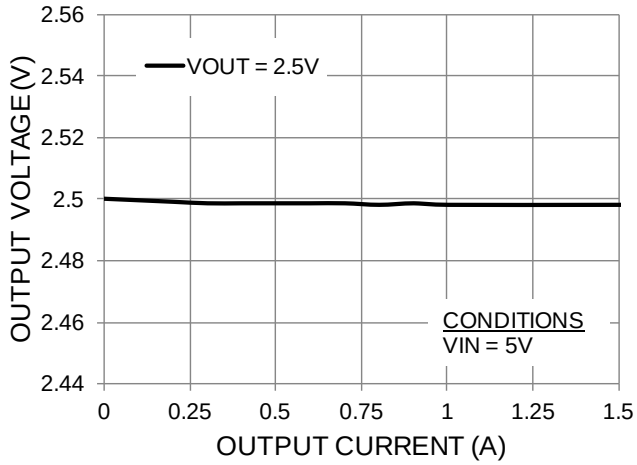
Dropout Voltage



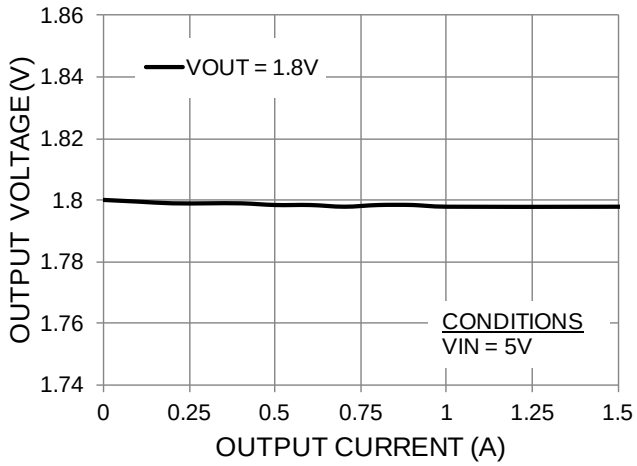
Output Voltage vs. Output Current



Output Voltage vs. Output Current

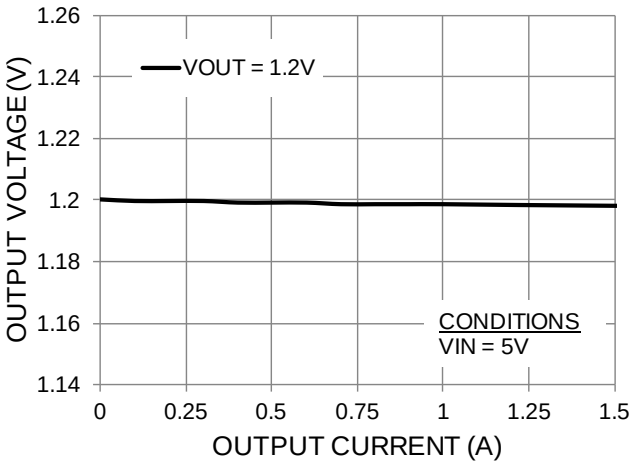


Output Voltage vs. Output Current

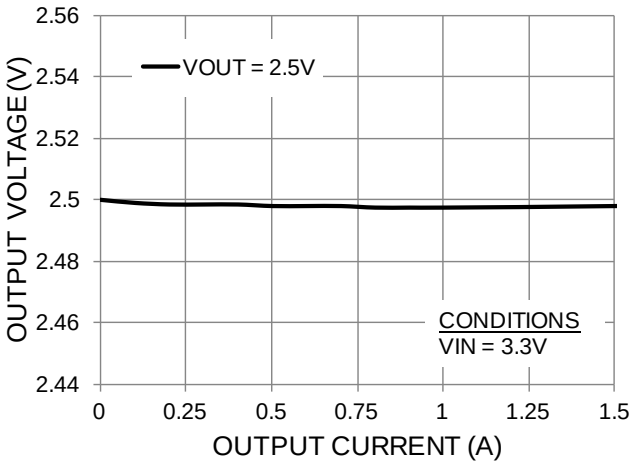


Typical Performance Curves (Continued)

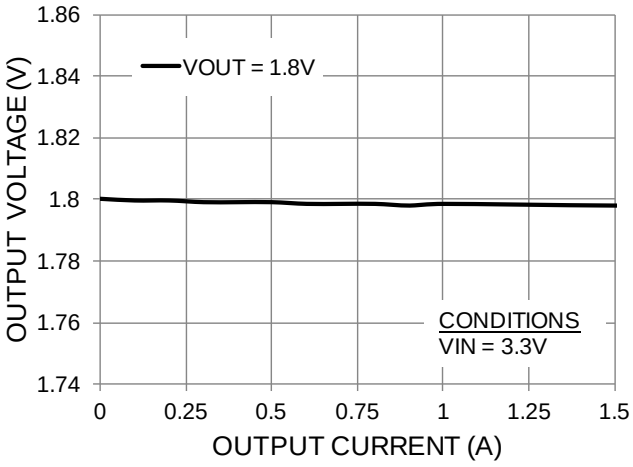
Output Voltage vs. Output Current



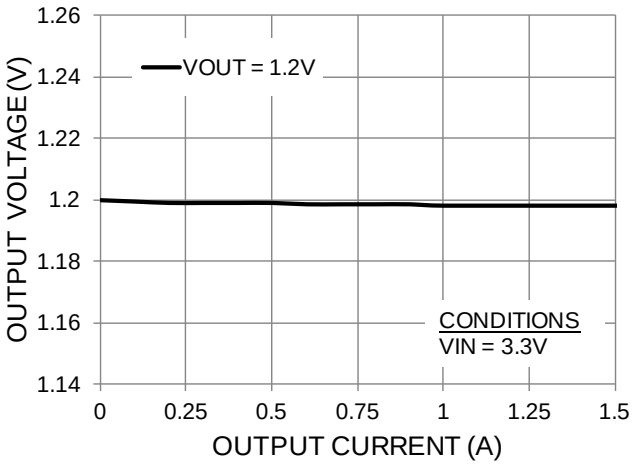
Output Voltage vs. Output Current



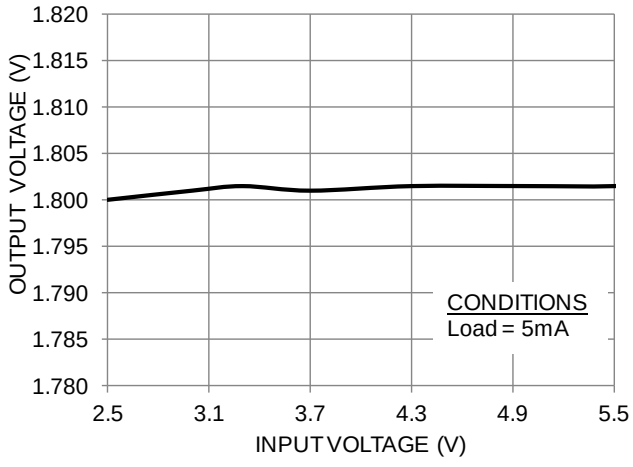
Output Voltage vs. Output Current



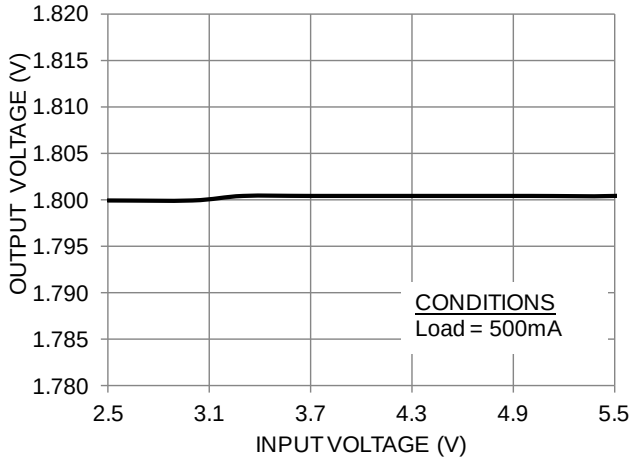
Output Voltage vs. Output Current



Output Voltage vs. Input Voltage

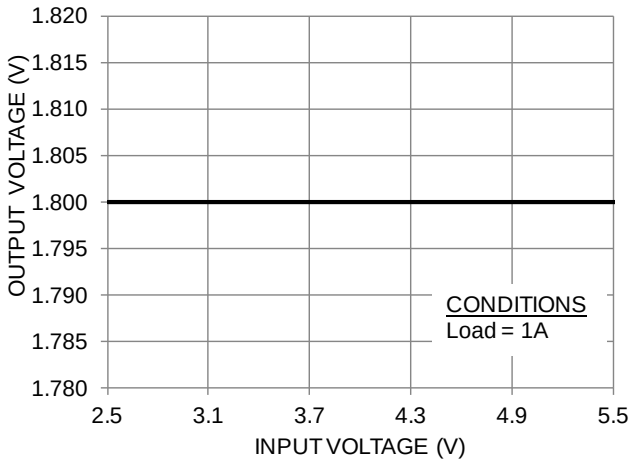


Output Voltage vs. Input Voltage

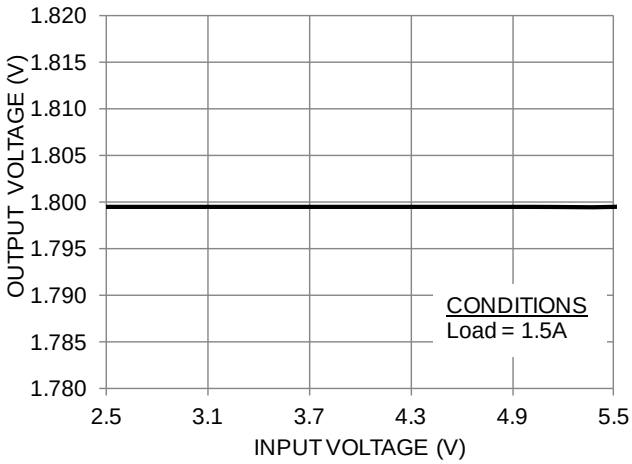


Typical Performance Curves (Continued)

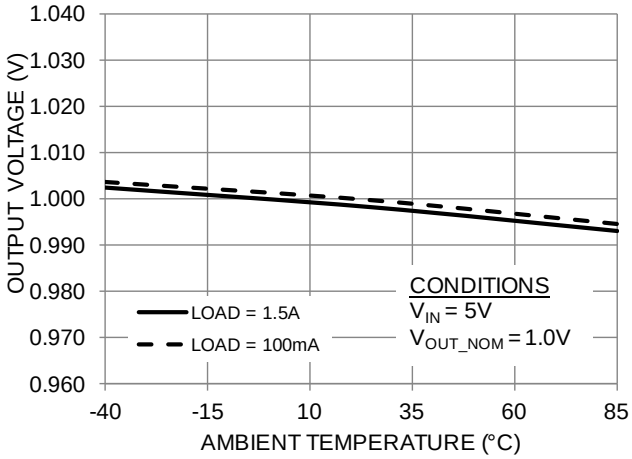
Output Voltage vs. Input Voltage



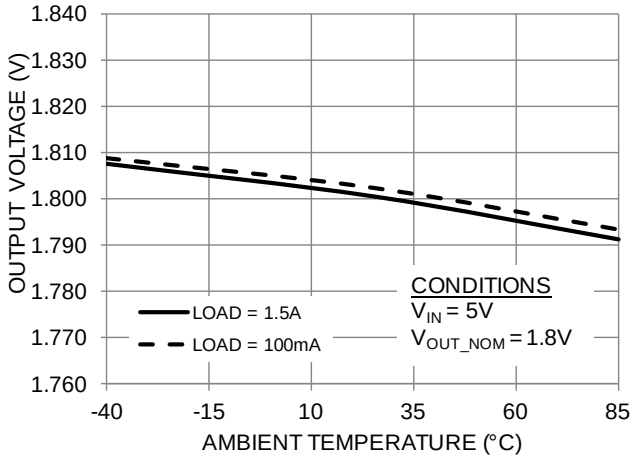
Output Voltage vs. Input Voltage



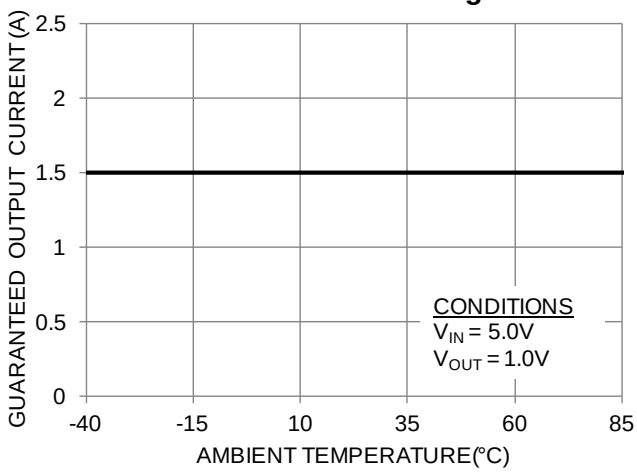
Output Voltage vs. Temperature



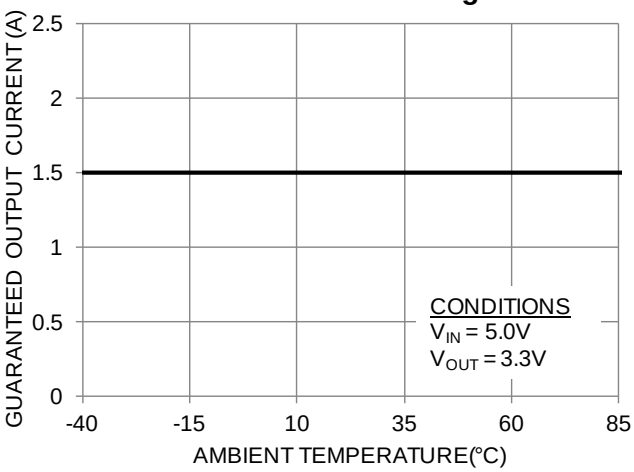
Output Voltage vs. Temperature



No Thermal Derating

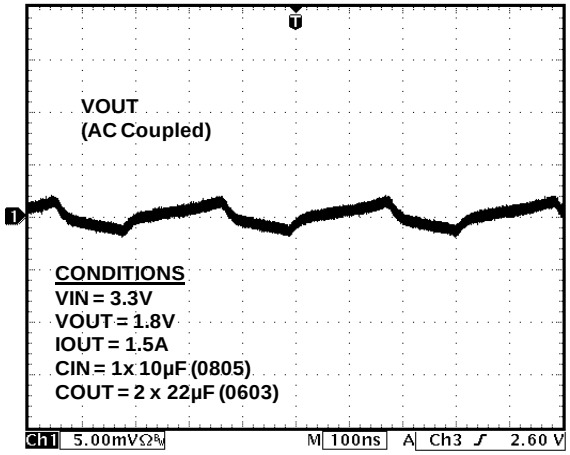


No Thermal Derating

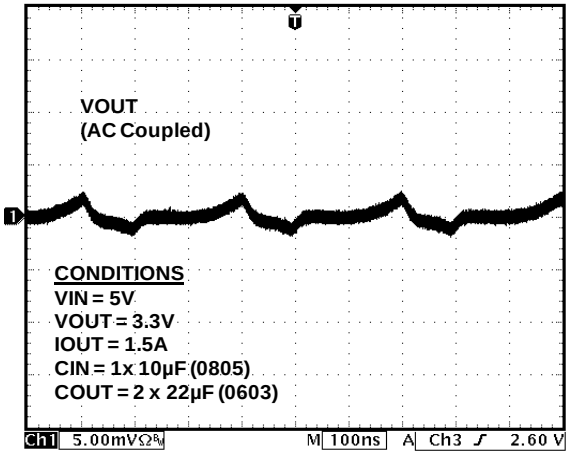


Typical Performance Characteristics (Continued)

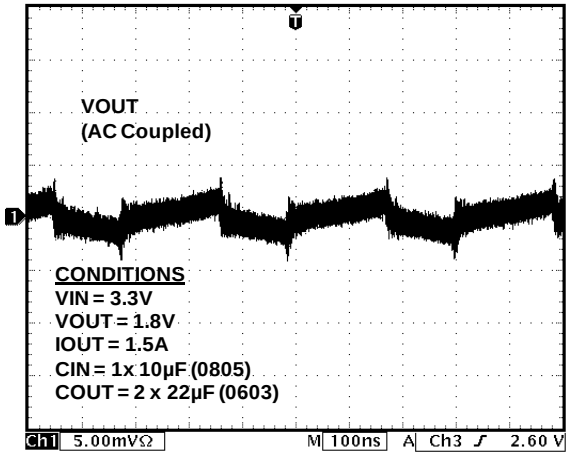
Output Ripple at 20MHz



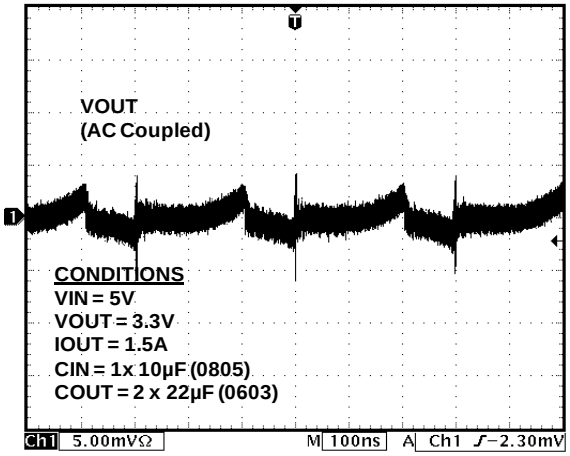
Output Ripple at 20MHz



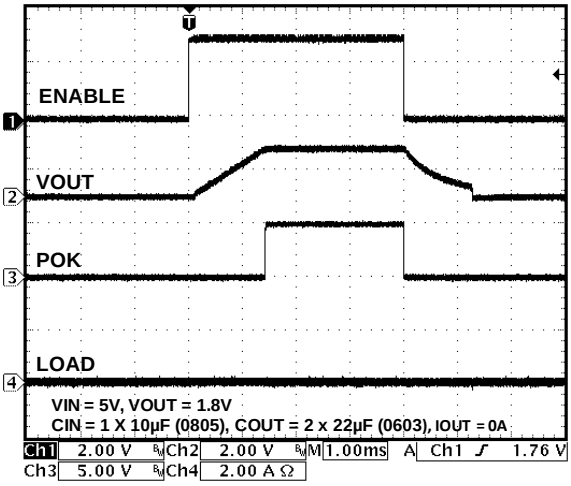
Output Ripple at 500MHz



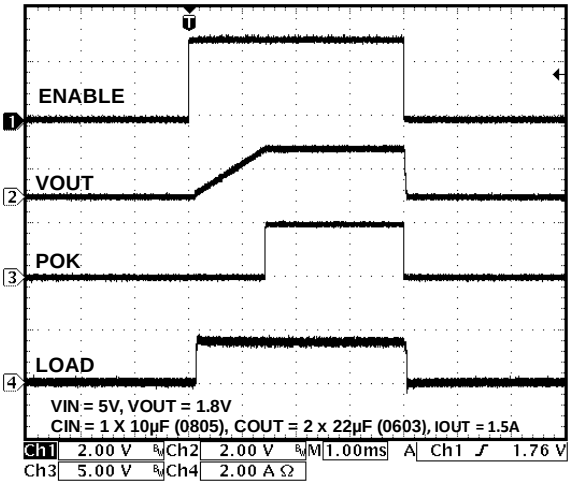
Output Ripple at 500MHz



Startup Waveforms at 0A

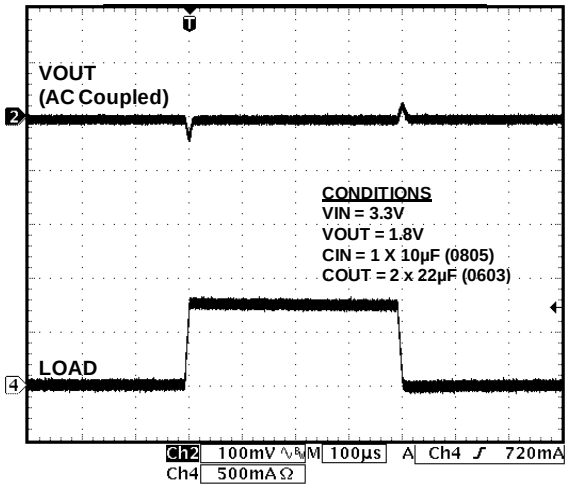


Startup Waveforms at 1.5A

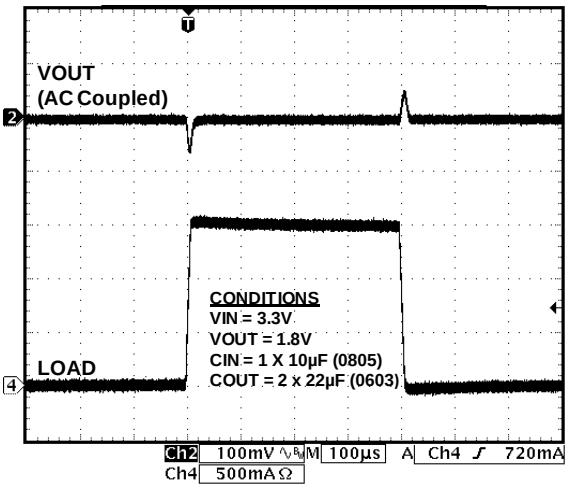


Typical Performance Characteristics (Continued)

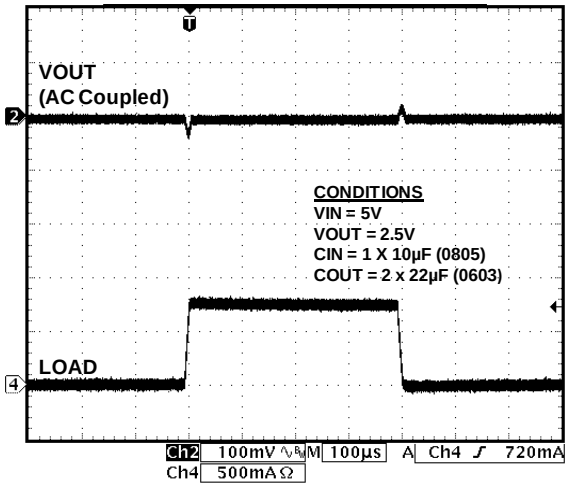
Load Transient from 0 to 750mA



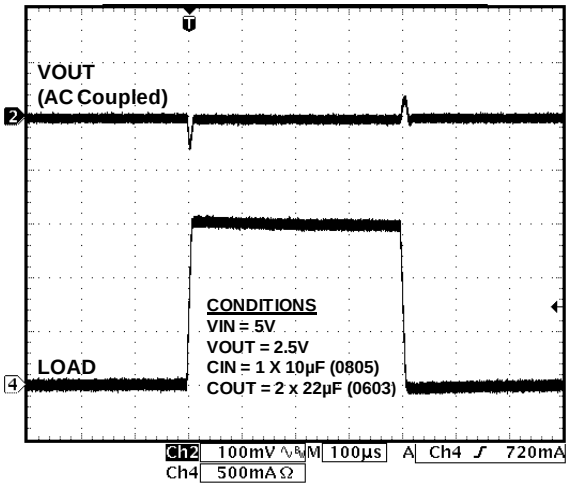
Load Transient from 0 to 1.5A



Load Transient from 0 to 750mA



Load Transient from 0 to 1.5A



Functional Block Diagram

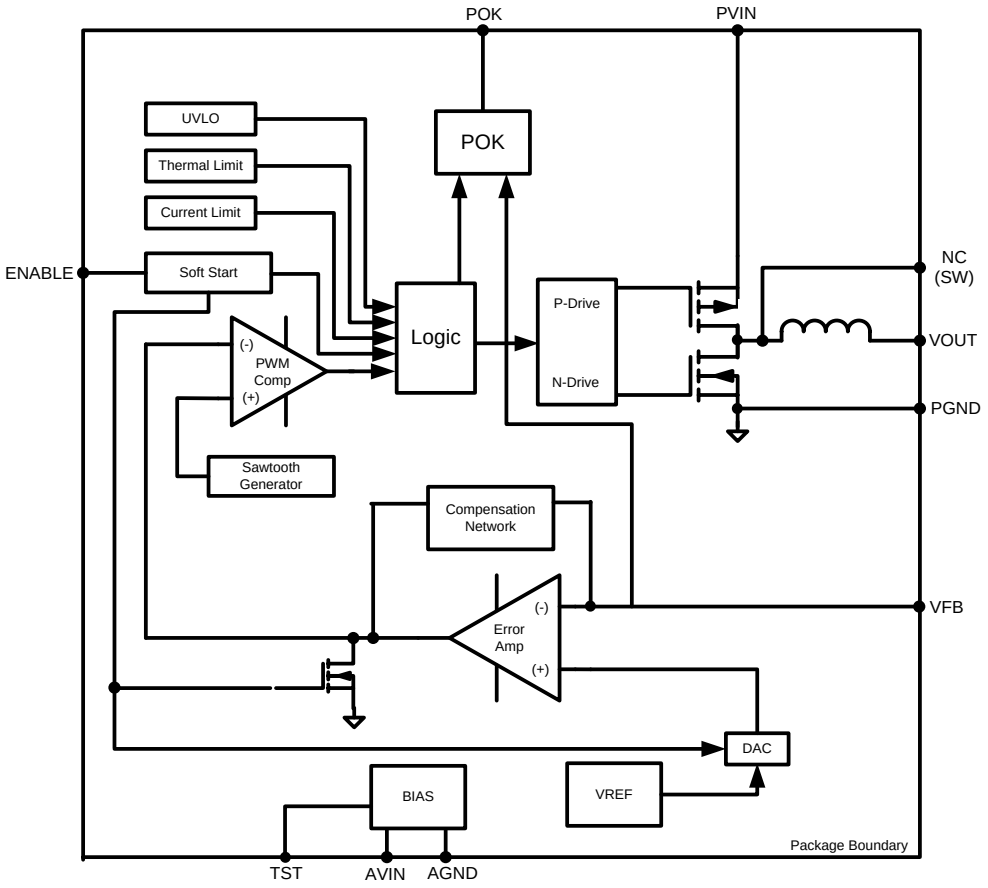


Figure 4: Functional Block Diagram

Functional Description

Overview

The EN5319QI is a highly integrated synchronous buck converter with an internal inductor utilizing advanced CMOS technology to provide high switching frequency, while also maintaining high efficiency. The EN5319QI is a high power density device packaged in a tiny 4x6x1.1mm 24-pin QFN package. Its high switching frequency allows for the use of very small MLCC input and output filter capacitors and results in a total solution size as small as 50mm^2.

The EN5319QI is a member of a family of pin compatible devices. This offers scalability for applications where load currents may not be known apriori, and/or speeds time to market with a convenient common solution footprint.

The EN5319QI buck converter uses Type III voltage mode control to provide pin-point output voltage accuracy, high noise immunity, low output impedance and excellent load transient response. The EN5319QI features include Power OK, under voltage lockout (UVLO), over current protection, short circuit protection, and thermal overload protection.

Stability and Compensation

The EN5319QI utilizes an internal compensation network that is designed to provide stable operation over a wide range of operating conditions. The output compensation circuit may be customized to improve transient performance or reduce output voltage ripple with dynamic loads.

Soft-Start

The EN5319QI has an internal soft-start circuit that controls the ramp of the output voltage. The control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETs and the integrated inductor.

The EN5319QI has a constant startup up time which is independent of the VOUT setting. The output rising slew rate is proportional to the output voltage. The startup time is approximately 1.4ms from when the ENABLE is first pulled high until VOUT reaches the regulated voltage level.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Since the slew rate varies with the output voltage setting, the maximum capacitance is a function of the VOUT setting.

The maximum capacitance on the output power rail, including the output filter capacitors and all decoupling and bulk capacitors on the supply rail is given by:

$C_{OUT\_TOTAL\_MAX}$ [µF] = $3.41x10^3 / V_{OUT}$

NOTE: The above number and formula assume a no load condition at startup.

Over Current/Short Circuit Protection

When an over current condition occurs, V_{OUT} is pulled low and the device disables switching internally. This condition is maintained for a period of 1.2 ms and then a normal soft-start cycle is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

An under voltage lockout circuit will hold off switching during initial power up until the input voltage reaches sufficient level to ensure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable switching. Hysteresis is included to prevent chattering between UVLO high and low states.

Enable

The ENABLE pin provides means to shut down the converter or initiate normal operation. A logic high on the ENABLE pin will initiate the converter to start the soft-start cycle and regulate the output voltage to the desired value. A logic low will allow the device to discharge the output and go into shutdown mode for minimal power consumption. When the output is discharged, an auxiliary NFET turns on and limits the discharge current to 300 mA or below. The ENABLE pin should not be left floating.

Thermal Shutdown

When excessive power is dissipated in the device, its junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature of 150°C, the thermal shutdown circuit turns off the converter, allowing the device to cool. When the junction temperature drops 15°C, the device will be re-enabled and go through a normal startup process.

Power OK

The Power OK (POK) feature is an open drain output signal used to indicate if the output voltage is within 92% of the set value. Within this range, the POK output is allowed to be pulled high. Outside this range, the POK output is maintained low. During transitions such as power up and power down, the POK output will not change state until the transition is complete for enhanced noise immunity.

The POK has 1mA sink capability. When POK is pulled high, the worst case pin leakage current is as low as 500nA over temperature. This allows a large pull up resistor such as 100kΩ to be used for minimal current consumption in shutdown mode.

The POK output can also be conveniently used as an enable input of the next stage for power sequencing of multiple converters.

Application Information

Setting the Output Voltage

The EN5319 uses a simple and flexible resistor divider network to program the output voltage. A feed-forward capacitor (Ca) is used to improve transient response. Table 3 shows the required critical component values for the feedback network as a function of VOUT. It is recommended to use 1% or better feedback resistors to ensure output voltage accuracy. The Ra resistor value is fixed at 348k as shown in Table 3. Based on that value, the bottom resistor Rb can be calculated below as:

$$Rb = \frac{Ra \times 0.6\,V}{V_{OUT} - 0.6\,V}$$

The V_{OUT} is the nominal output voltage. The Rb and Ra resistors have the same units based on the above equation.

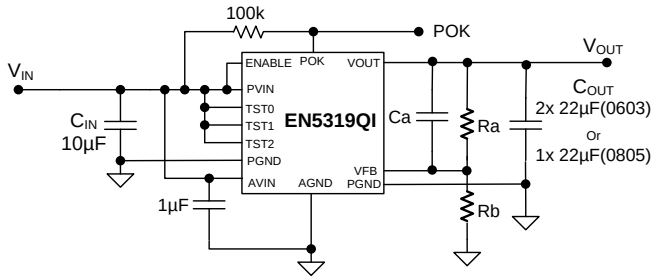


Figure 5. Typical Application Circuit.

(*NOTE:* Enable can be separated from PVIN if the application requires it)

AVIN Filter Capacitor

A 1.0 µF, 10V, 0402 MLCC capacitor should be placed between AVIN and AGND as close to the pins as possible. This will provide high frequency bypass to ensure clean chip supply for optimal performance.

Input Filter Capacitor Selection

A single 10µF, 0805 MLCC capacitor is needed on PVIN for all applications. Connect the input capacitor between PVIN and PGND as close to the pins as possible. Placement of the input capacitor is critical to ensure low noise and EMI Low ESR MLCC capacitors with X5R or X7R or equivalent dielectric should be used for the input capacitors. Y5V or equivalent dielectrics lose too much capacitance with frequency, DC bias, and temperature. Therefore, they are not suitable for switch-mode DC-DC converter filtering, and must be avoided.

Table 1: Recommended Input Capacitors

Description	MFG	P/N
10µF, 10V, X5R, 0805	Taiyo Yuden	LMK212ABJ106KG
	Murata	GRM21BR61A106KE19

Output Filter Capacitor Selection

The EN5319QI output capacitor selection may be determined based on two configurations. Table 3 provides the allowed output capacitor configurations based on operating conditions. For lower output ripple, choose 2 x 22µF 0603 for the output capacitors. For smaller solution size, use one 22µF 0805 output capacitor. Table 2 shows the recommended type and brand of output capacitors to use. For details regarding other configurations, contact Power Applications support (www.altera.com/mysupport).

In some rare applications modifications to the compensation may be required. The EN5329QI provides the capability to modify the control loop response to allow for customization for specific applications. For more information, contact Power Applications support.

Table 2: Recommended Output Capacitors

Description	MFG	P/N
22µF, 6.3V, X5R, 0805	Taiyo Yuden	JMK212ABJ226MG
	Murata	GRM21BR60J226ME39
22µF, 6.3V, X5R, 0603	Murata	GRM188R60J226MEA0

Table 3. Required Critical Components
(Note: Follow Layout Recommendations)

VOUT (V)	Ca (pF)	Ra (kΩ)	Cout (µF)
Vout ≤ 2.0V	10	348	1x22uF/0805
2.0V < Vout ≤ 3.3V	8.2		
Vout ≤ 2.0V	12	348	2x22uF/0603
2.0V < Vout ≤ 3.3V	6.8		
Vout ≤ 2.0V	12	348	2x22uF/0805
2.0V < Vout ≤ 3.3V	6.8		
Vout > 3.3V	6.8		

Power-Up/Power-Down

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, and ENABLE) together during power up or power down meets these requirements.

The EN5319QI supports startup into a pre-biased output of up to 1.5V. The output of the EN5319QI can be pre-biased with a voltage up to 1.5V when it is first enabled.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated needs to be accounted for. Altera's Enpirion PowerSoC™ helps alleviate some of those concerns.

Altera's Enpirion EN5319QI DC-DC converter is packaged in a 4x6x1.1mm 24-pin QFN package. The QFN package is constructed with exposed thermal pads on the bottom of the package. The exposed thermal pad should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The EN5319QI is guaranteed to support the full 2A output current up to 85°C ambient temperature. The following example and calculations illustrate the thermal performance of the EN5319QI.

Example:

V_{IN} = 5V

V_{OUT} = 3.3V

I_{OUT} = 1.5A

First calculate the output power.

P_{OUT} = 3.3V x 1.5A = 4.95W

Next, determine the input power based on the efficiency (η) shown in Figure 6.

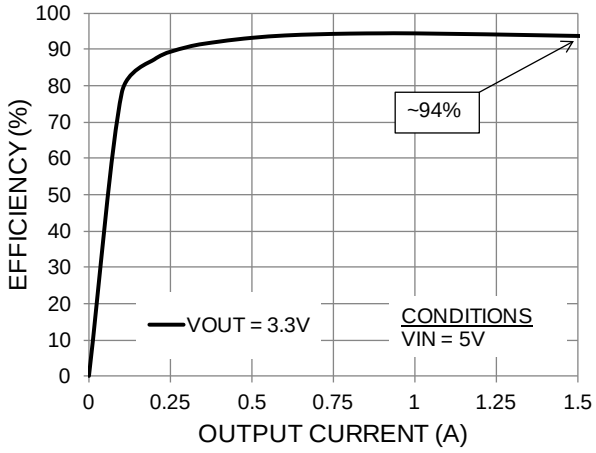


Figure 6: Efficiency vs. Output Current

For V_{IN} = 5V, V_{OUT} = 3.3V at 1.5A, η ≈ 94%

$\eta = P_{OUT} / P_{IN} = 94\% = 0.94$

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 4.95W / 0.94 \approx 5.3W$

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_D = P_{IN} - P_{OUT}$

$\approx 5.3W - 4.95W \approx 0.35W$

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN5319QI has a θ_{JA} value of 36 ºC/W without airflow.

Determine the change in die temperature (ΔT) based on P_D and θ_{JA}.

$\Delta T = P_D \times \theta_{JA}$

$\Delta T \approx 0.35W \times 36°C/W = 12.6°C \approx 13°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 13°C \approx 38°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} - P_D \times \theta_{JA}$

$\approx 125°C - 13°C \approx 112°C$

The ambient temperature can actually rise by another 87°C, bringing it to 112°C before the device will reach T_{JMAX}. This indicates that the EN5319QI can support the full 1.5A output current range up to approximately 112°C ambient temperature given the input and output voltage conditions. Note that the efficiency will be slightly lower at higher temperatures and these calculations are estimates.

Engineering Schematic

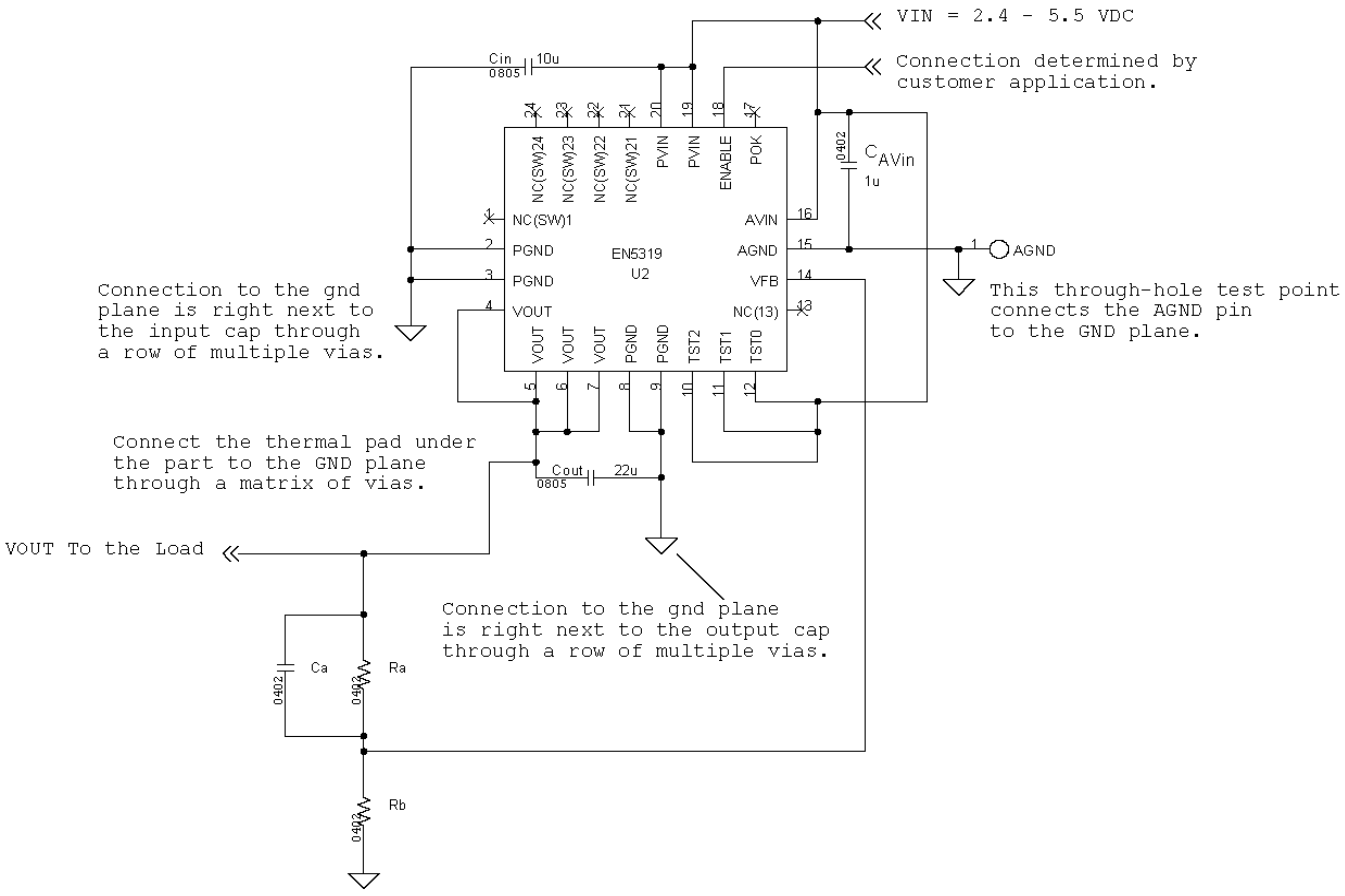


Figure 7. Engineering Schematic with Critical Components

Layout Recommendations

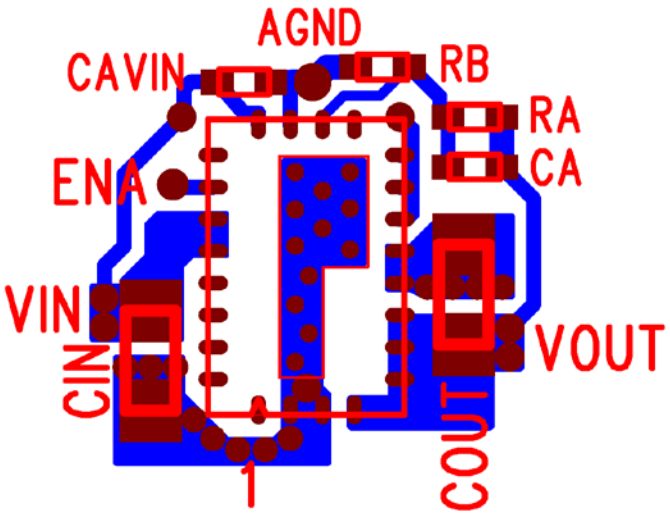


Figure 8. Optimized Layout Recommendations

This layout only shows the critical components and top layer traces for minimum footprint with ENABLE as a separate signal. Alternate ENABLE configurations & the POK pin need to be connected and routed according to customer application. Please see the Gerber files at www.altera.com/enpirion for details on all layer.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5319QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5319QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 3: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 3) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 8 this connection is made at the input capacitor. Connect a 1µF capacitor from the AVIN pin to AGND.

Recommendation 6: The layer 1 metal under the device must not be more than shown in Figure 8. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 7: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 8: Keep R_A, C_A, R_B close to the VFB pin (See Figures 6). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Recommendation 9: Altera provides schematic and layout reviews for all customer designs. Please contact local sales representatives for references to Power Applications support (www.altera.com/mysupport).

Design Considerations for Lead-Frame Based Modules

Exposed Metal Pads on Package Bottom

QFN lead-frame based package technology utilizes exposed metal pads on the bottom of the package that provide improved thermal dissipation, lower package thermal resistance, smaller package footprint and thickness, larger lead size and pitch, and excellent lead co-planarity. As the EN5319 package is a fully integrated module consisting of multiple internal devices, the lead-frame provides circuit interconnection and mechanical support of these devices resulting in multiple exposed metal pads on the package bottom.

Only the two large thermal pads and the perimeter leads are to be mechanically/electrically connected to the PCB through a SMT soldering process. All other exposed metal is to remain free of any interconnection to the PCB. Figure 9 shows the recommended PCB metal layout for the EN5319 package. A GND pad with a solder mask "bridge" to separate into two pads and 24 signal pads are to be used to match the metal on the package. The PCB should be clear of any other metal, including traces, vias, etc., under the package to avoid electrical shorting.

The Solder Stencil Aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult EN5319QI Soldering Guidelines for more details and recommendations.

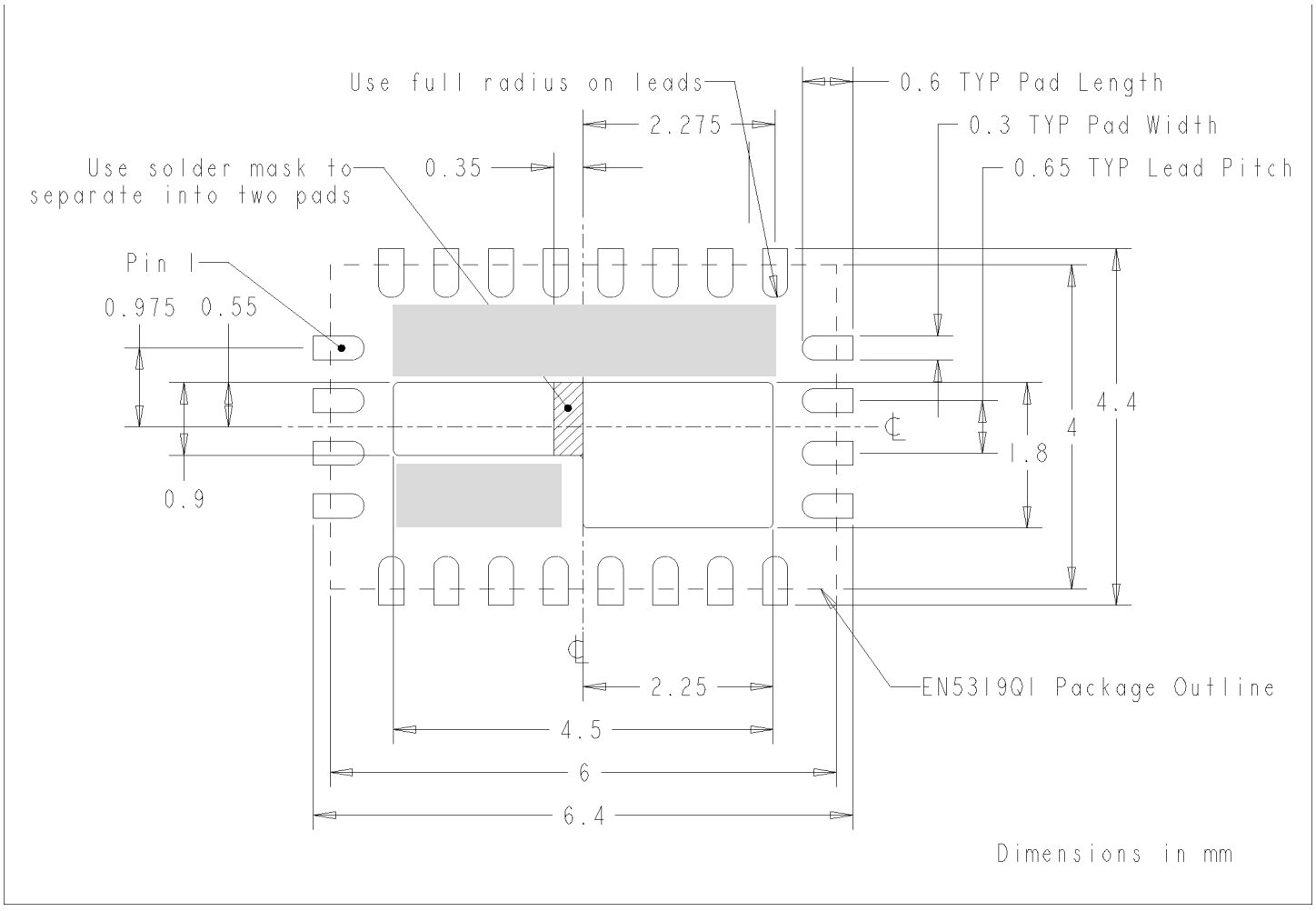


Figure 9. Recommended Footprint for PCB (Top View)

Note: Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Recommended PCB Footprint

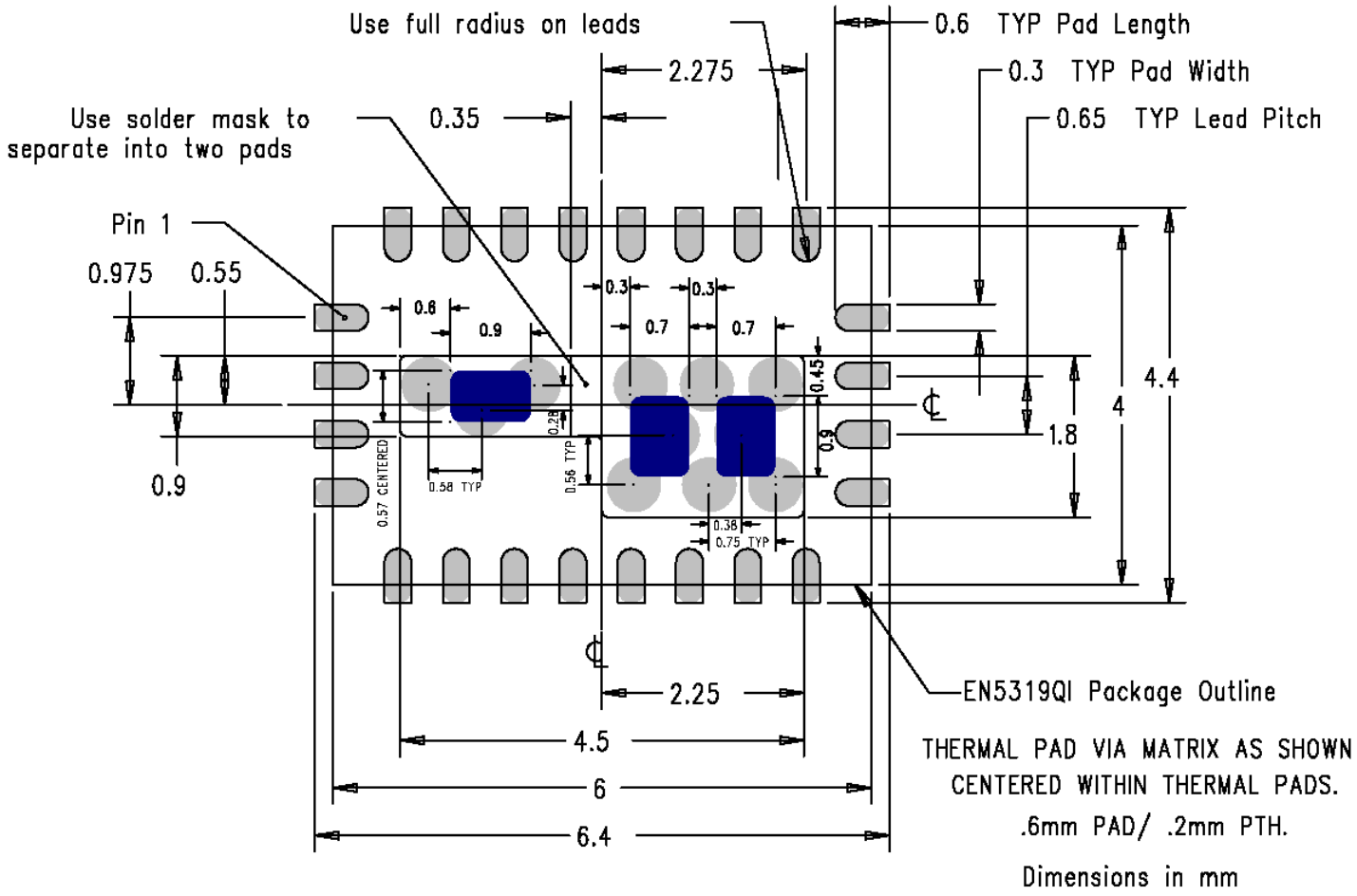


Figure 10. EN5319 PCB Footprint (Top View)

The solder stencil aperture for the thermal pads (shown in blue) is based on Altera's manufacturing recommendations.

Package Mechanical

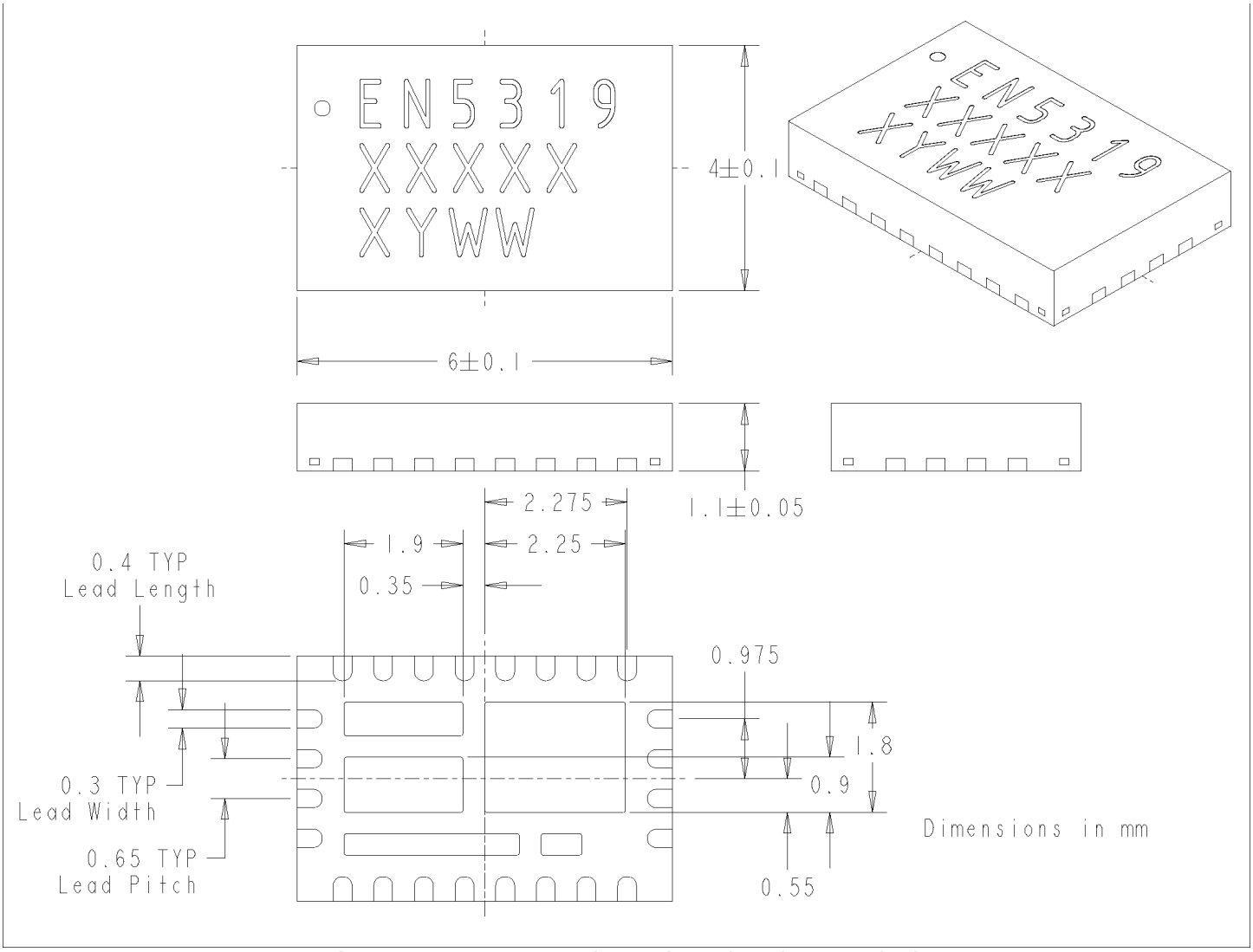


Figure 11. EN5319QI Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

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