



Enpirion[®] Power Datasheet

EN5335QI 3A PowerSoC

Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor

3-Pin Programmable Output

Description

The EN5335QI is a Power System on a Chip (PowerSoC). It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in a distributed power architecture. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. Operating this converter requires as few as three external components that include small value input and output ceramic capacitors and a soft-start capacitor.

The Altera Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Typical Application Circuit

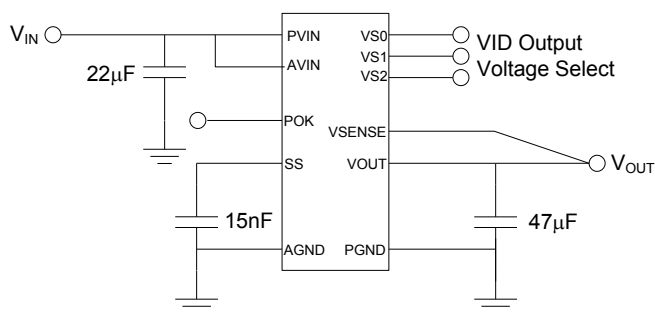


Figure 1. Simple Layout.

Features

- Integrated INDUCTOR, MOSFETS, Controller
- Footprint 1/3rd that of competing solutions
- Low Part Count: only 3 MLC Capacitors
- Up to 10W continuous output power
- 5MHz operating frequency
- High efficiency, up to 93%
- V_{OUT} accuracy 3% over line, load and temp
- Wide input voltage range of 2.375V to 6.6V
- 3-pin VID output voltage select to choose one of 7 pre-programmed voltage levels
- Output enable pin and Power OK signal
- Programmable soft-start time
- Programmable over-current protection
- Thermal shutdown, short circuit, and UVLO
- Output over-voltage protection
- RoHS compliant, MSL level 3, 260C reflow

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Notebook computers, servers, workstations
- Broadband, networking, LAN/WAN, optical
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- DSL, STB, DVR, DTV, iPC
- Ripple sensitive applications

Ordering Information

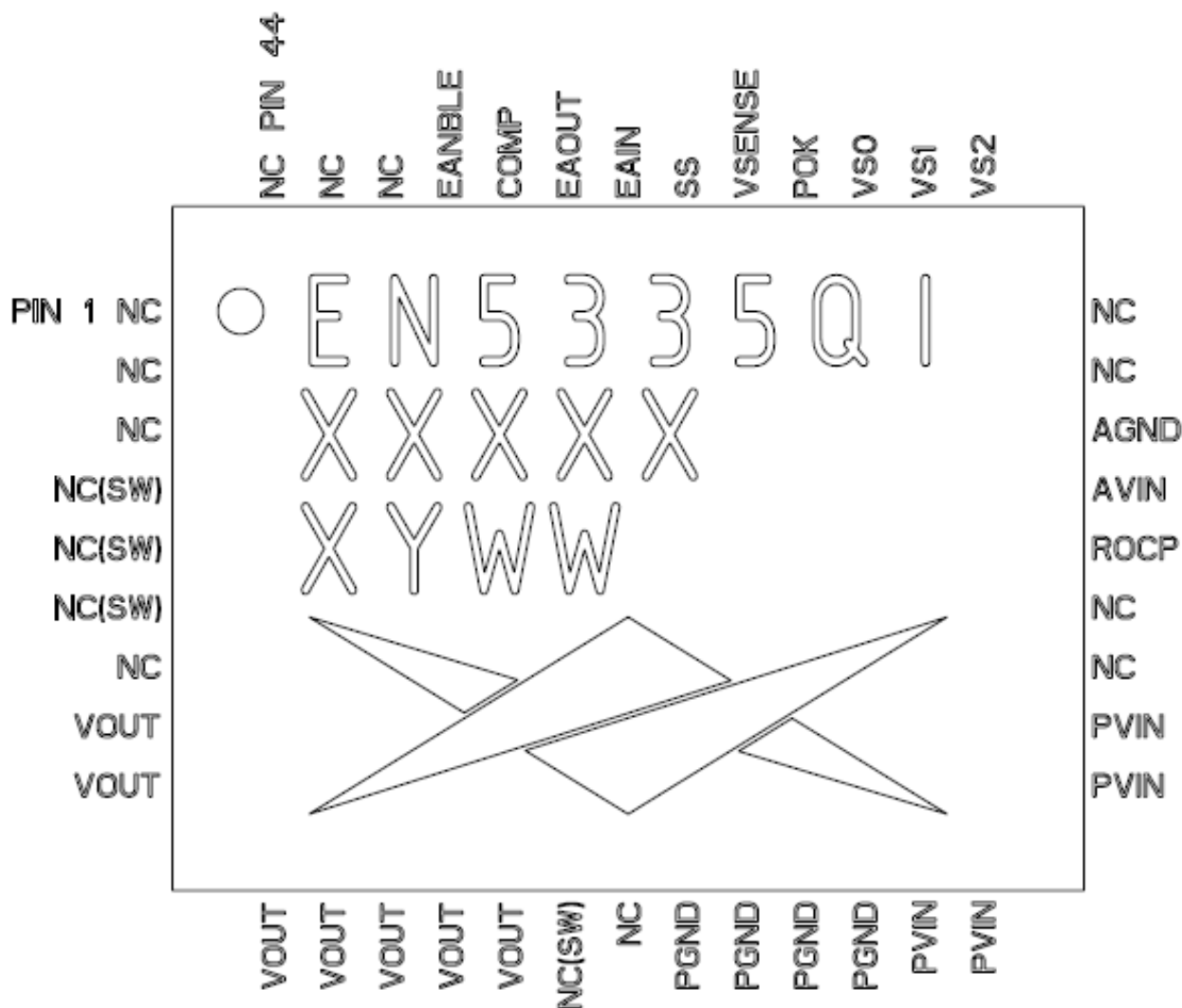
| Part Number | Temp Rating (°C) | Package |
|--------------|------------------|----------------------|
| EN5335QI | -40 to +85 | 44-pin QFN T&R |
| EVB-EN5335QI | | QFN Evaluation Board |

Pin Configuration

Below is a top view diagram of the EN5335QI package.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

Figure 2. Pin-out diagram, top view.



Pin Descriptions

| PIN | NAME | FUNCTION |
|-------|--------|--|
| 1-3 | NC | NO CONNECT – Do not electrically connect these pins to each other or to PCB. |
| 4-6 | NC(SW) | No Connect. These pins are internally connected to the switch node of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. |
| 7 | NC | No connect – Do not electrically connect these pins to each other or to PCB. |
| 8-14 | VOUT | Regulated converter output. Connect these pins to the load and place output capacitor from these pins the PGND pins 17-18 |
| 15 | NC(SW) | No Connect. These pins are internally connected to the switch node of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. |
| 16 | NC | No connect – Do not electrically connect these pins to each other or to PCB. |
| 17-20 | PGND | Output power ground. Connect these pins to the ground electrode of the output filter capacitors. Refer to layout guideline section. |
| 21-24 | PVIN | Input power supply. Connect to input power supply. Decouple with input capacitor to PGND (pins 19-20). |
| 25-26 | NC | No connect – Do not electrically connect these pins to each other or to PCB. |
| 27 | ROCP | Optional Over Current Protection adjust pin. Place ROCP resistor between this pin and AGND (pin 40) to increase the over current trip point by 50%. |
| 28 | AVIN | Analog voltage input for the controller circuits. Connect this pin to the input power supply. |
| 29 | AGND | Analog ground for the controller circuits. |
| 30-31 | NC | No connect – Do not electrically connect these pins to each other or to PCB. |
| 32 | VS2 | Voltage select line 2 input. See Table 1. |
| 33 | VS1 | Voltage select line 1 input. See Table 1. |
| 34 | VS0 | Voltage select line 0 input. See Table 1. |
| 35 | POK | Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal. |
| 36 | VSENSE | Remote voltage sense input. Connect this pin to the load voltage at the point to be regulated. |
| 37 | SS | Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this resistor determines the startup timing. |
| 38 | EAIN | Optional Error Amplifier input. Allows for customization of the control loop. |
| 39 | EAOUT | Optional Error Amplifier output. Allows for customization of the control loop. |
| 40 | COMP | Optional Error Amplifier Buffer output. Allows for customization of the control loop. |
| 41 | ENABLE | Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output. |
| 42-44 | NC | No connect – Do not electrically connect these pins to each other or to PCB. |

Block Diagram

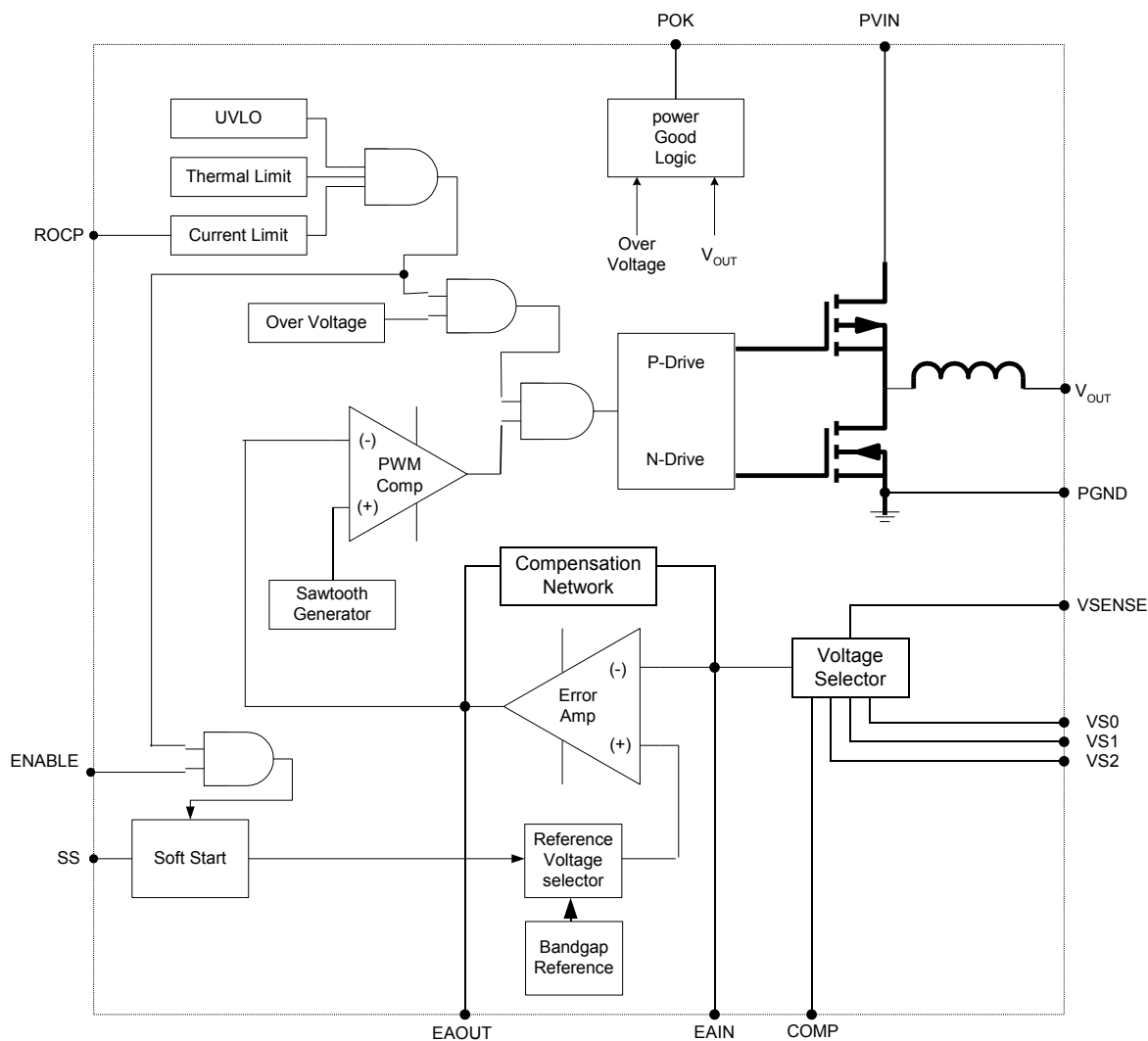


Figure 3. System block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond Absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

| Maximum Electrical Ratings | Min | Max |
|--|-------|-----------------|
| Voltages on: V_{IN} , V_{OUT} | -0.3V | 7.0V |
| Voltages on: V_{SENSE} | -0.3V | $V_{IN} + 0.3V$ |
| Voltages on: V_{S0} - V_{S2} (Note 1) | -0.3V | $V_{IN} + 0.3V$ |
| Voltages on: ENABLE | -0.3V | $V_{IN} + 0.3V$ |
| Maximum Thermal Ratings | | |
| Ambient operating range | -40°C | +85°C |
| Storage Temperature Range | -65°C | +150°C |
| Reflow Peak Body Temperature MSL3 (10 Sec) | | +260°C |

Note 1: V_{S0} - V_{S2} pins have an internal pull-up resistor, only ground potentials should be placed on them as required.

Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|----------|-------|------|--------------------|
| Input Voltage Range (for output voltages < 1.2V) | V_{IN} | 2.375 | 5.5 | V |
| Input Voltage Range (for output voltages \geq 1.2V) | V_{IN} | 2.375 | 6.6 | V |
| EN5335QI Operating Ambient Temperature | T_A | -40 | +85 | $^{\circ}\text{C}$ |
| Operating Junction Temperature | T_J | -40 | +125 | $^{\circ}\text{C}$ |

Thermal Characteristics

| PARAMETER | SYMBOL | TYP | UNITS |
|---|---------------|-----|-----------------------------|
| Thermal Shutdown | T_{SD} | 150 | $^{\circ}\text{C}$ |
| Thermal Shutdown Hysteresis | T_{SDH} | 15 | $^{\circ}\text{C}$ |
| Thermal Resistance: Junction to Case (0 LFM) (Note 2) | θ_{JC} | 3 | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance: Junction to Ambient (0 LFM) | θ_{JA} | 25 | $^{\circ}\text{C}/\text{W}$ |

Note 2: Based on a four-layer board and proper thermal design in line with JEDEC EIJ/JESD 51 Standards.

Electrical Characteristics

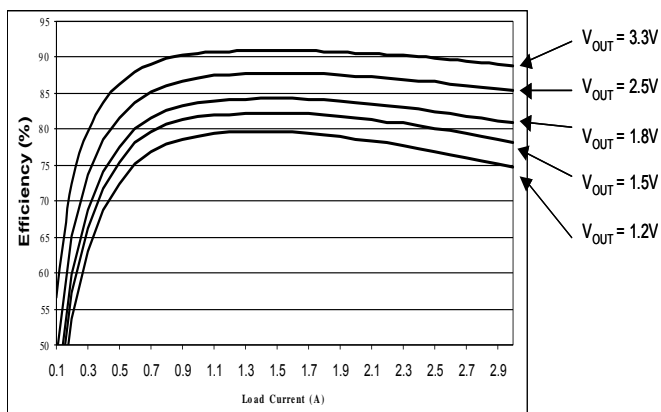
NOTE: $V_{IN}=5.5\text{V}$ over operating temperature range unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------------|--|--------------|------|------------|---------------|
| Operating Input Voltage (for output voltages < 1.2V) | V_{IN} | | 2.375 | | 5.5 | V |
| Operating Input Voltage (for output voltages \geq 1.2V) | V_{IN} | | 2.375 | | 6.6 | V |
| V_{OUT} Initial Accuracy | ΔV_{OUT_INIT} | $T_A = 25\text{C}$, $V_{IN} = 5.0\text{V}$, $I_{LOAD} = 0\text{A}$; <ul style="list-style-type: none"> • All VID Settings except 0.8V • 0.8V | -2 -3 | | +2 +2 | % |
| VID Output Voltage Settings | V_{OUT} | <u>VS2 VS1 VS0</u> | | | | |
| | | 0 0 0 | | 3.3 | | V |
| | | 0 0 1 | | 2.5 | | |
| | | 0 1 0 | | 1.8 | | |
| | | 0 1 1 | | 1.5 | | |
| | | 1 0 0 | | 1.25 | | |
| | | 1 0 1 | | 1.2 | | |
| | | 1 1 0 | | 0.8 | | |
| 1 1 1 | | reserved | | | | |
| Drop out voltage | $V_{IN} - V_{OUT}$ | Drop out voltage at full load | | | 600 | mV |
| Shut-Down Supply Current | I_S | ENABLE=0V | | 100 | | μA |
| Switching Frequency | F_{OSC} | | | 5 | | MHz |
| V_{OUT} | | | | | | |
| Output Voltage Regulation | V_{OUT} | Over line, load and temperature VID Output Voltage Setting (V): 1.2, 1.25, 1.5, 1.8, 2.5, 3.3 0.8V | -3.0 -4.0 | | 3.0 4.0 | % |
| Maximum Continuous Output Current | | | | | | |
| Over Current Trip Piont | I_{OCP} | | | 4.5 | | A |

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|----------------------|---|------------|--------------|-----------------|---------------|
| Enable Operation | | | | | | |
| Disable Threshold | V_{DISABLE} | Max voltage to ensure the converter is disabled | | | 0.8 | V |
| Enable Threshold | V_{ENABLE} | $2.375\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$ $5.5\text{V} < V_{\text{IN}}$ | 1.8 2.0 | | | V |
| Enable Pin Current | I_{ENABLE} | $V_{\text{IN}} = 5.5\text{V}$ | | 50 | | μA |
| Voltage Select Operation | | | | | | |
| VS_x Logic Low Threshold | $V_{\text{SX-Low}}$ | Threshold voltage for Logic Low | | | 0.8 | V |
| VS_x Logic High Threshold | $V_{\text{SX-High}}$ | Threshold voltage for Logic High (internally pulled high; can be left floating to achieve logic high) | 1.8 | | V_{IN} | V |
| VS_x Pin Current | I_{VSX} | $(V_{\text{IN}} = 5.5\text{V})$ $\text{VS}_x = \text{GND}$ $\text{VS}_x = V_{\text{IN}}$ $\text{VS}_x = \text{Open}$ | | 50 0 0 | | μA |
| Power OK Operation | | | | | | |
| POK low voltage | V_{POK} | $I_{\text{POK}} = 4\text{mA}$ (sink current) | | | 0.4 | V |
| Max POK Voltage | V_{POK} | | | | V_{IN} | V |

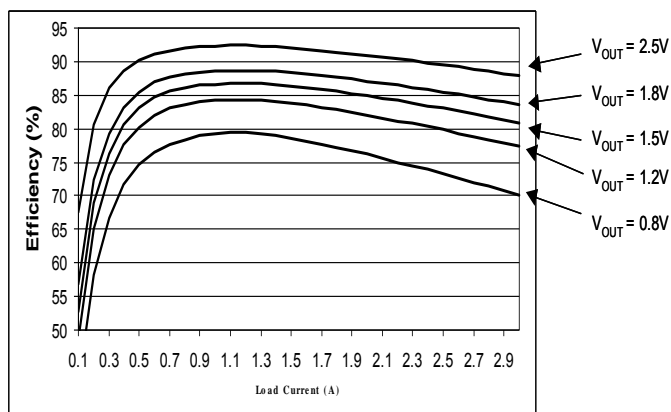
Typical Performance Characteristics

$V_{\text{IN}} = 5.0\text{V}$

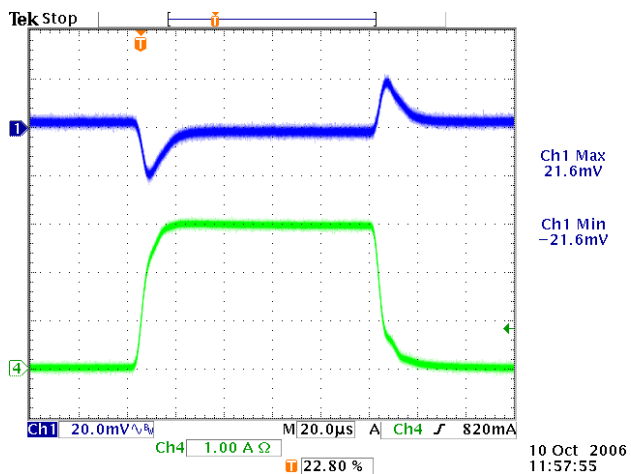


Efficiency versus Load, $V_{\text{IN}} = 5.0\text{V}$

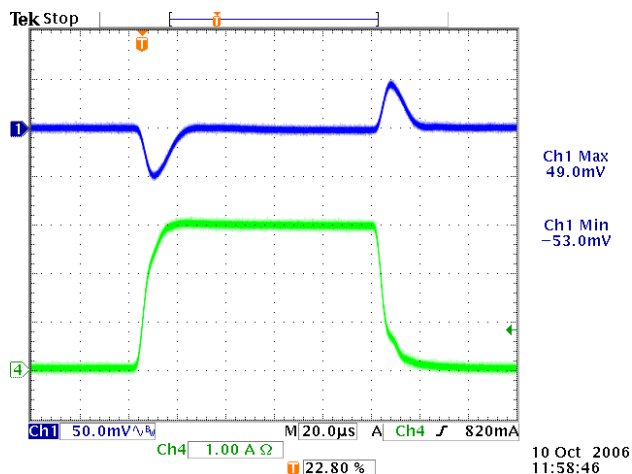
$V_{\text{IN}} = 3.3\text{V}$



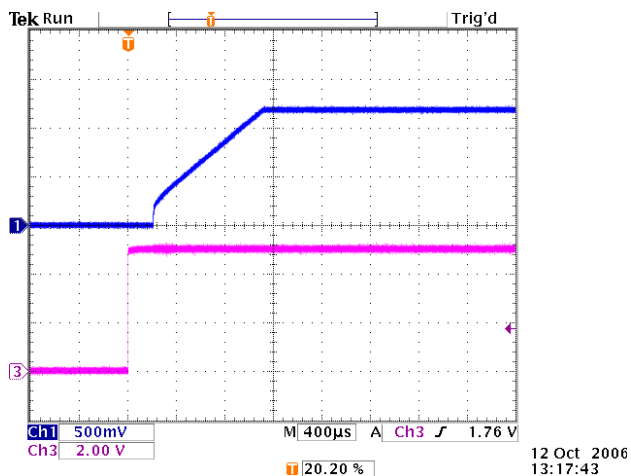
Efficiency versus Load, $V_{\text{IN}} = 3.3\text{V}$



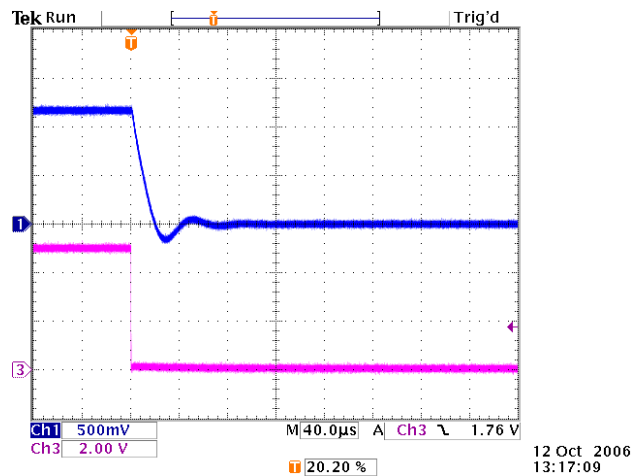
Load transient, 0 – 3A, $V_{IN}/V_{OUT} = 5.5V/1.2V$



Load transient, 0 – 3A, $V_{IN}/V_{OUT} = 5.5V/3.3V$



Start-up waveform, $V_{IN}/V_{OUT} = 5.5V/1.2V$



Shut-down waveform, $V_{IN}/V_{OUT} = 5.5V/1.2V$

Theory of Operation

Synchronous Buck Converter

The EN5335QI is a synchronous, pin programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.4-5.0V. The output can be set to common pre-set voltages by connecting appropriate combinations of 3 voltage selection pins to ground. The feedback control loop is a type III voltage-mode and the part uses a low-noise PWM topology. Up to 3A of output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size output capacitors.

The power supply has the following protection features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis
- Over-voltage protection
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, limiting the in-rush current when the converter is powered up
- Power good circuit indicating whether the output voltage is within 90% - 120% of the programmed voltage

Output Voltage Programming

The EN5335QI output voltage is programmed using a 3-pin voltage-ID or VID selector. Three binary VID pins allow the user to choose one of seven pre-set voltages. Refer to Table 1 for the proper VID pin settings to choose VOUT.

The voltage select pins, VS0, VS1, and VS2, are pulled-up internally and so will default to a logic high, or "1", if left "open". Connecting the voltage select pin to ground will result in a logic "0".

Table 1: Output Voltage Select Table:

| VS2* | VS1* | VS0* | Output Voltage |
|------|------|------|----------------|
| 0 | 0 | 0 | 3.3V |
| 0 | 0 | 1 | 2.5V |
| 0 | 1 | 0 | 1.8V |
| 0 | 1 | 1 | 1.5V |
| 1 | 0 | 0 | 1.25V |
| 1 | 0 | 1 | 1.2V |
| 1 | 1 | 0 | 0.8V |
| 1 | 1 | 1 | Reserved |

Input Capacitor Selection

The EN5335QI requires about 20uF of input capacitance. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. It is recommended to use 10V rated MLCC capacitors.

Table 2. Recommended input capacitors.

| Description | MFG | P/N |
|--|-----------------------|---------------------------------------|
| 10uF, 10V, 10% X7R, 1206 (2 capacitors needed) | Murata Taiyo Yuden | GRM31CR71A106KA01L LMK316B7106KL-T |
| 22uF, 10V, 10% X7R, 1210 (1 capacitor needed) | Murata Taiyo Yuden | GRM32ER71A226KE20L LMK325B7226KM-T |

Output Capacitor Selection

The EN5335QI has been optimized for use with approximately 50uF of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

$$Z = \text{ESR} + \text{ESL}.$$

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \dots + \frac{1}{Z_n}$$

Typical ripple versus capacitance is given below:

| Output Capacitor Configuration | Typical Output Ripple (mVp-p) (as measured on EN5335QI Evaluation Board) |
|--------------------------------|---|
| 1 x 47 uF | 30 |
| 3 x 22 uF | 15 |

Table 3. Recommended output capacitors.

| Description | MFG | P/N |
|---|-------------|--------------------|
| 22uF, 6.3V, 10% X5R, 1206 (3 capacitors needed) | Murata | GRM31CR60J226KE19L |
| | Taiyo Yuden | JMK316BJ226KL-T |
| 47uF, 10V, 10% X5R, 1210 47uF, 6.3V, 10% X5R, 1210 (1 capacitor needed) | Murata | GRM32ER61A476KE20L |
| | AVX | 12106D476KAT2A |

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted, the device will undergo a normal soft start. A logic low will disable the converter and cause it to shut down. When Enable goes low, circuitry internal to the device continue to operate to ensure the output voltage is gradually returned to zero and the circuits turn off subsequently. A short low going pulse on Enable is ignored.

Soft-Start Operation

Soft start is a method to reduce in-rush current when the device is enabled. The output voltage is ramped up slowly upon start-up. The output rise time is controlled by choice of a soft-start capacitor, which is placed between the SS pin (pin 37) and the AGND pin (pin 29).

$$\text{Rise Time: } T_R = C_{SS} * 75K\Omega$$

During start-up of the converter, the reference voltage to the error amplifier is gradually

increased from zero to its final level by an internal current source of typically 10uA. Typical soft-start rise time is 1mS to 3mS. The rise time is measured from the time when AVIN > V_{UVLO} and the Enable signal crosses its logic high threshold. Typical SS capacitor values are in the range of 15nF to 50 nF.

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EN5335QI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EN5335QI is not pre-biased when the EN5335QI is first enabled.

POK Operation

The POK signal is an open drain signal from the converter indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state (see also: Over-Voltage Protection).

Over-Current Protection

The current limit function is achieved by sensing the current flowing through the sense P-MOSFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off. If the over-current condition is removed, the over-current protection circuit will enable the PWM operation. This circuit is designed to provide high noise immunity.

The nominal over current trip point is set to 4.5A. It is possible to increase the over-current set point by about 50% by connecting a 7.5k Ω resistor between ROCP (pin 27) and GND. The typical voltage at the ROCP pin is 0.75V.

In some cases, such as the start-up of FPGA devices, it is desirable to blank the over-current protection feature. In order to disable over-current protection, the ROCP pin should be tied to any voltage between 2.5V and PVIN.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 150°C. Once the junction temperature drops by approx 25°C, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Circuitry is provided to ensure that when the input voltage is below the specified voltage range, the converter will not start-up. Circuits for hysteresis, input de-glitch and output leading edge blanking are included to ensure high noise immunity and prevent false tripping.

Compensation

The EN5335QI is internally compensated through the use of a type 3 compensation network and is optimized for use with about 50 μ F of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on recommended capacitor types.) Voltage mode operation provides high noise immunity at light load.

In some cases modifications to the compensation may be required. For more information, contact Altera Power Applications support.

Layout Recommendation

Figure 4 shows critical components and layer 1 traces of a recommended minimum footprint EN5335QI layout. Alternate ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Altera website www.altera.com/enpirion for exact dimensions and other layers. Please refer to Figure 4 while reading the layout recommendations in this section.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5335QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5335QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Two PGND pins are dedicated to the input circuit, and two to the output circuit. The slit in Figure 4 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Altera website www.altera.com/enpirion.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible.

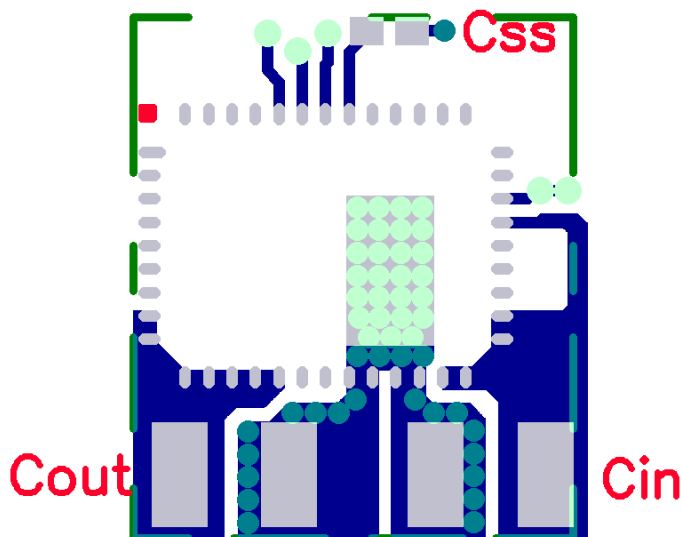


Figure 4: Top PCB Layer Critical Components and Copper for Minimum Footprint

The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figures: 7, 8, and 9.

Recommendation 5: Multiple small vias (the same size as the thermal via discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 4. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT} , then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 4 this connection is made at

the input capacitor close to the V_{IN} connection.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 4. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive

signal or control lines underneath the converter package on other layers.

Recommendation 8: The VSENSE point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5335QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 5 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB. Figure 6 shows the recommended PCB footprint for this device.

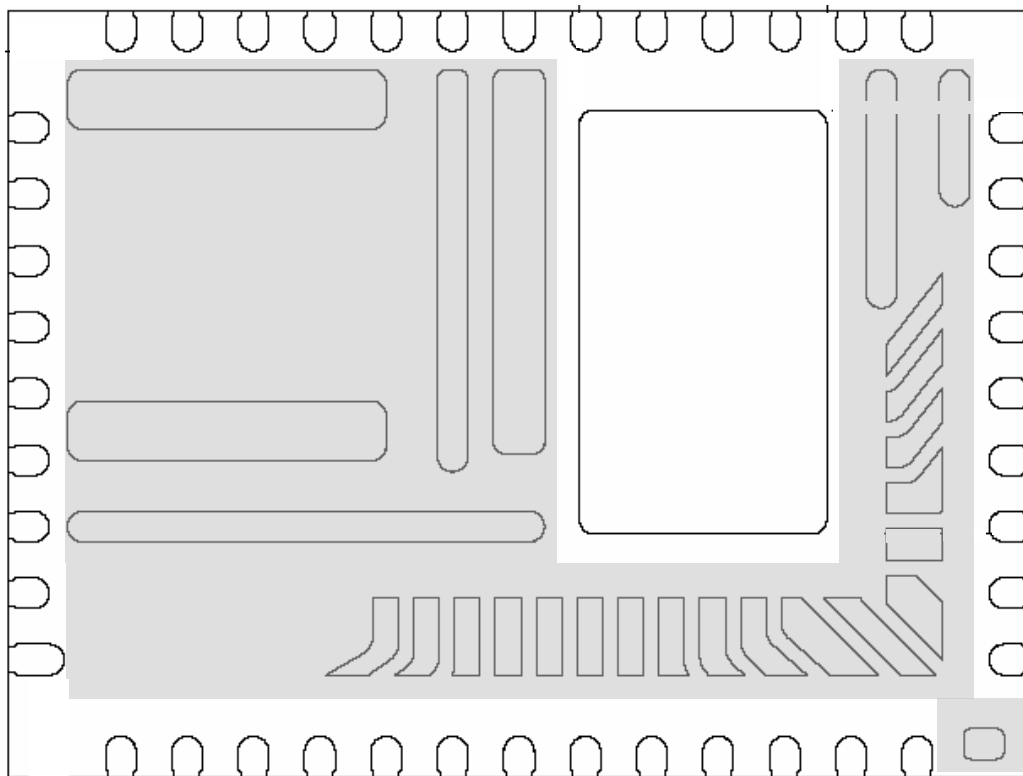


Figure 5. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

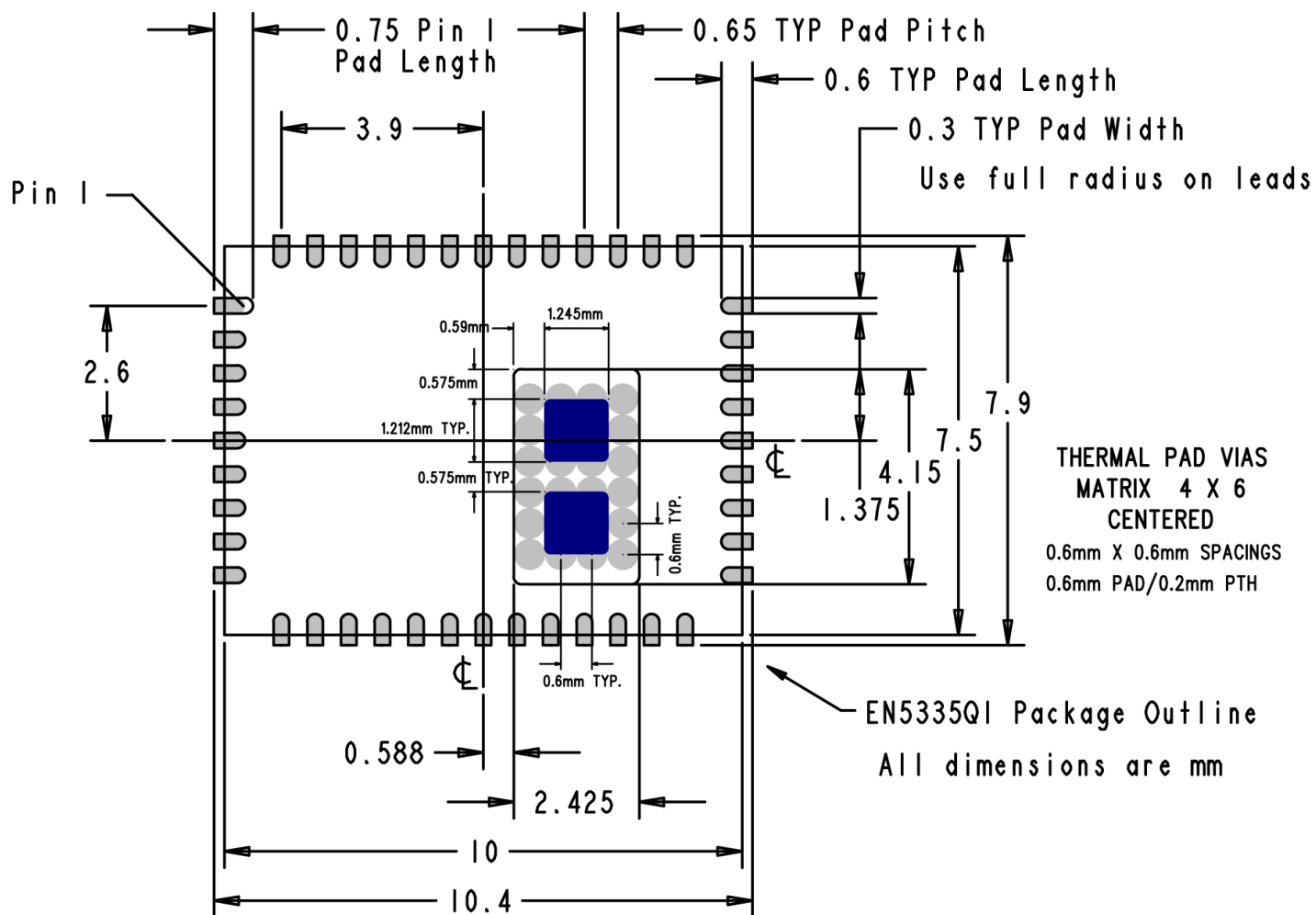


Figure 6: EN5335QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

Package Dimensions

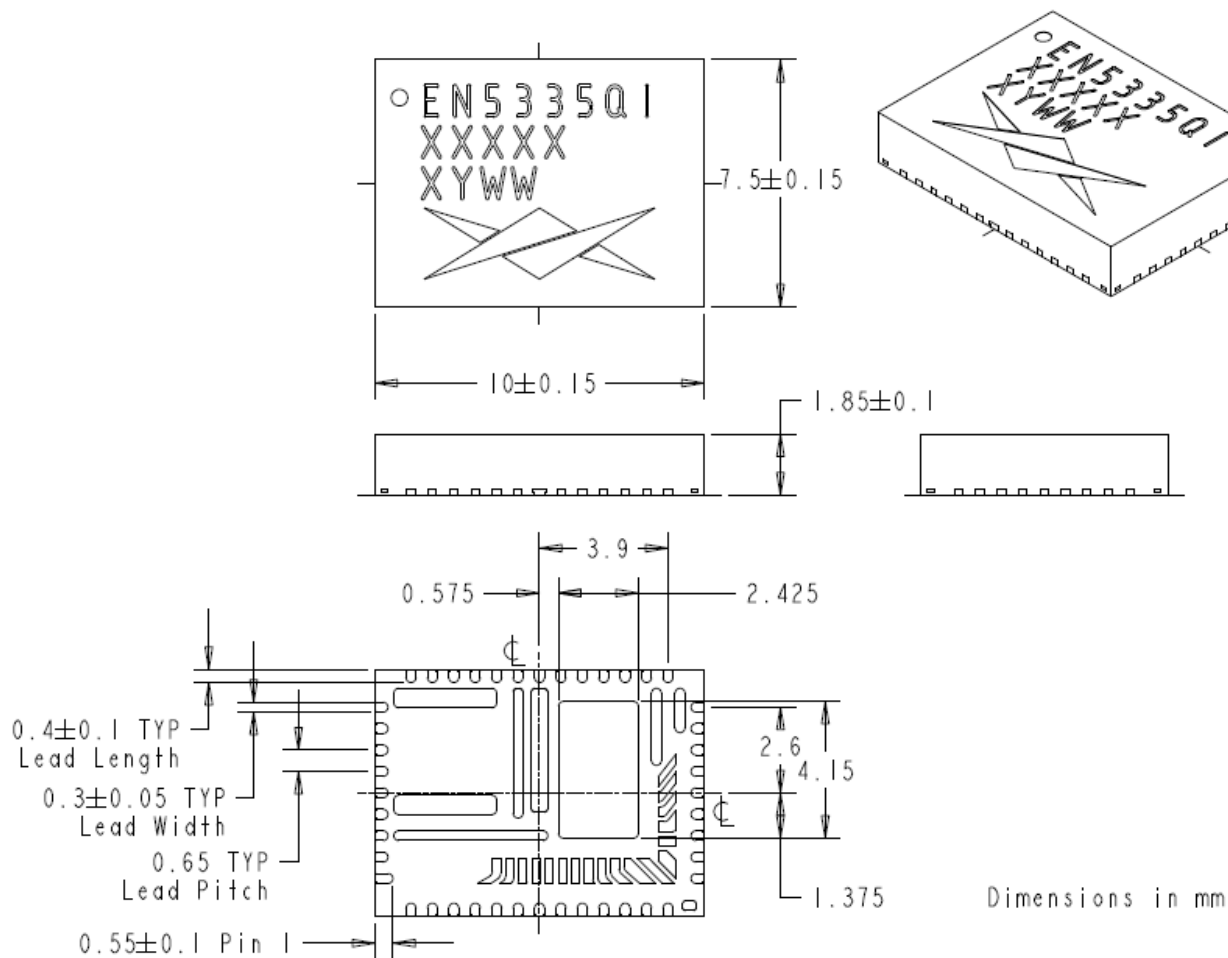


Figure 7. Package Dimensions

Contact Information

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