Enpirion® Power Datasheet EC7100VQI PWM DC/DC Controller with VS Inputs for FPGA Power Regulator

The Altera® Enpirion® EC7100VQI is a Single-Phase Synchronous-Buck PWM controller. The wide 3.3V to 25V input voltage range is ideal for systems that run on battery or AC-adapter power sources. The EC7100VQI is a low-cost solution for applications requiring dynamically selected slew-rate controlled output voltages. The soft-start and dynamic setpoint slew-rates are capacitor programmed. Voltage identification logic-inputs select four resistor-programmed setpoint reference voltages that directly set the output voltage of the converter between 0.5V and 1.5V, and up to 5V with a feedback voltage divider.

The EC7100VQI modulator has equivalent light-load efficiency, faster transient performance, accurately regulated frequency control and all internal compensation. These updates, together with integrated MOSFET drivers and schottky bootstrap diode, allow for a high-performance regulator that is highly compact and needs few external components. The EC7100VQI has differential remote sensing for output voltage and selectable switching frequency. For maximum efficiency, the converter automatically enters diode-emulation mode (DEM) during light-load conditions such as system standby.

Features

- Input Voltage Range: 3.3V to 25V
- Output Voltage Range: 0.5V to 5V
- Precision Regulation
  - Frequency Control Loop
  - ±0.5% System Accuracy Over -10°C to +100°C
- Optimal Transient Response
- Output Remote Sense
- Extremely Flexible Output Voltage Programmability
  - 2-Bit VS Selects Four Independent Setpoint Voltages
  - Simple Resistor Programming of Setpoint Voltages
- Selectable 300kHz, 500kHz, 600kHz or 1MHz PWM Frequency in Continuous Conduction
- Automatic Diode Emulation Mode for Highest Efficiency
- Power-OK Monitor for Soft-Start and Fault Detection

Applications

- FPGA power
- Digital processor power
- Mixed-signal ASIC power

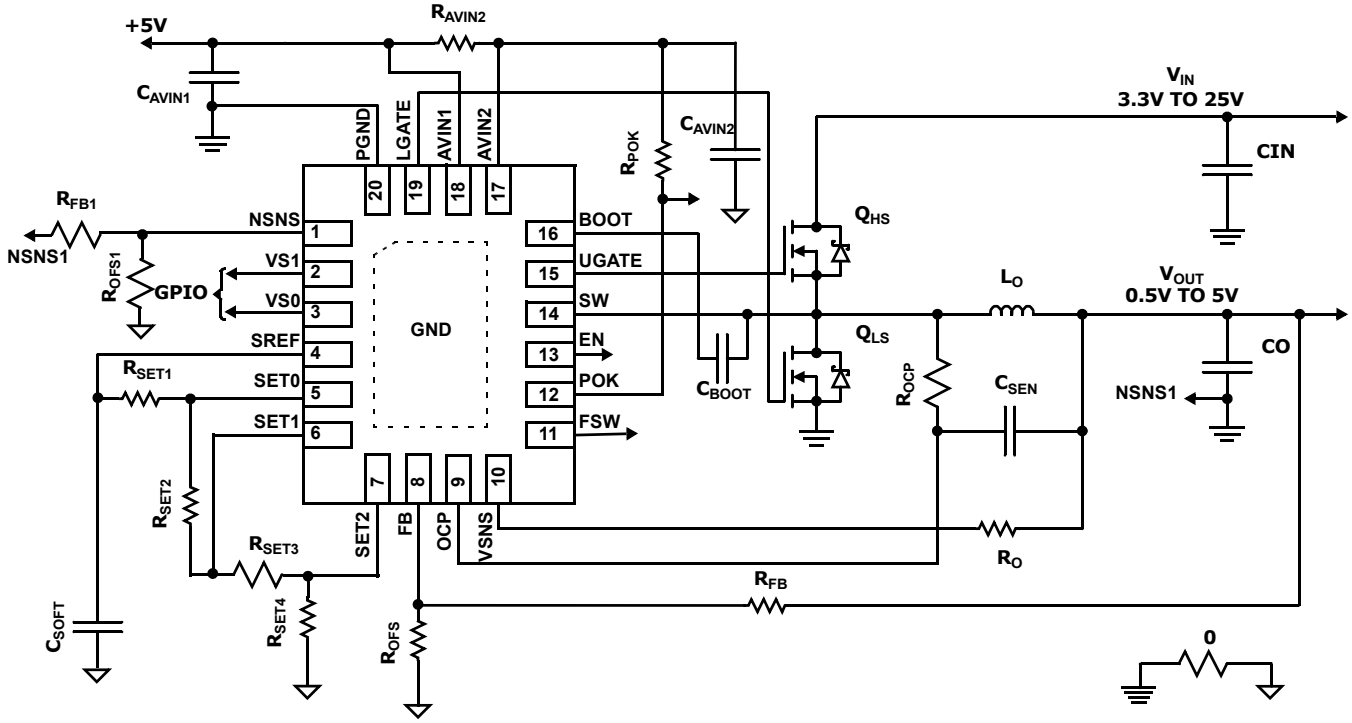

FIGURE 1. EC7100VQI APPLICATION SCHEMATIC WITH FOUR OUTPUT VOLTAGE SETPOINTS AND DCR CURRENT SENSE

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Ordering Information

PART NUMBER (Note 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
EC7100VQI (Note 1)	7100	-10 to +100	20 Ld 3x4 QFN	L20.3x4

NOTES:

1. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Applications Schematics: EC7100VQI

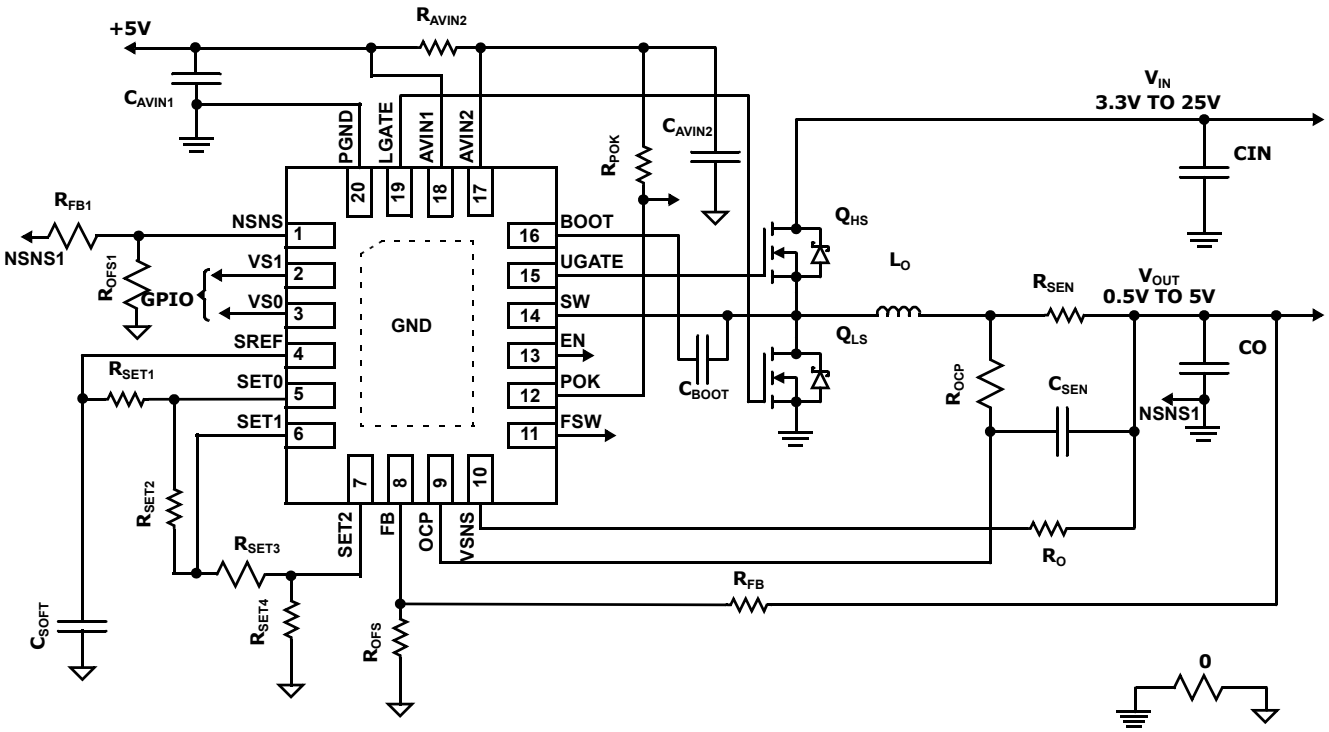


FIGURE 2. EC7100VQI APPLICATION SCHEMATIC WITH FOUR OUTPUT VOLTAGE SETPOINTS AND RESISTOR CURRENT SENSE

Block Diagram

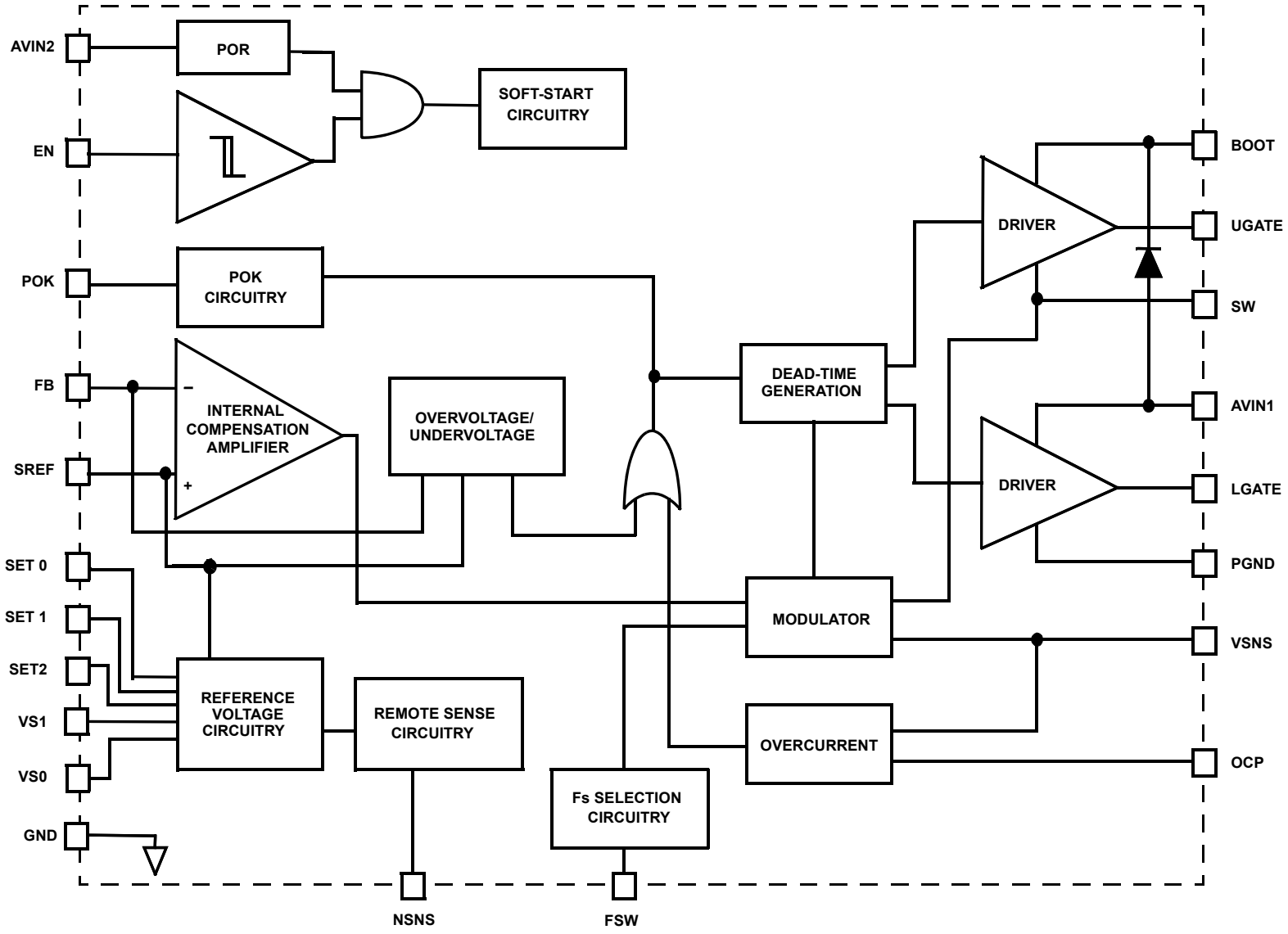
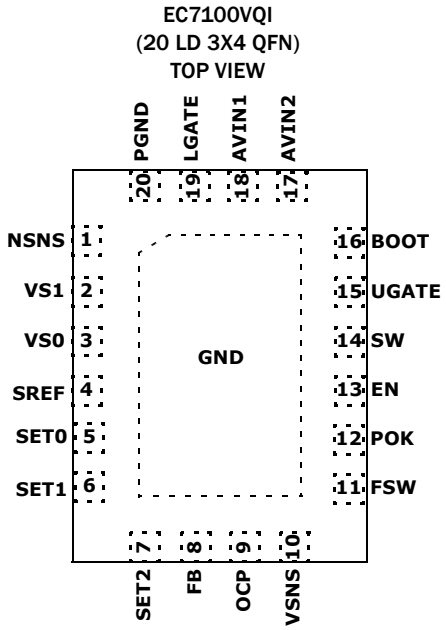


FIGURE 3. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF EC7100VQI

Pin Configurations



EC7100VQI Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	NSNS	Negative remote sense input of V_{OUT}. If resistor divider consisting of R_{FB} and R_{OFS} is used at FB pin, the same resistor divider should be used at NSNS pin, i.e. keep R_{FB1}=R_{FB}, and R_{OFS1}=R_{OFS}.
2	VS1	Logic input for setpoint voltage selector. Use in conjunction with the VS0 pin to select among four setpoint reference voltages.
3	VS0	Logic input for setpoint voltage selector. Use in conjunction with the VS1 pin to select among four setpoint reference voltages.
4	SREF	Soft-start and voltage slew-rate programming capacitor input and setpoint reference voltage programming resistor input. Connects internally to the inverting input of the V_{SET} voltage setpoint amplifier.
5	SET0	Voltage set-point programming resistor input.
6	SET1	Voltage set-point programming resistor input.
7	SET2	Voltage set-point programming resistor input.
8	FB	Voltage feedback sense input. Connects internally to the inverting input of the control-loop error transconductance amplifier. The converter is in regulation when the voltage at the FB pin equals the voltage on the SREF pin.
9	OCP	Input for the overcurrent detection circuit. The overcurrent setpoint programming resistor R_{OCP} connects from this pin to the sense node.
10	VSNS	Output voltage sense input for the modulator. The VSNS pin also serves as the reference input for the overcurrent detection circuit.
11	FSW	Input for programming the regulator switching frequency. Pull this pin to AVIN2 for 1MHz switching. Pull this pin to GND with a 100kΩ resistor for 600kHz switching. Leave this pin floating for 500kHz switching. Pull this pin directly to GND for 300kHz switching.
12	POK	Power-OK open-drain indicator output. This pin changes to high impedance when the converter is able to supply regulated voltage.
13	EN	Enable input for the IC. Pulling EN above the rising threshold voltage initializes the soft-start sequence.
14	SW	Return current path for the UGATE high-side MOSFET driver, V_{IN} sense input for the modulator, and inductor current polarity detector input.
15	UGATE	High-side MOSFET gate driver output. Connect to the gate terminal of the high-side MOSFET of the converter.
16	BOOT	Positive input supply for the UGATE high-side MOSFET gate driver. The BOOT pin is internally connected to the cathode of the Schottky boot-strap diode. Connect an MLCC between the BOOT pin and the SW pin.
17	AVIN2	Input for the IC bias voltage. Connect +5V to the AVIN2 pin and decouple with at least a MLCC to the GND pin.
18	AVIN1	Input for the LGATE and UGATE MOSFET driver circuits. The AVIN1 pin is internally connected to the anode of the Schottky boot-strap diode. Connect +5V to the AVIN1 pin and decouple with a MLCC to the PGND pin.
19	LGATE	Low-side MOSFET gate driver output. Connect to the gate terminal of the low-side MOSFET of the converter.
20	PGND	Return current path for the LGATE MOSFET driver. Connect to the source of the low-side MOSFET.
Bottom Pad	GND	IC ground for bias supply and signal reference.

Absolute Maximum Ratings

AVIN2, AVIN1, POK, FSW to GND . . . . . -0.3V to +7.0V
AVIN2, AVIN1to PGND . . . . . -0.3V to +7.0V
GND to PGND . . . . . -0.3V to +0.3V
EN, SET0, SET1, SET2, VSNS,
VS0, VS1, FB, NSNS, OCP, SREF . . -0.3V to GND, AVIN2 + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 33V
BOOT To SW Voltage ($V_{BOOT-SW}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
SW Voltage. . . . . GND - 0.3V to 28V
GND -8V (<20ns Pulse Width, 10µJ)
UGATE Voltage . . . . . V_{SW} - 0.3V (DC) to V_{BOOT}
V_{SW} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to AVIN2 + 0.3V
. . . . . GND - 2.5V (<20ns Pulse Width, 5µJ) to AVIN2 + 0.3V
ESD Rating
Human Body Model 2kV
Machine Model 200V
Charged Device Model 1kV
Latch Up . . . . . JEDEC Class II Level A at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld µTQFN (Note 2)	90	N/A
20 Ld µTQFN (Note 2)	88	N/A
20 Ld QFN (Notes 3, 4).	44	5

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range:
EC7100VQI . . . . . -40°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . —

Recommended Operating Conditions

Ambient Temperature Range:
EC7100VQI . . . . . -40°C to +100°C
Converter Input Voltage to GND . . . . . 3.3V to 25V
AVIN2, AVIN1 to GND. . . . . 5V ±5%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.
4. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

All typical specifications T_A = +25°C, AVIN2 = 5V. Boldface limits apply over the operating temperature range, -40°C to +100°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
AVIN2 and AVIN1						
AVIN2 Input Bias Current	I_{AVIN2}	EN = 5V, AVIN2 = 5V, FB = 0.55V, SREF < FB	-	1.2	1.9	mA
AVIN2 Shutdown Current	$I_{AVIN2off}$	EN = GND, AVIN2 = 5V	-	0	1.0	µA
AVIN1 Shutdown Current	$I_{AVIN1off}$	EN = GND, AVIN1 = 5V	-	0	1.0	µA
AVIN2 POR THRESHOLD						
Rising AVIN2 POR Threshold Voltage	V_{AVIN2_THR}		4.40	4.52	4.60	V
Falling AVIN2 POR Threshold Voltage	V_{AVIN2_THF}		4.10	4.22	4.35	V
REGULATION						
System Accuracy		VS0 = VS1 = AVIN2, PWM Mode = CCM	-0.5	-	+0.5	%
		VS0 = VS1 = AVIN2, PWM Mode = CCM	-0.75		+0.5	%
PWM						
Switching Frequency Accuracy	F_{SW}	PWM Mode = CCM	-15	-	+15	%
		PWM Mode = CCM	-22	-	+15	%
VSNS						
VSNS Input Impedance	R_{VSNS}	EN = 5V	-	600	-	kΩ
VSNS Reference Offset Current	I_{VSNS}	V_{ENTHR} < EN, SREF = Soft-Start Mode	-	8.5	-	µA
VSNS Input Leakage Current	$I_{VSNSoff}$	EN = GND, VSNS = 3.6V	-	0	-	µA

Electrical Specifications

All typical specifications T_A = +25°C, AVIN2 = 5V. Boldface limits apply over the operating temperature range, -40°C to +100°C, unless otherwise stated. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}	EN = 5V, FB = 0.50V	-20	-	+50	nA
SREF (Note 5)						
Soft-Start Current	I_{SS}	SREF = Soft-Start Mode	8.5	17	25.5	µA
Voltage Step Current	I_{VS}	SREF = Setpoint-Stepping Mode	±51	85	±119	µA
		SREF = Setpoint-Stepping Mode	±46	±85	±127	µA
POWER OK						
POK Pull-down Impedance	R_{POK}	POK = 5mA Sink	-	50	150	W
POK Leakage Current	I_{POK}	POK = 5V	-	0.1	1.0	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA Source Current	-	1.1	1.7	W
UGATE Source Current	I_{UGSRC}	UGATE - SW = 2.5V	-	1.8	-	A
UGATE Sink Resistance	R_{UGPD}	250mA Sink Current	-	1.1	1.7	W
UGATE Sink Current	I_{UGSNK}	UGATE - SW = 2.5V	-	1.8	-	A
LGATE Pull-Up Resistance	R_{LGPU}	250mA Source Current	-	1.1	1.7	W
LGATE Source Current	I_{LGSRC}	LGATE - GND = 2.5V	-	1.8	-	A
LGATE Sink Resistance	R_{LGPD}	250mA Sink Current	-	0.55	1.0	W
LGATE Sink Current	I_{LGSNK}	LGATE - PGND = 2.5V	-	3.6	-	A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load	-	21	-	ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load	-	21	-	ns
SW						
SW Input Impedance	R_{SW}		-	33	-	kΩ
BOOTSTRAP DIODE						
Forward Voltage	V_F	AVIN1 = 5V, I_F = 2mA	-	0.58	-	V
Reverse Leakage	I_R	V_R = 25V	-	0	-	µA
CONTROL INPUTS						
EN High Threshold Voltage	V_{ENTHR}		2.0	-	-	V
EN Low Threshold Voltage	V_{ENTHF}		-	-	1.0	V
EN Input Bias Current	I_{EN}	EN = 5V	0.85	1.7	2.55	µA
EN Leakage Current	I_{ENoff}	EN = GND	-	0	1.0	µA
VS<0,1> High Threshold Voltage	V_{VSTHR}		0.65	-	-	V
VS<0,1> Low Threshold Voltage	V_{VSTHF}		-	-	0.5	V
VS<0,1> Input Bias Current	I_{VS}	EN = 5V	-	0.5	-	µA
VS<0,1> Leakage Current	I_{VIDoff}	EN=0V	-	0	-	µA
PROTECTION						
OCP Threshold Voltage	V_{OCPTH}	V_{OCP} - VSNS	-1.75	-	1.75	mV

Electrical Specifications

All typical specifications T_A = +25°C, AVIN2 = 5V. Boldface limits apply over the operating temperature range, -40°C to +100°C, unless otherwise stated. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
OCP Reference Current	I_{OCP}	EN = 5.0V	7.65	8.5	9.35	µA
		EN = 5.0V	7.05	8.5	9.35	µA
OCP Input Resistance	R_{OCP}	EN = 5.0V	-	600	-	kΩ
OCP Leakage Current	I_{OCP}	EN = GND	-	0	-	µA
UVP Threshold Voltage	V_{UVTH}	V_{FB} = %V_{SREF}	81	84	87	%
OVP Rising Threshold Voltage	V_{OVRTH}	V_{FB} = %V_{SREF}	113	116	120	%
		V_{FB} = %V_{SREF}	112.5	116	120	%
OVP Falling Threshold Voltage	V_{OVFTH}	V_{FB} = %V_{SREF}	98	102	106	%
OTP Rising Threshold Temperature	T_{OTRTH}		-	150	-	°C
OTP Hysteresis	T_{OTHYS}		-	25	-	°C

NOTES:

5. For EC7100VQI,there is one internal reference 0.5V and there are four resistor-programmed reference voltages.
6. Limits established by characterization and are not production tested.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Theory of Operation

The following sections will provide a detailed description of the inner workings of the EC7100VQI.

Power-On Reset

The IC is disabled until the voltage at the AVIN2 pin has increased above the rising power-on reset (POR) threshold voltage V_{AVIN2_THR}. The controller will become disabled when the voltage at the AVIN2 pin decreases below the falling POR threshold voltage V_{AVIN2_THF}. The POR detector has a noise filter of approximately 1µs.

Start-Up Timing

Once AVIN2 has ramped above V_{AVIN2_THR}, the controller can be enabled by pulling the EN pin voltage above the input-high threshold V_{ENTHR}. Approximately 20µs later, the voltage at the SREF pin begins slewing to the designated VS set-point. The converter output voltage at the FB feedback pin follows the voltage at the SREF pin. During soft-start, The regulator always operates in CCM until the soft-start sequence is complete.

Start-Up and Voltage-Step Operation

When the voltage on the AVIN2 pin has ramped above the rising power-on reset voltage V_{AVIN2_THR}, and the voltage on the EN pin has increased above the rising enable threshold voltage V_{ENTHR}, the SREF pin releases its discharge clamp and enables the reference amplifier V_{SET}. The soft-start current I_{SS} is limited to 17µA and is sourced out of the SREF pin into the parallel RC network of capacitor C_{SOFT} and resistance R_T. The resistance R_T is the sum of all the series connected R_{SET} programming resistors and is written as Equation 1:

$$R_T = R_{SET1} + R_{SET2} + \ldots R_{SET(n)} \quad \textbf{(EQ. 1)}$$

The voltage on the SREF pin rises as I_{SS} charges C_{SOFT} to the voltage reference setpoint selected by the state of the VS inputs at the time the EN pin is asserted. The regulator controls the PWM such that the voltage on the FB pin tracks the rising voltage on the SREF pin. Once C_{SOFT} charges to the selected setpoint voltage, the I_{SS} current source comes out of the 17µA current limit and decays to the static value set by V_{SREF}/R_T. The elapsed time from when the EN pin is asserted to when V_{SREF} has reached the voltage reference setpoint is the soft-start delay t_{SS} which is given by Equation 2:

$$t_{SS} = -(R_T \cdot C_{SOFT}) \cdot LN\left(1 - \frac{V_{START\text{-}UP}}{I_{SS} \cdot R_T}\right) \quad \textbf{(EQ. 2)}$$

Where:

- I_{SS} is the soft-start current source at the 17µA limit
- $V_{START-UP}$ is the setpoint reference voltage selected by the state of the VS inputs at the time EN is asserted
- R_T is the sum of the R_{SET} programming resistors

The end of soft-start is detected by I_{SS} tapering off when capacitor C_{SOFT} charges to the designated V_{SET} voltage reference setpoint. The SSOK flag is set, and the POK pin goes high.

The I_{SS} current source changes over to the voltage-step current source I_{VS} which has a current limit of ±85µA. Whenever the VS inputs or the external setpoint reference programs a different setpoint reference voltage, the I_{VS} current source charges or discharges capacitor C_{SOFT} to that new level at ±85µA. Once C_{SOFT} charges to the selected setpoint voltage, the I_{VS} current source comes out of the 85µA current limit and decays to the static value set by V_{SREF}/R_T. The elapsed time to charge C_{SOFT} to the new voltage is called the voltage-step delay t_{VS} and is given by Equation 3:

$$t_{VS} = -(R_T \cdot C_{SOFT}) \cdot LN(1 - \frac{(V_{NEW} - V_{OLD})}{I_{VS} \cdot R_T}) \quad \textbf{(EQ. 3)}$$

Where:

- I_{VS} is the ±85µA setpoint voltage-step current; positive when $V_{NEW} > V_{OLD}$, negative when $V_{NEW} < V_{OLD}$
- V_{NEW} is the new setpoint voltage selected by the VS inputs
- V_{OLD} is the setpoint voltage that V_{NEW} is changing from
- R_T is the sum of the R_{SET} programming resistors

Choosing the C_{SOFT} capacitor to meet the requirements of a particular soft-start delay t_{SS} is calculated with Equation 4, which is written as:

$$C_{SOFT} = \frac{-t_{SS}}{\left(R_T \cdot LN(1 - \frac{V_{START-UP}}{I_{SS} \cdot R_T})\right)} \quad \textbf{(EQ. 4)}$$

Where:

- t_{SS} is the soft-start delay
- I_{SS} is the soft-start current source at the 17µA limit
- $V_{START-UP}$ is the setpoint reference voltage selected by the state of the VS inputs at the time EN is asserted
- R_T is the sum of the R_{SET} programming resistors

Choosing the C_{SOFT} capacitor to meet the requirements of a particular voltage-step delay t_{VS} is calculated with Equation 5, which is written as:

$$C_{SOFT} = \frac{-t_{VS}}{\left(R_T \cdot LN(1 - \frac{V_{NEW} - V_{OLD}}{I_{VS} \cdot R_T})\right)} \quad \textbf{(EQ. 5)}$$

Where:

- t_{VS} is the voltage-step delay
- V_{NEW} is the new setpoint voltage
- V_{OLD} is the setpoint voltage that V_{NEW} is changing from
- I_{VS} is the ±85µA setpoint voltage-step current; positive when $V_{NEW} > V_{OLD}$, negative when $V_{NEW} < V_{OLD}$
- R_T is the sum of the R_{SET} programming resistors

Output Voltage Programming

The EC7100VQI allows the user to select four different reference voltages, thus four different output voltages, by voltage identification pins VS1 and VS0. The maximum reference voltage cannot be designed higher than 1.5V. The implementation scheme is shown in Figure 4. The setpoint reference voltages are programmed with resistors that use the naming convention $R_{SET(x)}$ where (x) is the first, second, third, or fourth programming resistor connected in series starting at the SREF pin and ending at the GND pin. As shown in Table 1, different combinations of VS1 and VS0 close different switches and leave other switches open. For example, for the case of VS1 = 1 and
VS0 = 0, switch SW1 closes and all the other three switches SW0, SW2 and SW3 are open. For one combination of VS1 and VS0,

the internal switch connects the inverting input of the V_{SET} amplifier to a specific node among the string of R_{SET} programming resistors. All the resistors between that node and the SREF pin serve as the feedback impedance R_F of the V_{SET} amplifier. Likewise, all the resistors between that node and the GND pin serve as the input impedance R_{IN} of the V_{SET} amplifier. Equation 6 gives the general form of the gain equation for the V_{SET} amplifier:

$$V_{SETX} = V_{REF} \cdot \left(1 + \frac{R_F}{R_{IN}}\right) \quad \textbf{(EQ. 6)}$$

Where:

- V_{REF} is the 0.5V internal reference of the IC
- V_{SETx} is the resulting setpoint reference voltage that appears at the SREF pin

TABLE 1. EC7100VQI VS TRUTH TABLE

VS STATE		RESULT		
VS1	VS0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 7, 8, 9 and 10 give the specific V_{SET} equations for the EC7100VQI setpoint reference voltages.

The EC7100VQI V_{SET1} setpoint is written as Equation 7:

$$V_{SET1} = V_{REF} \quad \textbf{(EQ. 7)}$$

The EC7100VQI V_{SET2} setpoint is written as Equation 8:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \textbf{(EQ. 8)}$$

The EC7100VQI V_{SET3} setpoint is written as Equation 9:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \textbf{(EQ. 9)}$$

The EC7100VQI V_{SET4} setpoint is written as Equation 10:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \textbf{(EQ. 10)}$$

The V_{SET1} is fixed at 0.5V because it corresponds to the closure of internal switch SW0 that configures the V_{SET} amplifier as a unity-gain voltage follower for the 0.5V voltage reference V_{REF}. The setpoint reference voltages use the naming convention $V_{SET(x)}$ where (x) is the first, second, third, or fourth setpoint reference voltage where:

- $V_{SET1} < V_{SET2} < V_{SET3} < V_{SET4}$ Thus,
- $V_{OUT1} < V_{OUT2} < V_{OUT3} < V_{OUT4}$

For given four user selected reference voltages V_{SETx}, the programmed resistors R_{SET1}, R_{SET2}, R_{SET3} and R_{SET4} are designed in the following way. First, assign an initial value to R_{SET4} of approximately 100kΩ then calculate $R_{SET1,}$ R_{SET2} and R_{SET3} using Equations 11, 12, and 13 respectively.

$$R_{SET1} = \frac{R_{SET4} \cdot V_{SET4} \cdot (V_{SET2} - V_{REF})}{V_{REF} \cdot V_{SET2}} \quad \textbf{(EQ. 11)}$$

$$R_{SET2} = \frac{R_{SET4} \cdot V_{SET4} \cdot (V_{SET3} - V_{SET2})}{V_{SET2} \cdot V_{SET3}} \quad \textbf{(EQ. 12)}$$

$$R_{SET3} = \frac{R_{SET4} \cdot (V_{SET4} - V_{SET3})}{V_{SET3}} \quad \textbf{(EQ. 13)}$$

The sum of all the programming resistors should be approximately 300kΩ, as shown in Equation 14, otherwise adjust the value of R_{SET4} and repeat the calculations.

$$R_{SET1} + R_{SET2} + R_{SET3} + R_{SET4} \cong 300k\Omega \quad \text{(EQ. 14)}$$

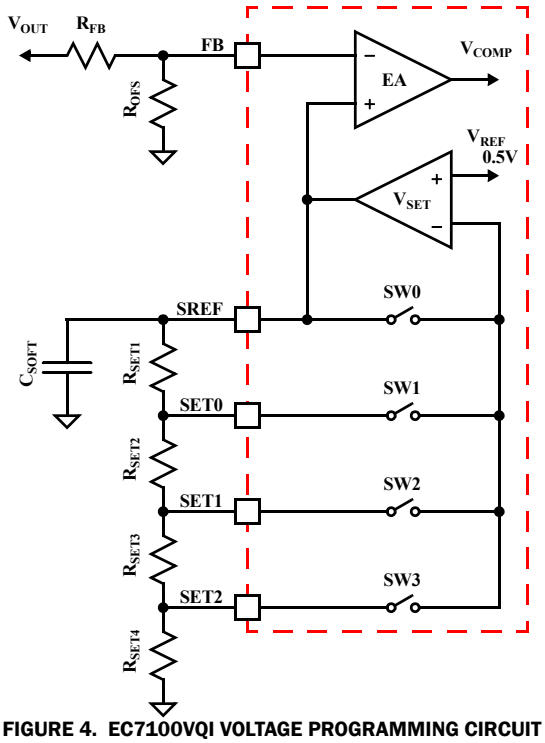


FIGURE 4. EC7100VQI VOLTAGE PROGRAMMING CIRCUIT

If the output voltage is in the range of 0.5V to 1.5V, the external resistor-divider is not necessary. The output voltage is equal to one of the reference voltages depending on the status of VS1 and VS0. The external resistor divider consisting of R_{FB} and R_{OFS} allows the user to program the output voltage in the range of 1.5V to 5V. The relation between the output voltage and the reference is given in Equation 15:

$$V_{OUT} = V_{SREF} \cdot \frac{R_{FB} + R_{OFS}}{R_{OFS}} = V_{SREF} \cdot k \quad \text{(EQ. 15)}$$

In this case, the four output voltages are equal to each of the corresponding reference voltages multiplying the factor k.

$$V_{OUTx} = V_{SETx} \cdot k \quad \text{(EQ. 16)}$$

High Output Voltage Programming

The EC7100VQI has a fixed 0.5V reference voltage (V_{SREF}). For high output voltage application, the resistor divider consisting of R_{FB} and R_{OFS} requires large ratio (R_{FB} :R_{OFS} = 9:1 for 5V output). The FB pin with large ratio resistor divider is noise sensitive and the PCB layout should be carefully routed. It is recommended to use small value resistor divider such as R_{FB}=1kΩ.

Modulator

The modulator allows variable frequency in response to load transients and maintains the benefits of current-mode hysteretic controllers. However, in addition, the modulator reduces regulator output impedance and uses accurate referencing to eliminate the need for a high-gain voltage amplifier in the compensation loop. The result is a topology that can be tuned to voltage-mode hysteretic transient speed while maintaining a linear control model and removes the need for any compensation. This greatly simplifies the regulator design for customers and reduces external component cost.

Stability

The removal of compensation derives from the modulator's lack of need for high DC gain. In traditional architectures, high DC gain is achieved with an integrator in the voltage loop. The integrator introduces a pole in the open-loop transfer function at low frequencies. That, combined with the double-pole from the output L/C filter, creates a three pole system that must be compensated to maintain stability.

Classic control theory requires a single-pole transition through unity gain to ensure a stable system. Current-mode architectures (includes peak, peak-valley, current-mode hysteretic) generate a zero at or near the L/C resonant point, effectively canceling one of the system's poles. The system still contains two poles, one of which must be canceled with a zero before unity gain crossover to achieve stability. Compensation components are added to introduce the necessary zero.

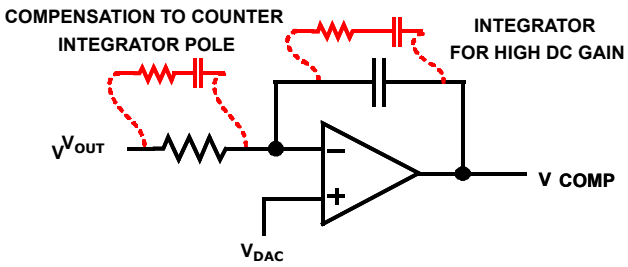


FIGURE 5. INTEGRATOR ERROR-AMPLIFIER CONFIGURATION

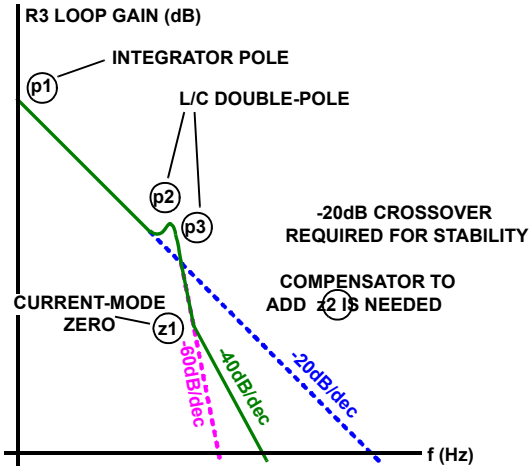


FIGURE 6. UNCOMPENSATED INTEGRATOR OPEN-LOOP RESPONSE

Figure 5 illustrates the classic integrator configuration for a voltage loop error-amplifier. While the integrator provides the high DC gain required for accurate regulation in traditional technologies, it also introduces a low-frequency pole into the control loop. Figure 6 shows the open-loop response that results from the addition of an integrating capacitor in the voltage loop. The compensation components found in Figure 5 are necessary to achieve stability.

Because the modulator does not require a high-gain voltage loop, the integrator can be removed, reducing the number of inherent poles in the loop to two. The current-mode zero continues to cancel one of the poles, ensuring a single-pole crossover for a wide

range of output filter choices. The result is a stable system with no need for compensation components or complex equations to properly tune the stability.

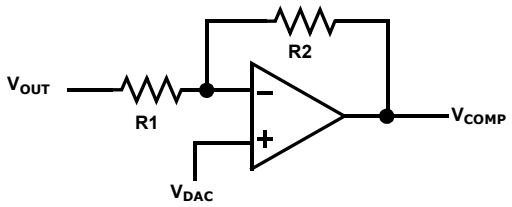


FIGURE 7. NON-INTEGRATED ERROR-AMPLIFIER CONFIGURATION

Figure 7 shows the error-amplifier that does not require an integrator for high DC gain to achieve accurate regulation. The result to the open loop response can be seen in Figure 8.

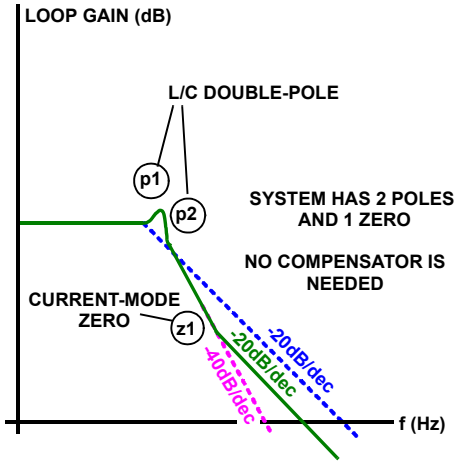


FIGURE 8. UNCOMPENSATED OPEN-LOOP RESPONSE

Transient Response

In addition to requiring a compensation zero, the integrator in traditional architectures also slows system response to transient conditions. The change in COMP voltage is slow in response to a rapid change in output voltage. If the integrating capacitor is removed, COMP moves as quickly as VOUT, and the modulator immediately increases or decreases switching frequency to recover the output voltage.

Diode Emulation

The polarity of the output inductor current is defined as positive when conducting away from the switch node, and defined as negative when conducting towards the switch node. The DC component of the inductor current is positive, but the AC component known as the ripple current, can be either positive or negative. Should the sum of the AC and DC components of the inductor current remain positive for the entire switching period, the converter is in continuous-conduction-mode (CCM). However, if the inductor current becomes negative or zero, the converter is in discontinuous-conduction-mode (DCM).

Unlike the standard DC/DC buck regulator, the synchronous rectifier can sink current from the output filter inductor during DCM, reducing the light-load efficiency with unnecessary conduction loss as the low-side MOSFET sinks the inductor current. The EC7100VQI controllers avoid the DCM conduction loss by making the low-side MOSFET emulate the current-blocking behavior of a diode. This smart-diode operation called diode-emulation-mode (DEM) is triggered when the negative inductor current produces a positive voltage drop across the $R_{DS(ON)}$ of the low-side MOSFET for eight consecutive PWM cycles while the LGATE pin is high. The converter will exit DEM on the next PWM pulse after detecting a negative voltage across the $R_{DS(ON)}$ of the low-side MOSFET.

It is characteristic of the architecture for the PWM switching frequency to decrease while in DCM, increasing efficiency by reducing unnecessary gate-driver switching losses. The extent of the frequency reduction is proportional to the reduction of load current. Upon entering DEM, the PWM frequency is forced to fall approximately 30% by forcing a similar increase of the window voltage V_W. This measure is taken to prevent oscillating between modes at the boundary between CCM and DCM. The 30%

increase of V_W is removed upon exit of DEM, forcing the PWM switching frequency to jump back to the nominal CCM value.

Overcurrent

The overcurrent protection (OCP) setpoint is programmed with resistor R_{OCP}, which is connected across the OCP and SW pins. Resistor R_O is connected between the VSNS pin and the actual output voltage of the converter. During normal operation, the VSNS pin is a high impedance path, therefore there is no voltage drop across R_O. The value of resistor R_O should always match the value of resistor R_{OCP}.

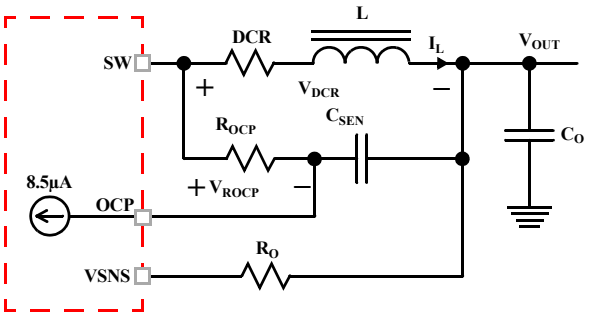


FIGURE 9. OVERCURRENT PROGRAMMING CIRCUIT

Figure 9 shows the overcurrent set circuit. The inductor consists of inductance L and the DC resistance DCR. The inductor DC current I_L creates a voltage drop across DCR, which is given by Equation 17:

$$V_{DCR} = I_L \cdot DCR \quad \textbf{(EQ. 17)}$$

The I_{OCP} current source sinks 8.5µA into the OCP pin, creating a DC voltage drop across the resistor R_{OCP}, which is given by Equation 18:

$$V_{ROCP} = 8.5\mu A \cdot R_{OCP} \quad \textbf{(EQ. 18)}$$

The DC voltage difference between the OCP pin and the VSNS pin, which is given by Equation 19:

$$V_{OCP} - V_{VO} = V_{DCR} - V_{ROCP} = I_L \cdot DCR - I_{OCP} \cdot R_{OCP} \quad \textbf{(EQ. 19)}$$

The IC monitors the voltage of the OCP pin and the VSNS pin. When the voltage of the OCP pin is higher than the voltage of the VSNS pin for more than 10µs, an OCP fault latches the converter off.

The value of R_{OCP} is calculated with Equation 20, which is written as:

$$R_{OC} = \frac{I_{OC} \cdot DCR}{I_{OCP}} \quad \textbf{(EQ. 20)}$$

Where:

- R_{OC} (Ω) is the resistor used to program the overcurrent setpoint
- I_{OC} is the output DC load current that will activate the OCP fault detection circuit
- DCR is the inductor DC resistance

For example, if I_{OC} is 20A and DCR is 4.5mΩ, the choice of R_{OCP} is equal to 20A x 4.5mΩ/8.5µA = 10.5kΩ.

Resistor R_{OCP} and capacitor C_{SEN} form an R-C network to sense the inductor current. To sense the inductor current correctly not only in DC operation, but also during dynamic operation, the R-C network time constant $R_{OCP}\,C_{SEN}$ needs to match the inductor time constant L/DCR. The value of C_{SEN} is then written as Equation 21:

$$C_{SEN} = \frac{L}{R_{OCP} \cdot DCR} \quad \textbf{(EQ. 21)}$$

For example, if L is 1.5µH, DCR is 4.5mΩ, and R_{OCP} is 9kΩ, the choice of C_{SEN} = 1.5µH/(9kΩ x 4.5mΩ) = 0.037µF.

When an OCP fault is declared, the converter will be latched off and the POK pin will be asserted low. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if AVIN2 has decayed below the falling POR threshold voltage V_{AVIN2_THF}.

Overvoltage

The OVP fault detection circuit triggers after the FB pin voltage is above the rising overvoltage threshold V_{OVRTH} for more than 2µs. For example, if the converter is programmed to regulate 1.0V at the FB pin, that voltage would have to rise above the typical V_{OVRTH} threshold of 116% for more than 2µs in order to trip the OVP fault latch. In numerical terms, that would be 116% x 1.0V = 1.16V. When an OVP fault is declared, the converter will be latched off and the POK pin will be asserted low. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if AVIN2 has decayed below the falling POR threshold voltage V_{AVIN2_THF}.

Although the converter has latched-off in response to an OVP fault, the LGATE gate-driver output will retain the ability to toggle the low-side MOSFET on and off, in response to the output voltage transversing the V_{OVRTH} and V_{OVFTH} thresholds. The LGATE gate-driver will turn-on the low-side MOSFET to discharge the output voltage, protecting the load. The LGATE gate-driver will turn-off the low-side MOSFET once the FB pin voltage is lower than the falling overvoltage threshold V_{OVRTH} for more than 2µs. The falling overvoltage threshold V_{OVFTH} is typically 102%. That means if the FB pin voltage falls below 102% x 1.0V = 1.02V for more than 2µs, the LGATE gate-driver will turn off the low-side MOSFET. If the output voltage rises again, the LGATE driver will again turn on the low-side MOSFET when the FB pin voltage is above the rising overvoltage threshold V_{OVRTH} for more than 2µs. By doing so, the IC protects the load when there is a consistent overvoltage condition.

Undervoltage

The UVP fault detection circuit triggers after the FB pin voltage is below the undervoltage threshold V_{UVTH} for more than 2µs. For example if the converter is programmed to regulate 1.0V at the FB pin, that voltage would have to fall below the typical V_{UVTH} threshold of 84% for more than 2µs in order to trip the UVP fault latch. In numerical terms, that would be 84% x 1.0V = 0.84V. When a UVP fault is declared, the converter will be latched off and the POK pin will be asserted low. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if AVIN2 has decayed below the falling POR threshold voltage V_{AVIN2_THF}.

Over-Temperature

When the temperature of the IC increases above the rising threshold temperature T_{OTRTH}, it will enter the OTP state that suspends the PWM, forcing the LGATE and UGATE gate-driver outputs low. The status of the POK pin does not change nor does the converter latch-off. The PWM remains suspended until the IC temperature falls below the hysteresis temperature T_{OTHYS} at which time normal PWM operation resumes. The OTP state can be reset if the EN pin is pulled below the falling EN threshold voltage V_{ENTHF} or if AVIN2 has decayed below the falling POR threshold voltage V_{AVIN2_THF}. All other protection circuits remain functional while the IC is in the OTP state. It is likely that the IC will detect an UVP fault because in the absence of PWM, the output voltage decays below the undervoltage threshold V_{UVTH}.

POK Monitor

The POK pin indicates when the converter is capable of supplying regulated voltage. The POK pin is an undefined impedance if the AVIN2 pin has not reached the rising POR threshold V_{AVIN2_THR}, or if the AVIN2 pin is below the falling POR threshold V_{AVIN2_THF}. If there is a fault condition of output overcurrent, overvoltage or undervoltage, POK is asserted low. The POK pull-down impedance is 50Ω.

Integrated MOSFET Gate-Drivers

The LGATE pin and UGATE pins are MOSFET driver outputs. The LGATE pin drives the low-side MOSFET of the converter while the UGATE pin drives the high-side MOSFET of the converter.

The LGATE driver is optimized for low duty-cycle applications where the low-side MOSFET experiences long conduction times. In this environment, the low-side MOSFETs require exceptionally low $R_{DS(ON)}$ and tend to have large parasitic charges that conduct transient currents within the devices in response to high dv/dt switching present at the switch node. The drain-gate charge in particular can conduct sufficient current through the driver pull-down resistance that the $V_{GS(th)}$ of the device can be exceeded and turned on. For this reason, the LGATE driver has been designed with low pull-down resistance and high sink current capability to ensure clamping the MOSFETs gate voltage below $V_{GS(th)}$.

Adaptive Shoot-Through Protection

Adaptive shoot-through protection prevents a gate-driver output from turning on until the opposite gate-driver output has fallen below approximately 1V. The dead-time shown in Figure 10 is extended by the additional period that the falling gate voltage remains above the 1V threshold. The high-side gate-driver output voltage is measured across the UGATE and SW pins while the low-side gate-driver output voltage is measured across the LGATE and PGND pins. The power for the LGATE gate-driver is sourced directly from the AVIN1 pin. The-power for the UGATE gate-driver is supplied by a boot-strap capacitor connected across

the BOOT and SW pins. The capacitor is charged each time the switch node voltage falls a diode drop below AVIN1 such as when the low-side MOSFET is turned on.

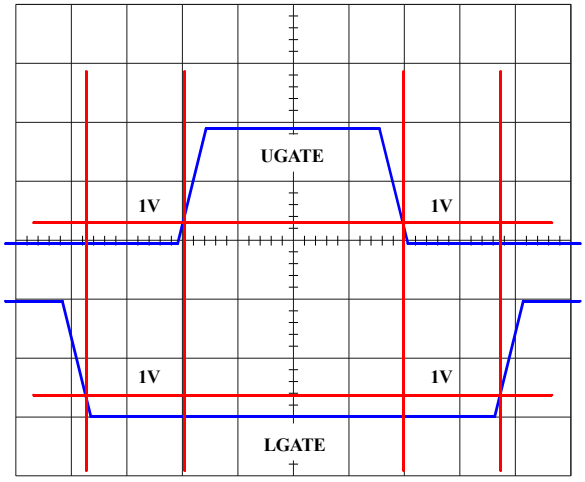


FIGURE 10. GATE DRIVE ADAPTIVE SHOOT-THROUGH PROTECTION

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase buck converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Altera provides complete reference designs that include schematics, bills of materials, and example board layouts.

Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is expressed in Equation 22:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \textbf{(EQ. 22)}$$

The output inductor peak-to-peak ripple current is expressed in Equation 23:

$$I_{P\text{-}P} = \frac{V_{OUT} \cdot (1 - D)}{F_{SW} \cdot L} \quad \textbf{(EQ. 23)}$$

A typical step-down DC/DC converter will have an I_{PP} of 20% to 40% of the maximum DC output load current. The value of $I_{P\text{-}P}$ is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated using Equation 24:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \textbf{(EQ. 24)}$$

Where, I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR of the inductor. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current $I_{P\text{-}P}$ can flow. Current $I_{P\text{-}P}$ develops a corresponding ripple voltage $V_{P\text{-}P}$ across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are expressed in Equations 25 and 26:

$$\Delta V_{ESR} = I_{P\text{-}P} \cdot ESR \quad \textbf{(EQ. 25)}$$

$$\Delta V_{C} = \frac{I_{P\text{-}P}}{8 \cdot C_O \cdot F_{SW}} \quad \textbf{(EQ. 26)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can significantly impact the output voltage ripple and cause a brief voltage spike if the load transient has an extremely high slew rate. Low inductance capacitors should be considered. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at F_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Selecting the Input Capacitor

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 11 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle that is adjusted for converter efficiency. The ripple current calculation is written as Equation 27:

$$I_{IN\_RMS} = \frac{\sqrt{(I_{MAX}^2 \cdot (D - D^2)) + \left(x^2 \cdot I_{MAX}^2 \cdot \frac{D}{12}\right)}}{I_{MAX}} \quad \textbf{(EQ. 27)}$$

Where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- x is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter

Duty cycle is written as Equation 28:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \textbf{(EQ. 28)}$$

In addition to the bulk capacitors, some low ESL ceramic capacitors are recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

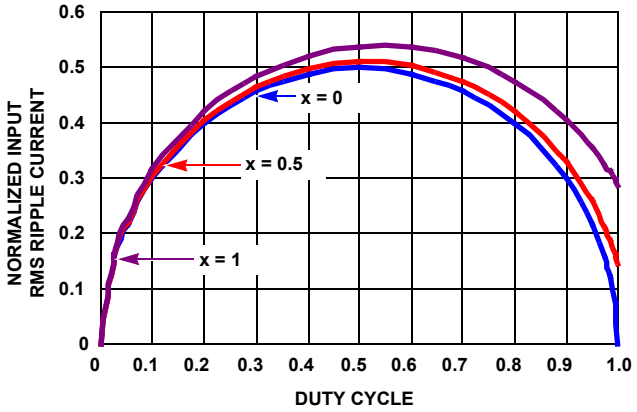


FIGURE 11. NORMALIZED INPUT RMS CURRENT FOR EFF = 1

Selecting the Bootstrap Capacitor

The integrated driver features an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and SW pins completes the bootstrap circuit. The bootstrap capacitor voltage rating is selected to be at least 10V. Although the theoretical

maximum voltage of the capacitor is AVIN1-V_{DIODE} (voltage drop across the boot diode), large excursions below ground by the switch node requires at least a 10V rating for the bootstrap capacitor. The bootstrap capacitor can be chosen from Equation 29:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \textbf{(EQ. 29)}$$

Where:

- Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET
- ΔV_{BOOT} is the maximum decay across the BOOT capacitor

As an example, suppose the high-side MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V, and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF will suffice. Use a low temperature-coefficient ceramic capacitor.

Driver Power Dissipation

Switching power dissipation in the driver is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. When designing the application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the drivers is approximated as Equation 30:

$$P = F_{sw}(1.5V_U Q_U + V_L Q_L) + P_L + P_U \quad \textbf{(EQ. 30)}$$

Where:

- F_{sw} is the switching frequency of the PWM signal
- V_U is the upper gate driver bias supply voltage
- V_L is the lower gate driver bias supply voltage
- Q_U is the charge to be delivered by the upper driver into the gate of the MOSFET and discrete capacitors
- Q_L is the charge to be delivered by the lower driver into the gate of the MOSFET and discrete capacitors
- P_L is the quiescent power consumption of the lower driver
- P_U is the quiescent power consumption of the upper driver

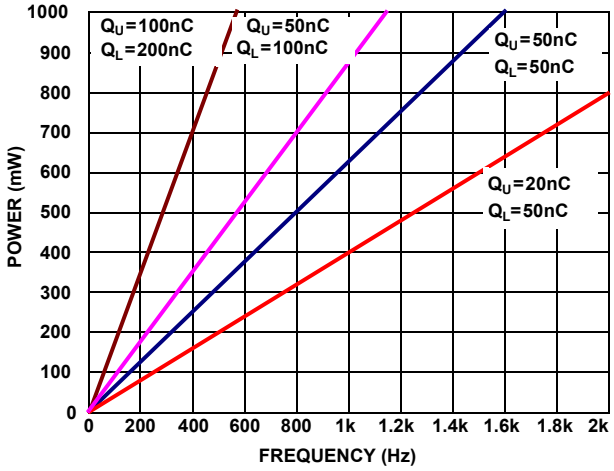


FIGURE 12. POWER DISSIPATION vs FREQUENCY

MOSFET Selection and Considerations

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum V_{DS} rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFETs switch.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. The preferred low-side MOSFET emphasizes low $R_{DS(ON)}$ when fully saturated to minimize conduction loss.

For the low-side MOSFET, (LS), the power loss can be assumed to be conductive only and is written as Equation 31:

$$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1 - D) \quad \textbf{(EQ. 31)}$$

For the high-side MOSFET, (HS), its conduction loss is written as Equation 32:

$$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D \quad \textbf{(EQ. 32)}$$

For the high-side MOSFET, its switching loss is written as Equation 33:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot F_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot F_{SW}}{2} \quad \textbf{(EQ. 33)}$$

Where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Layout Considerations

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground-plane layer should be adjacent to the signal layer to provide shielding. The ground plane layer should have an island located under the IC, the components connected to analog or logic signals. The island should be connected to the rest of the ground plane layer at one quiet point.

There are two sets of components in a DC/DC converter, the power components and the small signal components. The power components are the most critical because they switch large amount of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, PGND, SW and BOOT.

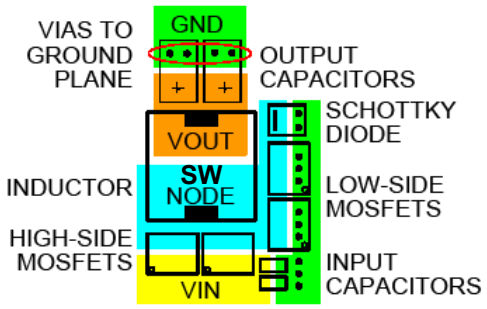


FIGURE 13. TYPICAL POWER COMPONENT PLACEMENT

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible. See Figure 13. Input high frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target, making use of the shortest

connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and switch node signals.

AVIN2 AND AVIN1 PINS

Place the decoupling capacitors as close as practical to the IC. In particular, the AVIN1 decoupling capacitor should have a very short and wide connection to the PGND pin. The AVIN2 decoupling capacitor should be referenced to GND pin.

EN, POK, VS0, VS1, AND FSW PINS

These are logic signals that are referenced to the GND pin. Treat as a typical logic signal.

OCP AND VSNS PINS

The current-sensing network consisting of R_{OCP}, RO, and CSEN needs to be connected to the inductor pads for accurate measurement of the DCR voltage drop. These components however, should be located physically close to the OCP and VSNS pins with traces leading back to the inductor. It is critical that the traces are shielded by the ground plane layer all the way to the inductor pads. The procedure is the same for resistive current sense.

FB, SREF, SET0, SET1, SET2, AND NSNS PINS

The input impedance of these pins is high, making it critical to place the components connected to these pins as close as possible to the IC.

LGATE, PGND, UGATE, BOOT, AND SW PINS

The signals going through these traces are high dv/dt and high di/dt, with high peak charging and discharging current. The PGND pin can only flow current from the gate-source charge of the low-side MOSFETs when LGATE goes low. Ideally, route the trace from the LGATE pin in parallel with the trace from the PGND pin, route the trace from the UGATE pin in parallel with the trace from the SW pin. In order to have more accurate zero-crossing detection of inductor current, it is recommended to connect SW pin to the drain of the low-side MOSFETs with Kelvin connection. These pairs of traces should be short, wide, and away from other traces with high input impedance; weak signal traces should not be in proximity with these traces on any layer.

Document Revision History

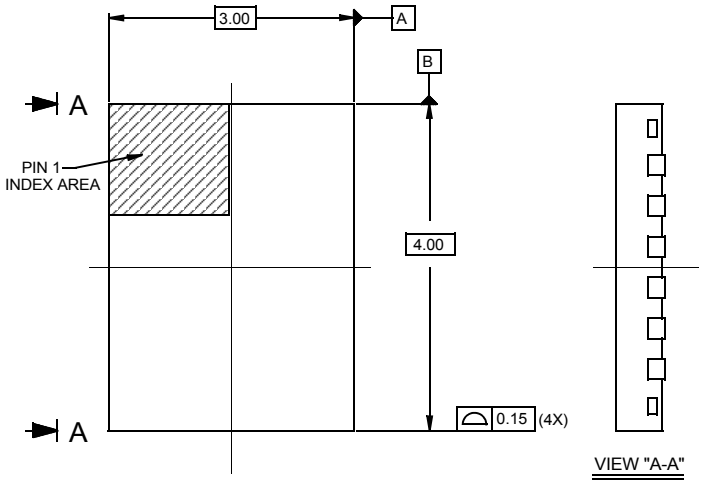
The table lists the revision history for this document.

Date	Version	Changes
March 2014	1.0	Initial release.

Package Outline Drawing

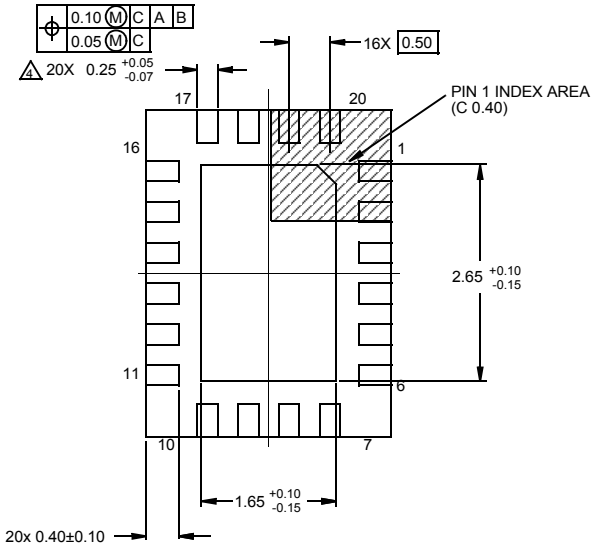
L20.3x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

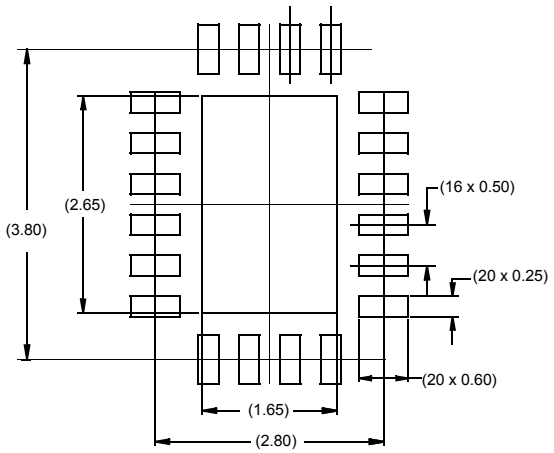


TOP VIEW

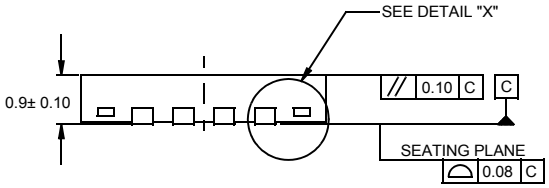
VIEW "A-A"



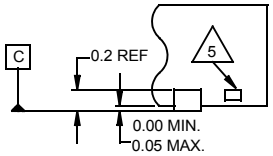
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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