Enpirion® Power Datasheet EC7401QI 4-Phase PWM Controller with 8-Bit DAC Code

The Altera® Enpirion® EC7401QI controls microprocessor core voltage regulation by driving up to 4 synchronous-rectified buck channels in parallel. The EC7401QI can precision R_{DS}(ON) or DCR Differential Current Sensing. Multiphase buck converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area.

Microprocessor loads can generate load transients with extremely fast edge rates. The EC7401QI features a high bandwidth control loop and ripple frequencies up to >4MHz to provide optimal response to the transients.

Today's microprocessors require a tightly regulated output voltage position versus load current (droop). The EC7401QI senses current by utilizing patented techniques to measure the voltage across the on resistance, R_{DS}(ON), of the lower MOSFETs or DCR of the output inductor during the lower MOSFET conduction intervals. Current sensing provides the needed signals for precision droop, channel-current balancing, and overcurrent protection. A programmable internal temperature compensation function is implemented to effectively compensate for the temperature coefficient of the current sense element.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds can be completely eliminated using the remote-sense amplifier. Eliminating ground differences improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start up of the EC7401QI with any other voltage rail. VID Voltage Scaling technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting.

Features

- Precision Multiphase Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Life, Load, Line and Temperature
  - Adjustable Precision Reference-Voltage Offset
- Precision R_{DS}(ON) or DCR Current Sensing
  - Accurate Load-Line Programming
  - Accurate Channel-Current Balancing
  - Differential Current Sense
- Microprocessor Voltage Identification Input
  - VID Voltage Scaling Technology
  - 8-Bit VID Input with Selectable VR11 Code and Extended VR10 Code at 6.25mV per Bit
  - 0.5V to 1.6V Operation Range
- Thermal Sensing
- Integrated Programmable Temperature Compensation
- Threshold-Sensitive Enable Function for Power Sequencing and VTT Enable
- Overcurrent Protection
- Overvoltage Protection
- 2-, 3- or 4-Phase Operation
- Adjustable Switching Frequency Up to 1MHz Per Phase
- Package Option
  - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-Free (RoHS Compliant)

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Ordering Information

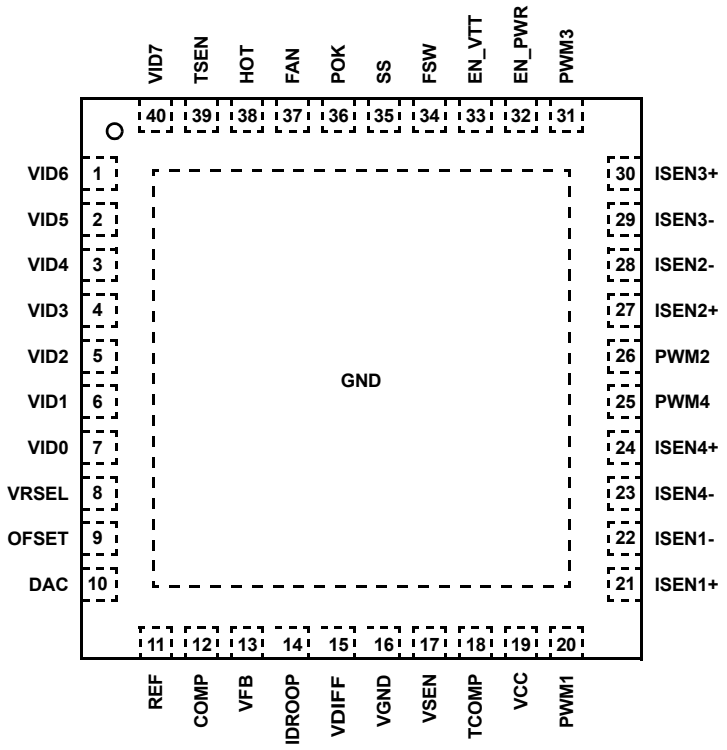
PART NUMBER (Note)	PART MARKING	TEMP. (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
EC7401QI	EC7401	-40 to +85	40 Ld 6x6 QFN	**L40.6x6**

*Add “-T” suffix for tape and reel.

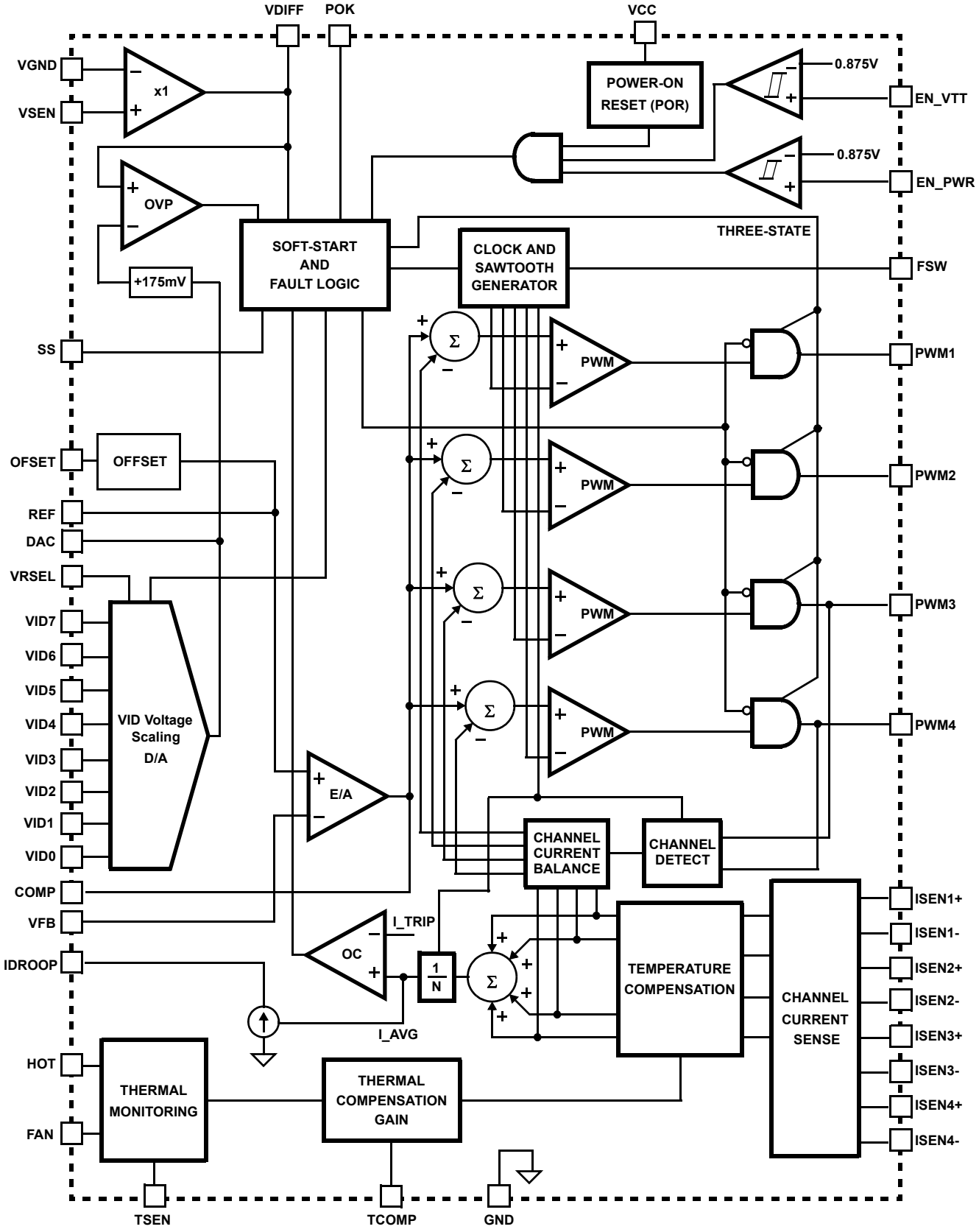
NOTE: These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

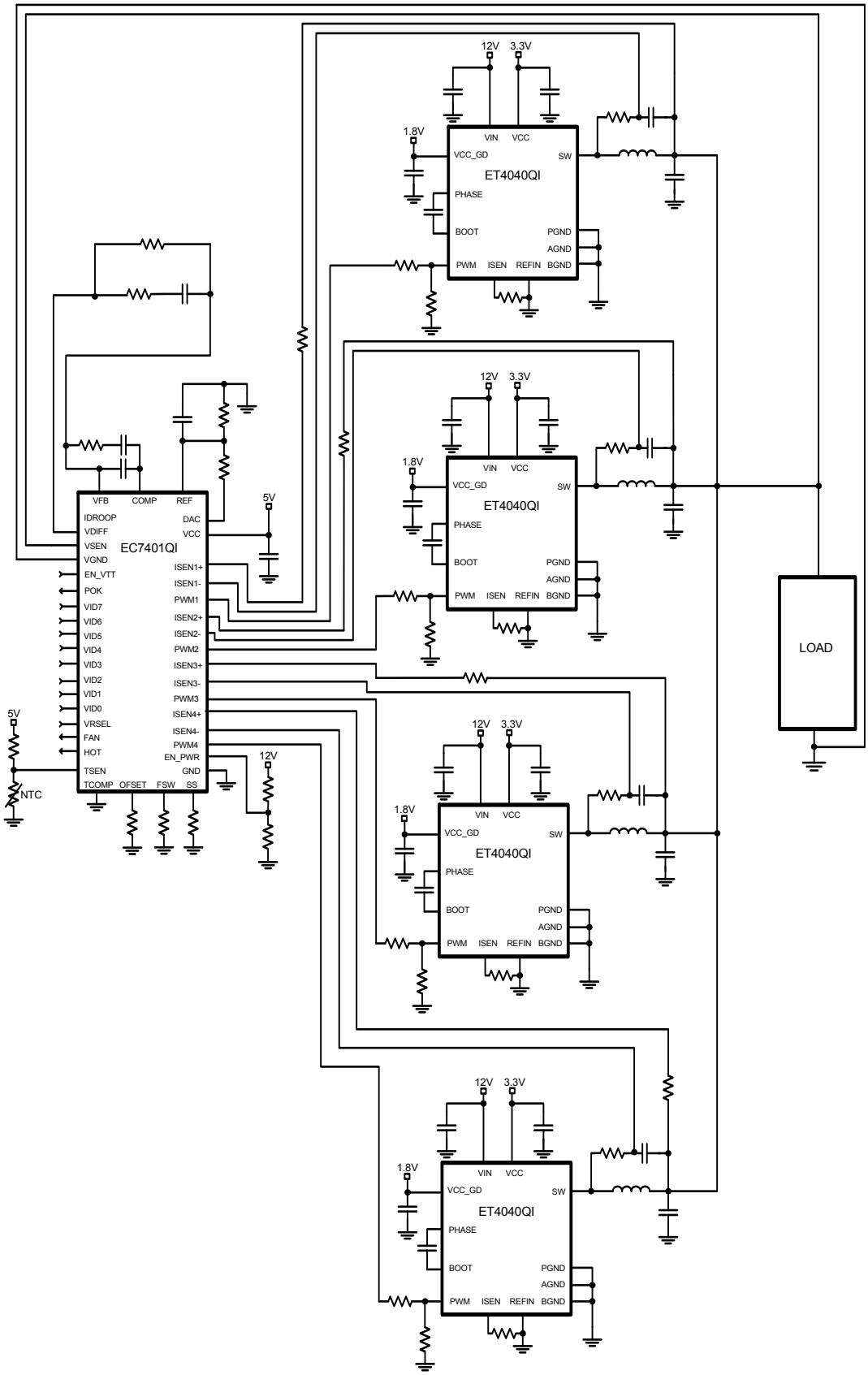
EC7401QI
(40 LD QFN)
TOP VIEW



EC7401QI Block Diagram



Typical Application - 4-Phase Buck Converter with DCR Sensing and External TCOMP



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . +6V
All Pins . . . . . GND -0.3V to VCC + 0.3V
ESD Ratings
Human body model . . . . . >2kV
Machine model . . . . . >200V
Charged device model . . . . . >1.5kV

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	34	6.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . —

Operating Conditions

Supply Voltage (VCC) . . . . . +5V ±5%
Ambient Temperature
EC7401QI . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
	VCC = 5VDC; EN_PWR = 5VDC; R_T = 100kΩ, ISEN1 = ISEN2 = ISEN3 = ISEN4 = -70µA	-	15	20	mA
	VCC = 5VDC; EN_PWR = 0VDC; R_T = 100kΩ	-	10	12	mA
POR Threshold	VCC Rising	4.3	4.5	4.7	V
	VCC Falling	3.7	3.9	4.2	V
EN_PWR Threshold	Nominal Supply	0.850	0.875	0.910	V
	Shutdown Supply	-	130	-	mV
	POWER-ON RESET AND ENABLE				
EN_VTT Threshold	Rising	0.850	0.875	0.910	V
	Hysteresis	-	130	-	mV
	Falling	0.720	0.745	0.775	V
REFERENCE VOLTAGE AND DAC					
System Accuracy of EC7401QI (VID = 1V to 1.6V, **T_J = -40°C to +85°C**)	**(Note 3)**	-0.6	-	0.6	%VID
System Accuracy of EC7401QI (VID = 0.5V to 1V, **T_J = -40°C to +85°C**)	**(Note 3)**	-1	-	1	%VID
VID Pull-up		-60	-40	-20	µA
VID Input Low Level		-	-	0.4	V
VID Input High Level		0.8	-	-	V
VRSEL Input Low Level		-	-	0.4	V
VRSEL Input High Level		0.8	-	-	V
DAC Source Current		-	4	7	mA
DAC Sink Current		-	-	300	µA

Electrical Specifications Operating Conditions: VCC = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
REF Source Current		45	50	55	µA
REF Sink Current		45	50	55	µA
PIN-ADJUSTABLE OFFSET					
Voltage at OFSET Pin of EC7401QI	Offset resistor connected to ground	388	400	412	mV
	Voltage below VCC, offset resistor connected to VCC	1.552	1.600	1.648	V
OSCILLATORS					
Accuracy of Switching Frequency Setting	R_T = 100kΩ	225	250	275	kHz
Adjustment Range of Switching Frequency	**(Note 4)**	0.08	-	1.0	MHz
Soft-Start Ramp Rate	R_S = 100kΩ (Notes 5, 6)	-	1.563	-	mV/µs
Adjustment Range of Soft-start Ramp Rate	**(Note 4)**	0.625	-	6.25	mV/µs
PWM GENERATOR					
Sawtooth Amplitude		-	1.5	-	V
Max Duty Cycle		-	66.7	-	%
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground **(Note 4)**	-	96	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground **(Note 4)**	-	20	-	MHz
Slew Rate	C_L = 100pF	-	9	-	V/µs
Maximum Output Voltage		3.8	4.3	4.9	V
Output High Voltage @ 2mA		3.6	-	-	V
Output Low Voltage @ 2mA		-	-	1.2	V
REMOTE-SENSE AMPLIFIER					
Bandwidth	**(Note 4)**	-	20	-	MHz
Output High Current	VSEN - VGND = 2.5V	-500	-	500	µA
Output High Current	VSEN - VGND = 0.6	-500	-	500	µA
PWM OUTPUT					
PWM Output Voltage LOW Threshold	I_{LOAD} = ±500µA	-	-	0.5	V
PWM Output Voltage HIGH Threshold	I_{LOAD} = ±500µA	4.3	-	-	V
SENSE CURRENT OUTPUT (IDROOP and IOUT)					
Sensed Current Tolerance	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 80µA	76	80	84	µA
Overcurrent Trip Level		90	100	110	µA
Maximum Voltage at IDROOP Pin		-	2	-	V
THERMAL MONITORING AND FAN CONTROL					
TSEN Input Voltage for FAN Trip		1.6	1.65	1.69	V
TSEN Input Voltage for FAN Reset		1.89	1.93	1.98	V
TSEN Input Voltage for HOT Trip		1.35	1.4	1.44	V
TSEN Input Voltage for HOT Reset		1.6	1.65	1.69	V
Leakage Current of FAN	With externally pull-up resistor connected to VCC	-	-	30	µA

Electrical Specifications Operating Conditions: VCC = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FAN Low Voltage	With 1.25k resistor pull-up to VCC, I_{FAN} = 4mA	-	-	0.3	V
Leakage Current of HOT	With externally pull-up resistor connected to VCC	-	-	30	µA
HOT Low Voltage	With 1.25k resistor pull-up to VCC, I_{HOT} = 4mA	-	-	0.3	V
VR READY AND PROTECTION MONITORS					
Leakage Current of POK	With externally pull-up resistor connected to VCC	-	-	30	µA
POK Low Voltage	I_{POK} = 4mA	-	-	0.3	V
Undervoltage Threshold	VDIFF Falling	48	50	52	%VID
POK Reset Voltage	VDIFF Rising	58	60	62	%VID
Overvoltage Protection Threshold	Before valid VID	1.250	1.275	1.300	V
	After valid VID, the voltage above VID	150	175	200	mV
Overvoltage Protection Reset Threshold		0.38	0.40	0.42	V

NOTES:

3. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
4. Limits established by characterization and are not production tested.
5. During soft-start, VDAC rises from 0 to 1.1V first and then ramp to VID voltage after receiving valid VID.
6. Soft-start ramp rate is determined by the adjustable soft-start oscillator frequency at the speed of 6.25mV per cycle.

Functional Pin Description

VCC

Supplies the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply.

GND

Bias and reference ground for the IC. The bottom metal base of EC7401QI is the GND.

EN_PWR

This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN_PWR through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN_PWR is driven above 0.875V, the EC7401QI is active depending on status of EN_VTT, the internal POR, and pending fault states. Driving EN_PWR below 0.745V will clear all fault states and prime the EC7401QI to soft-start when re-enabled.

EN_VTT

This pin is another threshold-sensitive enable input for the controller. It's typically connected to VTT output of VTT voltage regulator in the computer mother board. When EN_VTT is driven above 0.875V, the EC7401QI is active depending on status of ENLL, the internal POR, and pending fault states. Driving EN_VTT below 0.745V will clear all fault states and prime the EC7401QI to soft-start when re-enabled.

FSW

Use this pin to set up the desired switching frequency. A resistor, placed from FSW to ground will set the switching frequency. The relationship between the value of the resistor and the switching frequency will be described by an approximate equation.

SS

Use this pin to set up the desired start-up oscillator frequency. A resistor, placed from SS to ground will set up the soft-start ramp rate. The relationship between the value of the resistor and the soft-start ramp-up time will be described by an approximate equation.

VID7, VID6, VID5, VID4, VID3, VID2, VID1 and VID0

These are the inputs to the internal DAC that generates the reference voltage for output regulation. Connect these pins either to open-drain outputs with or without external pull-up resistors or to active pull-up outputs. All VID pins have 40µA internal pull-up current sources that diminish to zero as the voltage rises above the logic-high level. These inputs can be pulled up externally as high as VCC plus 0.3V.

When an OFF VID code causes shut-down, the controller needs to be reset before it starts again.

VRSEL

Use this pin to select Internal VID code. When it is connected to GND, the extended VR10 code is selected. When it's floated or pulled to high, VR11 code is selected. This input can be pulled up as high as VCC plus 0.3V.

VDIFF, VSEN, and VGND

VSEN and VGND form the precision differential remote-sense amplifier. This amplifier converts the differential voltage of the remote output to a single-ended voltage referenced to local ground. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and VGND to the sense pins of the remote load.

VFB and COMP

Inverting input and output of the error amplifier respectively. VFB can be connected to VDIFF through a resistor. A properly chosen resistor between VDIFF and VFB can set the load line (droop), when IDROOP pin is tied to VFB pin. The droop scale factor is set by the ratio of the ISEN resistors and the inductor DCR or the lower MOSFET R_{DS}(ON). COMP is tied back to VFB through an external RC network to compensate the regulator.

DAC and REF

The DAC pin is the output of the precision internal DAC reference. The REF pin is the positive input of the Error Amplifier. In typical applications, a 1kΩ, 1% resistor is used between DAC and REF to generate a precision offset voltage. This voltage is proportional to

the offset current determined by the offset resistor from OFSET to ground or VCC. A capacitor is used between REF and ground to smooth the voltage transition during VID Voltage Scaling operations.

PWM1, PWM2, PWM3, PWM4

Pulse width modulation outputs. Connect these pins to the PWM input pins of the Altera Enpirion driver IC. The number of active channels is determined by the state of PWM3 and PWM4. Tie PWM3 to VCC to configure for 2-phase operation. Tie PWM4 to VCC to configure for 3-phase operation.

ISEN1+, ISEN1-; ISEN2+, ISEN2-; ISEN3+, ISEN3-; ISEN4+ and ISEN4

The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers. The sensed current is used for channel current balancing, overcurrent protection, and droop regulation. Inactive channels should have their respective current sense inputs left open (for example, open ISEN4+ and ISEN4- for 3-phase operation).

For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor through a resistor, R_{ISEN}. The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sense current is proportional to the inductor current and scaled by the DCR of the inductor and R_{ISEN}.

When configured for $R_{DS}(ON)$ current sensing, the ISEN1-, ISEN2-, ISEN3-, and ISEN4- pins are grounded at the lower MOSFET sources. The ISEN1+, ISEN2+, ISEN3+, and ISEN4+ pins are then held at a virtual ground. Therefore, a resistor, connected between these current sense pins and the drain terminals of the associated lower MOSFET, will carry the current proportional to the current flowing through that channel. The sensed current is determined by the negative voltage across the lower MOSFET when it is ON, which is the channel current scaled by $R_{DS}(ON)$ and R_{ISEN}.

POK

POK indicates that the soft-start is completed and the output voltage is within the regulated range around VID setting. It is an open-drain logic output. When OCP or OVP occurs, POK will be pulled to low. It will also be pulled low if the output voltage is below the undervoltage threshold.

OFSET

The OFSET pin provides a means to program a DC offset current for generating a DC offset voltage at the REF input. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFSET pin should be left unterminated.

TCOMP

Temperature compensation scaling input. The voltage sensed on the TSEN pin is utilized as the temperature input to adjust ldroop and the overcurrent protection limit to effectively compensate for the temperature coefficient of the current sense element. To implement the integrated temperature compensation, a resistor divider circuit is needed with one resistor being connected from TCOMP to VCC of the controller and another resistor being connected from TCOMP to GND. Changing the ratio of the resistor values will set the gain of the integrated thermal compensation. When integrated temperature compensation function is not used, connect TCOMP to GND.

IDROOP

IDROOP is the output pin of sensed average channel current which is proportional to load current. In the application which does not require loadline, leave this pin open. In the application which requires load line, connect this pin to VFB so that the sensed average current will flow through the resistor between VFB and VDIFF to create a voltage drop which is proportional to load current.

TSEN

TSEN is an input pin for VR temperature measurement. Connect this pin through NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is reverse proportional to VR temperature. EC7401QI monitors the VR temperature based on the voltage at TSEN pin and outputs HOT and FAN signals.

HOT

HOT is used as an indication of high VR temperature. It is an open-drain logic output. It will be open when the measured VR temperature reaches a certain level.

FAN

FAN is an output pin with open-drain logic output. It will be open when the measured VR temperature reaches a certain level.

Operation

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multiphase. The EC7401QI controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagram on page 4 provides top level views of multiphase power conversion using the EC7401QI controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

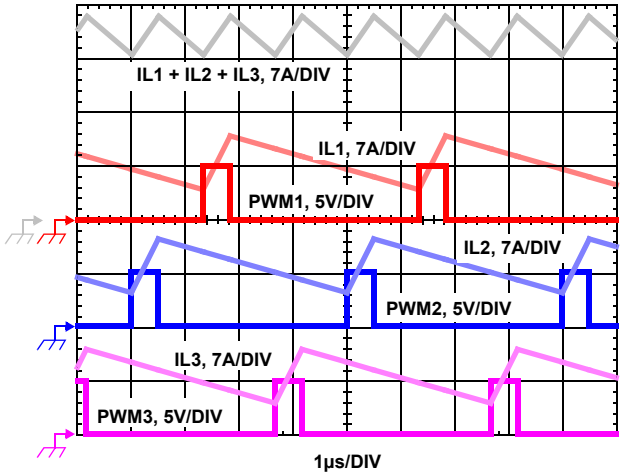


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1 which represents an individual channel's peak-to-peak inductor current.

$$I_{P\text{-}P} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{Lf_{SW}V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_{SW} is the switching frequency.

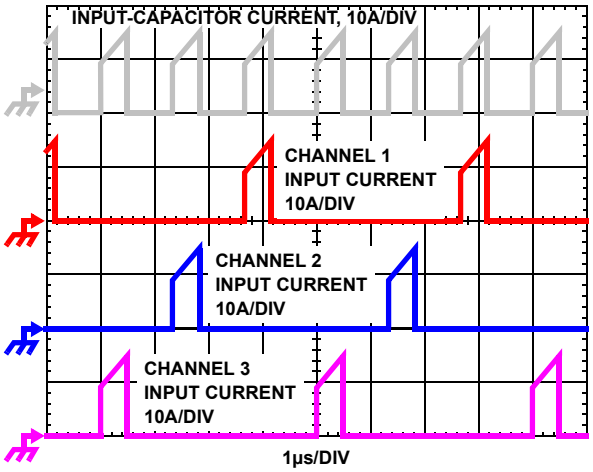


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR THREE-PHASE CONVERTER

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,P\text{-}P} = \frac{(V_{IN} - N\,V_{OUT})\,V_{OUT}}{L\,f_{SW}\,V_{IN}} \qquad \textbf{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a 3-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent 3-phase converter.

Figures 21, 22 and 23 in the section entitled “Input Capacitor Selection” on page 41, can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 23 shows the single-phase input-capacitor RMS current for comparison.

PWM Operation

The timing of each channel is set by the number of active channels. The default channel setting for the EC7401QI is four. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The pulse termination signal is an internally generated clock signal which triggers the falling edge of PWM signal. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FSW pin and ground. Each cycle begins when the clock signal commands the channel PWM signal to go low. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

For 4-channel operation, the channel firing order is 4-3-2-1: PWM3 pulse terminates 1/4 of a cycle after PWM4, PWM2 output follows another 1/4 of a cycle after PWM3, and PWM1 terminates another 1/4 of a cycle after PWM2. For 3-channel operation, the channel firing order is 3-2-1.

Connecting PWM4 to VCC selects three channel operation and the pulse-termination times are spaced in 1/3 cycle increments. If PWM3 is connected to VCC, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle later.

Once a PWM signal transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction

signal relative to the sawtooth ramp as illustrated in Figure 7. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Current Sampling

During the forced off-time following a PWM transition low, the associated channel current sense amplifier uses the I_{SEN} inputs to reproduce a signal proportional to the inductor current (I_L). This current gets sampled starting 1/6 period after each PWM goes low and continuously gets sampled for 1/3 period, or until the PWM goes high, whichever comes first. No matter the current sense method, the sense current (I_{SEN}) is simply a scaled version of the inductor current. Coincident with the falling edge of the PWM signal, the sample and hold circuitry samples the sensed current signal (I_{SEN}) as illustrated in Figure 3.

Therefore, the sample current (I_n) is proportional to the output current and held for one switching cycle. The sample current is used for current balance, load-line regulation, and overcurrent protection.

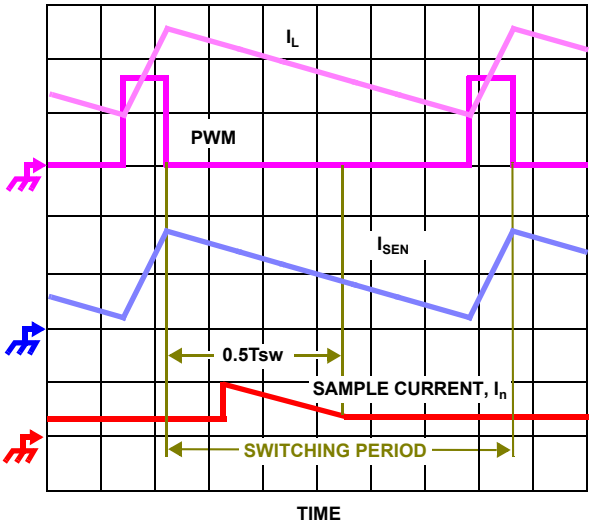


FIGURE 3. SAMPLE AND HOLD TIMING

Current Sensing

The EC7401QI supports inductor DCR sensing, MOSFET $R_{DS}(ON)$ sensing, or resistive sensing techniques. The internal circuitry, shown in Figures 4, 5, and 6, represents one channel of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PWM3 and PWM4 pins, as described in “PWM Operation” on page 12.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 4. The channel current (I_L) flowing through the inductor, will also pass through the DCR. Equation 3 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad \textbf{(EQ. 3)}$$

A simple RC network across the inductor extracts the DCR voltage, as shown in Figure 4.

The voltage on the capacitor (V_C) can be shown to be proportional to the channel current (I_L) see Equation 4.

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \textbf{(EQ. 4)}$$

If the RC network components are selected such that the RC time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor (V_C) is equal to the voltage drop across the DCR (i.e., proportional to the channel current).

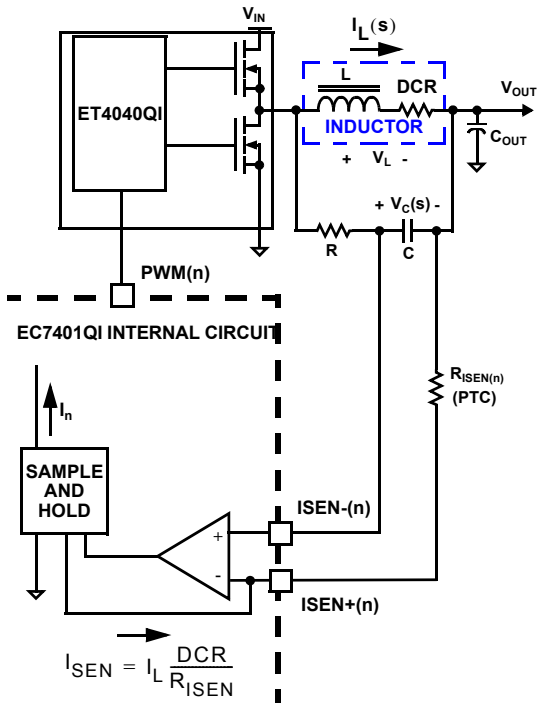


FIGURE 4. DCR SENSING CONFIGURATION

With the internal low-offset current amplifier, the capacitor voltage (V_C) is replicated across the sense resistor (R_{ISEN}). Therefore the current out of ISEN+ pin (I_{SEN}) is proportional to the inductor current.

Equation 5 shows that the ratio of the channel current to the sensed current (I_{SEN}) is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \textbf{(EQ. 5)}$$

RESISTIVE SENSING

For accurate current sense, a dedicated current-sense resistor (R_{SENSE}) in series with each output inductor can serve as the current sense element (see Figure 5). This technique is more accurate, but reduces overall converter efficiency due to the additional power loss on the current sense element (R_{SENSE}).

Equation 6 shows the ratio of the channel current to the sensed current (I_{SEN}).

$$I_{SEN} = I_L \cdot \frac{R_{SENSE}}{R_{ISEN}} \quad \text{(EQ. 6)}$$

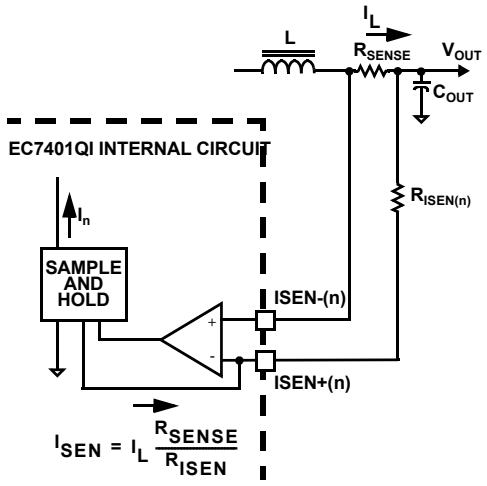


FIGURE 5. SENSE RESISTOR IN SERIES WITH INDUCTORS

MOSFET R_{DS}(ON) SENSING

The controller can also sense the channel load current by sampling the voltage across the lower MOSFET R_{DS}(ON) (see Figure 6). The amplifier is ground-reference by connecting the ISEN- pin to the source of the lower MOSFET. ISEN+ pin is connected to the PHASE node through the current sense resistor (R_{ISEN}). The voltage across R_{ISEN} is equivalent to the voltage drop across the R_{DS}(ON) of the lower MOSFET while it is conducting. The resulting current out of the ISEN+ pin is proportional to the channel current I_L.

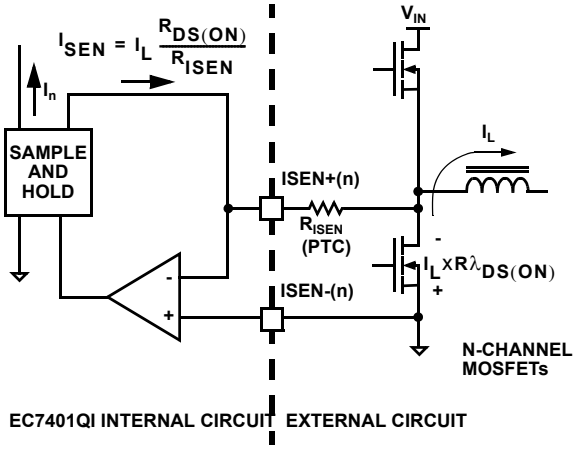


FIGURE 6. MOSFET R_{DS}(ON) CURRENT-SENSING CIRCUIT

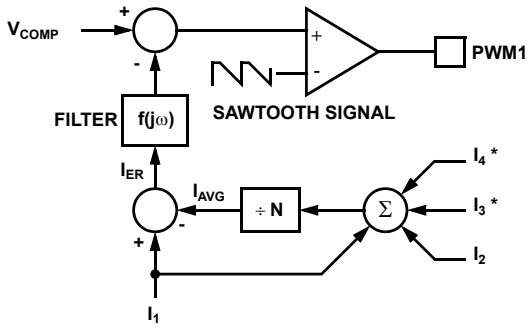
Equation 7 shows the ratio of the channel current to the sensed current I_{SEN}.

$$I_{SEN} = I_L \frac{R_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 7)}$$

Both inductor DCR and MOSFET R_{DS}(ON) value will increase as the temperature increases. Therefore the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Positive Temperature Coefficient (PTC) resistor can be selected for the sense resistor (R_{ISEN}), or the integrated temperature compensation function of EC7401QI should be utilized. The integrated temperature compensation function is described in “Temperature Compensation” on page 33.

Channel-Current Balance

The sensed current (I_N) from each active channel are summed together and divided by the number of active channels. The resulting average current (I_{AVG}) provides a measure of the total load current. Channel current balance is achieved by comparing the sampled current of each channel to the average current to make an appropriate adjustment to the WPM duty cycle of each channel. The current-balance method is illustrated in Figure 7. In the figure, the average current combines with the Channel 1 current (I_1) to create an error signal (I_{ER}). The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: *Channels 3 and 4 are optional for 2 or 3 phase designs.

FIGURE 7. CHANNEL 1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

Voltage Regulation

The compensation network shown in Figure 8 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFSET current source, remote-sense and error amplifiers. Altera specifies the guaranteed tolerance of the EC7401QI to include the combined tolerances of each of these elements.

The output of the error amplifier (V_{COMP}) is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the MOSFET drivers and regulate the converter output to the specified reference voltage. The internal and external circuitry, which control voltage regulation, are illustrated in Figure 8.

The EC7401QI incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, V_{SEN}, and inverting input, VGND, of the remote-sense amplifier. The remote-sense output (V_{DIF}), is connected to the inverting input of the error amplifier through an external resistor.

A digital-to-analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID7 through VID0. The DAC decodes the 8 6-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 45µA pull-up to an internal 2.5V source for use with open-drain outputs. The pull-up current diminishes to zero above the logic threshold to protect voltage-sensitive output devices. External pull-up resistors can augment the pull-up current sources if case leakage into the driving device is greater than 45µA.

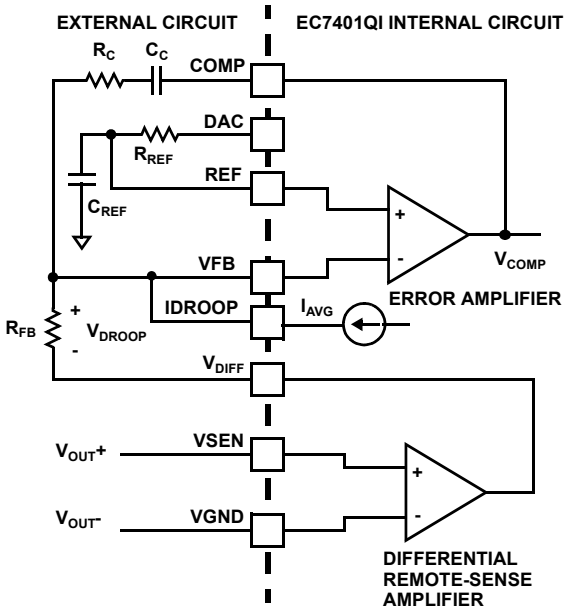


FIGURE 8. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION) (Continued)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION) (Continued)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION) (Continued)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

TABLE 2. VR11 VID 8 BIT

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Load-Line Regulation

Some microprocessor manufacturers require a precisely-controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 8, a current proportional to the average current of all active channels (I_{AVG}) flows from VFB through a load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as Equation 8:

$$V_{DROOP} = I_{AVG} R_{FB} \quad \textbf{(EQ. 8)}$$

The regulated output voltage is reduced by the droop voltage (V_{DROOP}). The output voltage as a function of load current is derived by combining Equation 8 with the appropriate sample current expression defined by the current sense method employed.

$$V_{OUT} = V_{REF} - V_{OFSET} - \left(\frac{I_{OUT}}{N} \frac{R_X}{R_{ISEN}} R_{FB} \right) \quad \textbf{(EQ. 9)}$$

Where V_{REF} is the reference voltage, V_{OFSET} is the programmed offset voltage, I_{OUT} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback resistor, N is the active channel number, and R_X is the DCR, $R_{DS}(ON)$, or R_{SENSE} depending on the sensing method.

Therefore the equivalent loadline impedance, i.e. Droop impedance, is equal to Equation 10:

$$R_{LL} = \frac{R_{FB}}{N} \frac{R_X}{R_{ISEN}} \quad \textbf{(EQ. 10)}$$

Output-Voltage Offset Programming

The EC7401QI allows the designer to accurately adjust the offset voltage. When a resistor (R_{OFSET}) is connected between OFSET to VCC, the voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFSET}) to flow into OFSET. If R_{OFSET} is connected to ground, the voltage across it is regulated to 0.4V, and I_{OFSET} flows out of OFSET. A resistor between DAC and REF (R_{REF}) is selected so that the product (I_{OFSET} x R_{OFSET}) is equal to the desired offset voltage. These functions are shown in Figure 9.

Once the desired output offset voltage has been determined, use Equations 11 and 12 to set R_{OFSET}:

For Positive Offset (connect R_{OFSET} to VCC):

$$R_{OFSET} = \frac{1.6 \times R_{REF}}{V_{OFFSET}} \quad \textbf{(EQ. 11)}$$

For Negative Offset (connect R_{OFSET} to GND):

$$R_{OFSET} = \frac{0.4 \times R_{REF}}{V_{OFFSET}} \quad \textbf{(EQ. 12)}$$

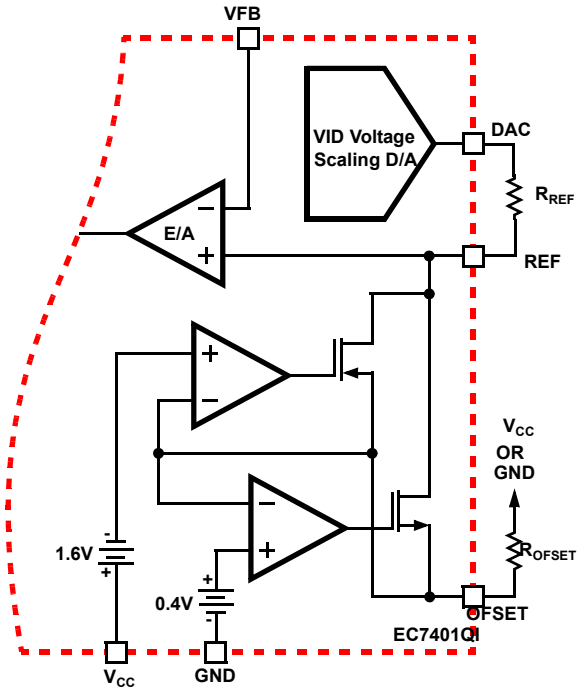


FIGURE 9. OUTPUT VOLTAGE OFFSET PROGRAMMING

VID Voltage Scaling

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs during regulator operation. The power management solution is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption is a necessary function of the core-voltage regulator.

The EC7401QI checks the VID inputs six times every switching cycle. If the VID code is found to have been changed, the controller waits for half of a switching cycle before executing a 6.25mV step change. If the difference between DAC level and the new VID code changes during the half-cycle waiting period, no change to the DAC output is made. If the VID code is more than 1 bit higher or lower than the DAC (not recommended), the controller will execute 6.26mV step change six times per cycle until VID and DAC are equal. Therefore it is important to carefully control the rate of VID stepping in 1-bit increments.

In order to ensure the smooth transition of output voltage during VID change, a VID step change smoothing network, composed of R_{REF} and C_{REF}, can be used. The selection of R_{REF} is based on the desired offset voltage as detailed in “Output-Voltage Offset Programming” on page 27. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1-bit every T_{VID}, the relationship between the time constant of R_{REF} and C_{REF} network and T_{VID} is given by Equation 13.

$$C_{REF} R_{REF} = T_{VID} \quad \text{(EQ. 13)}$$

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and VCC. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, POK asserts logic high.

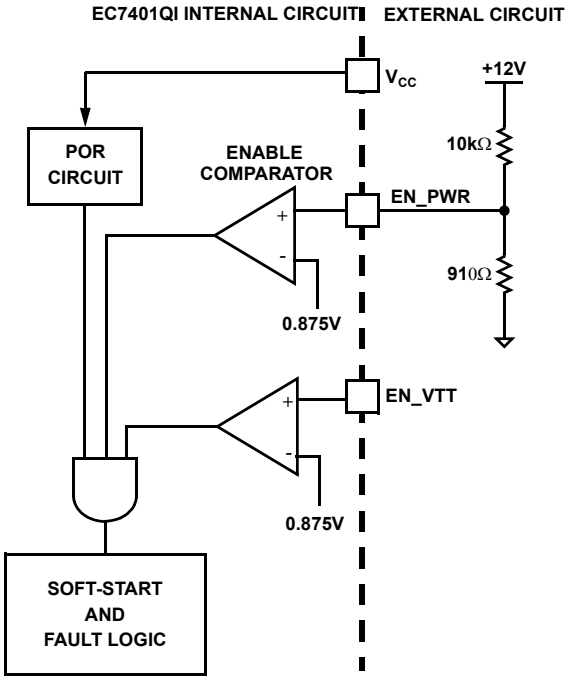


FIGURE 10. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met before the EC7401QI is released from shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the EC7401QI is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the EC7401QI will not inadvertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 6).
2. The EC7401QI features an enable input (EN_PWR) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the EC7401QI in shutdown until the voltage at EN_PWR rises above 0.875V. The enable comparator has about 130mV of hysteresis to prevent bounce. It is important that the driver ICs reach their POR level before the EC7401QI becomes enabled. The schematic in Figure 10 demonstrates sequencing the EC7401QI with the ISL66xx family of MOSFET drivers, which require 12V bias.
3. The voltage on EN_VTT must be higher than 0.875V to enable the controller. This pin is typically connected to the output of VTT VR.

When all conditions above are satisfied, EC7401QI begins the soft-start and ramps the output voltage to 1.1V first. After remaining at 1.1V for some time, EC7401QI reads the VID code at VID input pins. If the VID code is valid, EC7401QI will regulate the output to the final VID setting. If the VID code is OFF code, EC7401QI will shut down, and cycling VCC, EN_PWR or EN_VTT is needed to restart.

Soft-Start

EC7401QI based VR has 4 periods during soft-start as shown in Figure 11. After VCC, EN_VTT and EN_PWR reach their POR/enable thresholds, The controller will have fixed delay period TD1. After this delay period, the VR will begin first soft-start

ramp until the output voltage reaches 1.1V V_{BOOT} voltage. Then, the controller will regulate the VR voltage at 1.1V for another fixed period TD3. At the end of TD3 period, EC7401QI reads the VID signals. If the VID code is valid, EC7401QI will initiate the second soft-start ramp until the voltage reaches the VID voltage minus offset voltage.

The soft-start time is the sum of the 4 periods as shown in Equation 14.

$$T_{SS} = TD1 + TD2 + TD3 + TD4 \quad \textbf{(EQ. 14)}$$

TD1 is a fixed delay with the typical value as 1.36ms. TD3 is determined by the fixed 85µs plus the time to obtain valid VID voltage. If the VID is valid before the output reaches the 1.1V, the minimum time to validate the VID input is 500ns. Therefore the minimum TD3 is about 86µs.

During TD2 and TD4, EC7401QI digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor R_{ss} from SS pin to GND. The second soft-start ramp time TD2 and TD4 can be calculated based on Equations 15 and 16:

$$TD2 = \frac{1.1xR_{SS}}{6.25x25}(\mu s) \quad \textbf{(EQ. 15)}$$

$$TD4 = \frac{(V_{VID} - 1.1)xR_{SS}}{6.25x25}(\mu s) \quad \textbf{(EQ. 16)}$$

For example, when VID is set to 1.5V and the Rss is set at 100kΩ, the first soft-start ramp time TD2 will be 704µs and the second soft-start ramp time TD4 will be 256µs.

After the DAC voltage reaches the final VID setting, POK will be set to high with the fixed delay TD5. The typical value for TD5 is 85µs.

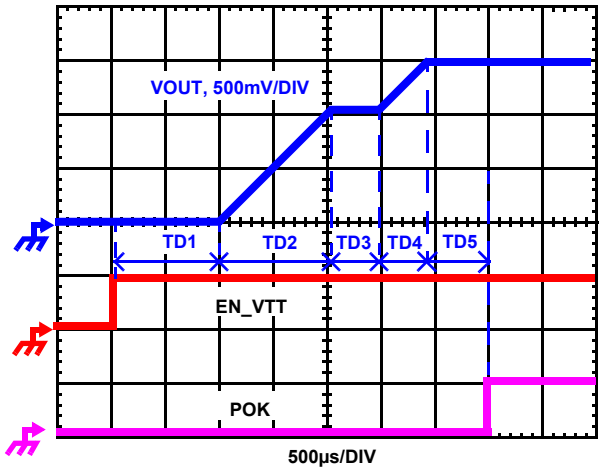


FIGURE 11. SOFT-START WAVEFORMS

Fault Monitoring and Protection

The EC7401QI actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 12 outlines the interaction between the fault monitors and the POK signal.

POK Signal

The POK pin is an open-drain logic output to indicate that the soft-start period is completed and the output voltage is within the regulated range. POK is pulled low during shutdown and releases high after a successful soft-start and a fixed delay TD5. POK will be pulled low when an undervoltage or overvoltage condition is detected, or the controller is disabled by a reset from EN_PWR, EN_VTT, POR, or VID OFF-code.

Undervoltage Detection

The undervoltage threshold is set at 50% of the VID code. When the output voltage at V_{SEN} is below the undervoltage threshold, POK is pulled low.

Overvoltage Protection

Regardless of the VR being enabled or not, the EC7401QI overvoltage protection (OVP) circuit will be active after its POR. The OVP thresholds are different under different operation conditions. When VR is not enabled and before the second soft-start, the OVP threshold is 1.275V. Once the controller detects valid VID input, the OVP trip point will be changed to VID plus 175mV.

Two actions are taken by the EC7401QI to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low instantly (less than 20ns) until the voltage at VDIFF falls below 0.4V. This causes the drivers to turn on the lower MOSFETs and pull the output voltage below a level that might cause damage to the load. The PWM outputs remain low until VDIFF falls below 0.4V, and then PWM signals enter a high-impedance state. The drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, the EC7401QI will again command the lower MOSFETs to turn on. The EC7401QI will continue to protect the load in this fashion as long as the overvoltage condition occurs.

Once an overvoltage condition is detected, normal PWM operation ceases until the EC7401QI is reset. Cycling the voltage on EN_PWR, EN_VTT or VCC below the POR-falling threshold will reset the controller. Cycling the VID codes will not reset the controller.

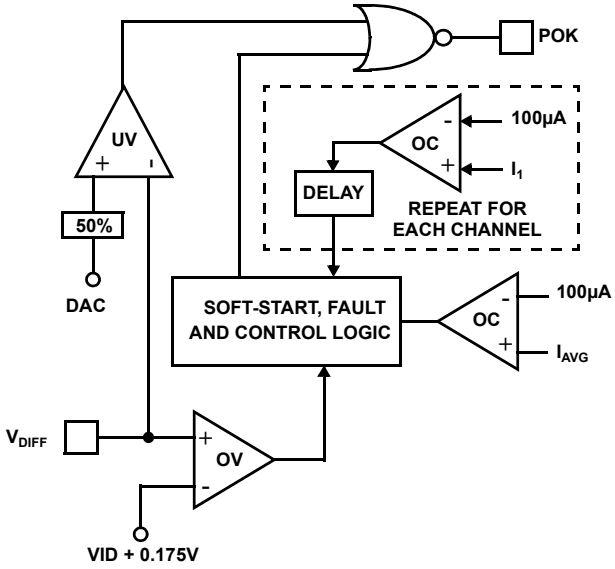


FIGURE 12. POK AND PROTECTION CIRCUITRY

Overcurrent Protection

EC7401QI has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition on a delayed basis, while the combined phase currents are protected on an instantaneous basis.

In instantaneous protection mode, the EC7401QI utilizes the sensed average current I_{AVG} to detect an overcurrent condition. See “Channel-Current Balance” on page 16 for more detail on how the average current is measured. The average current is continually compared with a constant 100µA reference current as shown in Figure 12. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown.

In individual overcurrent protection mode, the EC7401QI continuously compares the current of each channel with the same 100µA reference current. If any channel current exceeds the reference current continuously for eight consecutive cycles, the comparator triggers the converter to shutdown.

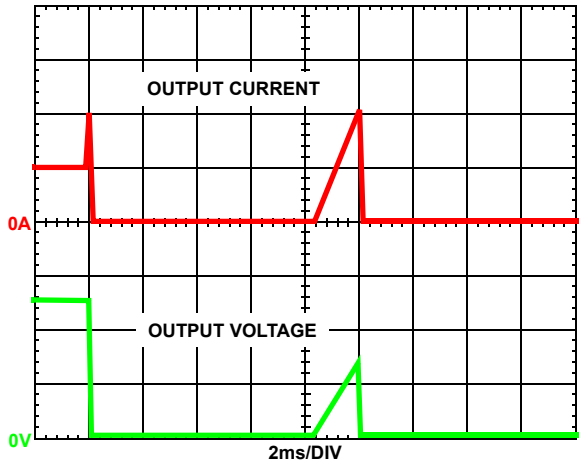


FIGURE 13. OVERCURRENT BEHAVIOR IN HICCUP MODE. F_{SW} = 500kHz

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state within 20ns commanding the MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will continue indefinitely (as shown in Figure 13) until either controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard during this kind of operation.

Thermal Monitoring (HOT/FAN)

There are two thermal signals to indicate the temperature status of the voltage regulator: HOT and FAN. Both FAN and HOT are open-drain outputs, and external pull-up resistors are required.

FAN signal indicates that the temperature of the voltage regulator is high and more cooling airflow is needed. HOT signal can be used to inform the system that the temperature of the voltage regulator is too high and the CPU should reduce its power consumption. HOT signal may be tied to the CPU's PROC_HOT signal.

The diagram of thermal monitoring function block is shown in Figure 14. One NTC resistor should be placed close to the power stage of the voltage regulator to sense the operational temperature, and one pull-up resistor is needed to form the voltage divider for TSEN pin. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at TSEN pin. Figure 15 shows the TSEN voltage over the temperature for a typical design with a recommended 6.8kΩ NTC (P/N: NTHS0805N02N6801 from Vishay) and 1kΩ resistor R_{TSEN1}. We recommend using those resistors for the accurate temperature compensation.

There are two comparators with hysteresis to compare the TSEN pin voltage to the fixed thresholds for FAN and HOT signals respectively. FAN signal is set to high when TSEN voltage is lower than 33% of VCC voltage, and is pulled to GND when TSEN voltage increases to above 39% of VCC voltage. FAN is set to high when TSEN voltage goes below 28% of VCC voltage, and is pulled to GND when TSEN voltage goes back to above 33% of VCC voltage. Figure 16 shows the operation of those signals.

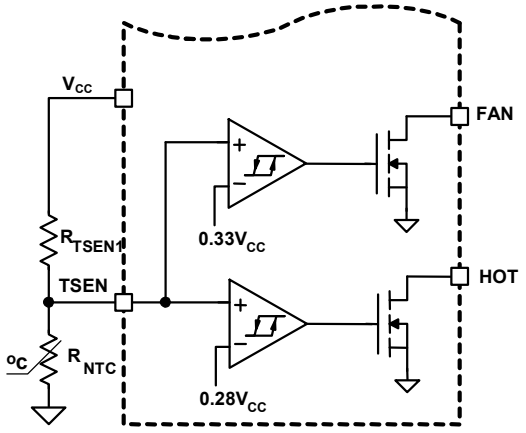


FIGURE 14. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

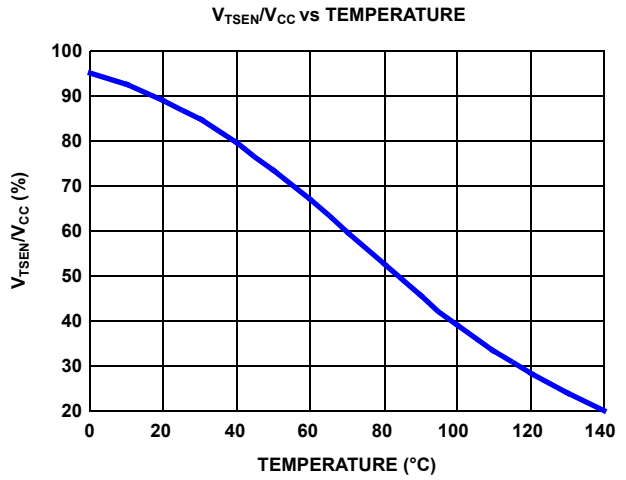


FIGURE 15. THE RATIO OF TSEN VOLTAGE TO NTC TEMPERATURE WITH RECOMMENDED PARTS

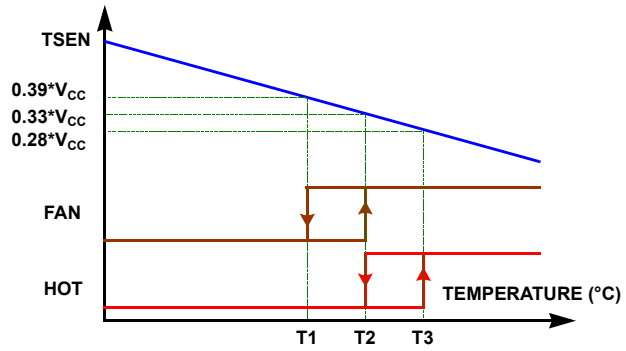


FIGURE 16. HOT AND FAN SIGNAL vs TSEN VOLTAGE

Based on the NTC temperature characteristics and the desired threshold of HOT signal, the pull-up resistor R_{TSEN1} of TSEN pin is given by:

$$R_{TSEN1} = 2.75 \times R_{NTC(T3)} \quad \text{(EQ. 17)}$$

$R_{NTC(T3)}$ is the NTC resistance at the HOT threshold temperature T3.

The NTC resistance at the set point T2 and release point T1 of FAN signal can be calculated as:

$$R_{NTC(T2)} = 1.267 \times R_{NTC(T3)} \quad \text{(EQ. 18)}$$

$$R_{NTC(T1)} = 1.644 \times R_{NTC(T3)} \quad \text{(EQ. 19)}$$

With the NTC resistance value obtained from Equations 18 and 19, the temperature value T2 and T1 can be found from the NTC datasheet.

Temperature Compensation

EC7401QI supports inductor DCR sensing, MOSFET $R_{DS}(ON)$ sensing, or resistive sensing techniques. Both inductor DCR and MOSFET $R_{DS}(ON)$ have the positive temperature coefficient, which is about +0.38%/°C. Because the voltage across inductor or MOSFET is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR or MOSFET $R_{DS}(ON)$.

In order to obtain the correct current information, there should be a way to correct the temperature impact on the current sense component. EC7401QI provides two methods: integrated temperature compensation and external temperature compensation.

Integrated Temperature Compensation

When TCOMP voltage is equal or greater than VCC/15, EC7401QI will utilize the voltage at TSEN and TCOMP pins to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 17.

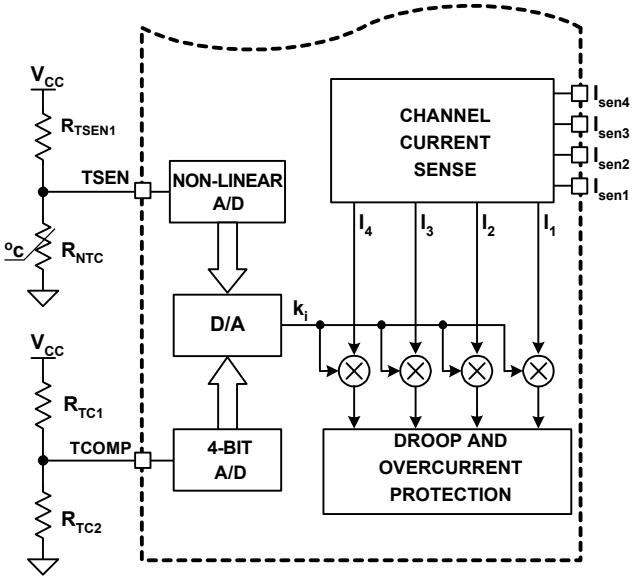


FIGURE 17. BLOCK DIAGRAM OF INTEGRATED TEMPERATURE COMPENSATION

When the TSEN NTC is placed close to the current sense component (inductor or MOSFET), the temperature of the NTC will track the temperature of the current sense component. Therefore the TSEN voltage can be utilized to obtain the temperature of the current sense component.

Based on VCC voltage, EC7401QI converts the TSEN pin voltage to a 6-bit TSEN digital signal for temperature compensation. With the non-linear A/D converter of EC7401QI, TSEN digital signal is linearly proportional to the NTC temperature. For accurate temperature compensation, the ratio of the TSEN voltage to the NTC temperature of the practical design should be similar to that in Figure 15.

Depending on the location of the NTC and the airflow, the NTC may be cooler or hotter than the current sense component. TCOMP pin voltage can be utilized to correct the temperature difference between NTC and the current sense component. When a different NTC type or different voltage divider is used for the TSEN function, TCOMP voltage can also be used to compensate for the difference between the recommended TSEN voltage curve in Figure 16 and that of the actual design. According to the VCC voltage, EC7401QI converts the TCOMP pin voltage to a 4-bit TCOMP digital signal as TCOMP factor N.

TCOMP factor N is an integer between 0 and 15. The integrated temperature compensation function is disabled for N = 0. For N = 4, the NTC temperature is equal to the temperature of the current sense component. For N < 4, the NTC is hotter than the current sense component. The NTC is cooler than the current sense component for N > 4. When N > 4, the larger TCOMP factor N, the larger the difference between the NTC temperature and the temperature of the current sense component.

EC7401QI multiplexes the TCOMP factor N with the TSEN digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated channel current signal is used for droop and overcurrent protection functions.

Design Procedure

1. Properly choose the voltage divider for TSEN pin to match the TSEN voltage V_S temperature curve with the recommended curve in Figure 15.
2. Run the actual board under the full load and the desired cooling condition.
3. After the board reaches the thermal steady state, record the temperature (T_{CSC}) of the current sense component (inductor or MOSFET) and the voltage at TSEN and VCC pins.
4. Use Equation 20 to calculate the resistance of the TSEN NTC, and find out the corresponding NTC temperature T_{NTC} from the NTC datasheet.

$$R_{NTC(T_{NTC})} = \frac{V_{TSEN} \times R_{TSEN1}}{V_{CC} - V_{TSEN}} \quad \textbf{(EQ. 20)}$$

5. Use Equation 21 to calculate the TCOMP factor N:

$$N = \frac{209x(T_{CSC} - T_{NTC})}{3xT_{NTC} + 400} + 4 \quad \textbf{(EQ. 21)}$$

6. Choose an integral number close to the above result for the TCOMP factor. If this factor is higher than 15, use N = 15. If it is less than 1, use N = 1.
7. Choose the pull-up resistor R_{TC1} (typical 10kΩ).
8. If N = 15, do not need the pull-down resistor R_{TC2}, otherwise obtain R_{TC2} by Equation 22:

$$R_{TC2} = \frac{NxR_{TC1}}{15 - N} \quad \textbf{(EQ. 22)}$$

9. Run the actual board under full load again with the proper resistors connected to the TCOMP pin.
10. Record the output voltage as V1 immediately after the output voltage is stable with the full load. Record the output voltage as V2 after the VR reaches the thermal steady state.
11. If the output voltage increases over 2mV as the temperature increases, i.e. V2 - V1 > 2mV, reduce N and redesign R_{TC2}; if the output voltage decreases over 2mV as the temperature increases, i.e. V1 - V2 > 2mV, increase N and redesign R_{TC2}.

The design spreadsheet is available for those calculations.

External Temperature Compensation

By setting the voltage of TCOMP pin to 0, the integrated temperature compensation function is disabled. And one external temperature compensation network, shown in Figure 18, can be used to cancel the temperature impact on the droop (i.e. load line).

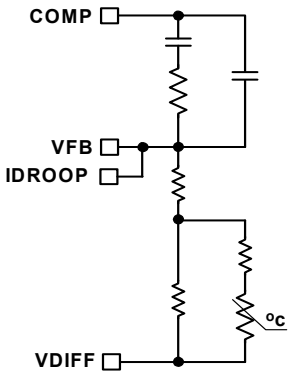


FIGURE 18. VOLTAGE AT IDROOP PIN WITH A RESISTOR PLACED FROM IDROOP PIN TO GND WHEN LOAD CURRENT CHANGES

The sensed current will flow out of IDROOP pin and develop the droop voltage across the resistor equivalent (R_{FB}) between VFB and VDIFF pins. If R_{FB} resistance reduces as the temperature increases, the temperature impact on the droop can be compensated. An NTC resistor can be placed close to the power stage and used to form R_{FB}. Due to the non-linear temperature characteristics of the NTC, a resistor network is needed to make the equivalent resistance between VFB and VDIFF pin is reverse proportional to the temperature.

The external temperature compensation network can only compensate the temperature impact on the droop, while it has no impact to the sensed current inside EC7401QI. Therefore this network cannot compensate for the temperature impact on the overcurrent protection function.

Current Sense Output

The current from IDROOP pin is the sensed average current inside EC7401QI. In typical application, IDROOP pin is connected to VFB pin for the application where load line is required. When load line function is not needed, IDROOP pin can used to obtain the load current information: with one resistor from IDROOP pin to GND, the voltage at IDROOP pin will be proportional to the load current. The resistor from IDROOP to GND should be chosen to ensure that the voltage at IDROOP pin is less than 2V under the maximum load current.

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power-supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 20A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($R_{DS}(ON)$). In Equation 23, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor current (see Equation 1); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = R_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2(1-d) + \frac{I_{L,P\text{-}P}^2(1-d)}{12}\right] \quad \textbf{(EQ. 23)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_{SW}; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} f_{SW}\left[\left(\frac{I_M}{N} + \frac{I_{P\text{-}P}}{2}\right)t_{d1} + \left(\frac{I_M}{N} - \frac{I_{P\text{-}P}}{2}\right)t_{d2}\right] \quad \textbf{(EQ. 24)}$$

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $R_{DS}(ON)$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge (Q_{rr}) and the upper MOSFET $R_{DS}(ON)$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 25, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{P\text{-}P}}{2}\right)\left(\frac{t_1}{2}\right)f_{SW} \quad \textbf{(EQ. 25)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 26, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{P\text{-}P}}{2}\right)\left(\frac{t_2}{2}\right)f_{SW} \quad \textbf{(EQ. 26)}$$

A third component involves the lower MOSFET's reverse-recovery charge (Q_{rr}). Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across V_{IN}. The power dissipated as a result is $P_{UP,3}$ and is approximately

$$P_{UP,3} = V_{IN} Q_{rr} f_{SW} \quad \textbf{(EQ. 27)}$$

Finally, the resistive part of the upper MOSFET's is given in Equation 28 as $P_{UP,4}$.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 25, 26, and 27. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

$$P_{UP,4} \approx r_{DS(ON)} \left[\left(\frac{I_M}{N} \right)^2 d + \frac{I_{P\text{-}P}^2}{12} d \right] \quad \textbf{(EQ. 28)}$$

Current Sensing Resistor

The resistors connected between these pins and the respective phase nodes determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point. Select values for these resistors based on the room temperature $R_{DS}(ON)$ of the lower MOSFETs, DCR of inductor or additional resistor; the full-load operating current, I_{FL}; and the number of phases, N using Equation 29.

$$R_{ISEN} = \frac{R_X}{70 \times 10^{-6}} \frac{I_{FL}}{N} \quad \textbf{(EQ. 29)}$$

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistor. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of R_{ISEN} for the affected phases (see the section entitled "Channel-Current Balance" on page 16). Choose R_{ISEN2} in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad \textbf{(EQ. 30)}$$

In Equation 30, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 30 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labelled R_{FB} in Figure 8. Its value depends on the desired full load droop voltage (V_{DROOP} in Figure 8). If Equation 29 is used to select each ISEN resistor, the load-line regulation resistor is as shown in Equation 31.

$$R_{FB} = \frac{V_{DROOP}}{70 \times 10^{-6}} \quad \textbf{(EQ. 31)}$$

If one or more of the ISEN resistors is adjusted for thermal balance, as in Equation 30, the load-line regulation resistor should be selected according to Equation 32 where I_{FL} is the full-load operating current and $R_{ISEN(n)}$ is the ISEN resistor connected to the n^{th} ISEN pin.

$$R_{FB} = \frac{V_{DROOP}}{I_{FL} r_{DS(ON)}} \sum_n R_{ISEN(n)} \quad \textbf{(EQ. 32)}$$

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in Load-Line Regulation, there are two distinct methods for achieving these goals.

COMPENSATING LOAD-LINE REGULATED CONVERTER

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter LC resonant frequency split with the introduction of current information into the control loop. The final location of

these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator by compensating the LC poles and the ESR zero of the voltage-mode approximation yields a solution that is always stable with very close to ideal transient performance.

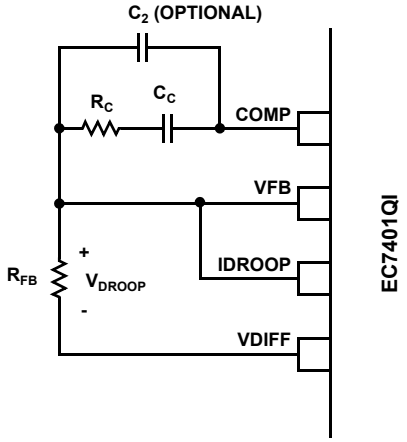


FIGURE 19. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED EC7401QI CIRCUIT

The feedback resistor, R_{FB}, has already been chosen as outlined in "Load-Line Regulation Resistor" on page 37. Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the LC pole frequency and the ESR zero frequency. For each of the three cases which follow, there is a separate set of equations for the compensation components.

Case 1:

$$\frac{1}{2\pi\sqrt{LC}} > f_0$$

$$R_C = R_{FB}\frac{2\pi f_0 V_{P\text{-}P}\sqrt{LC}}{0.75V_{IN}}$$

$$C_C = \frac{0.75V_{IN}}{2\pi V_{P\text{-}P}R_{FB}f_0}$$

Case 2:

$$\frac{1}{2\pi\sqrt{LC}} \le f_0 < \frac{1}{2\pi C(ESR)}$$

$$R_C = R_{FB}\frac{V_{P\text{-}P}(2\pi)^2 f_0^2 LC}{0.75\,V_{IN}} \qquad \textbf{(EQ. 33)}$$

$$C_C = \frac{0.75V_{IN}}{(2\pi)^2 f_0^2 V_{P\text{-}P}R_{FB}\sqrt{LC}}$$

Case 3:

$$f_0 > \frac{1}{2\pi C(ESR)}$$

$$R_C = R_{FB}\frac{2\pi f_0 V_{P\text{-}P}L}{0.75\,V_{IN}(ESR)}$$

$$C_C = \frac{0.75V_{IN}(ESR)\sqrt{C}}{2\pi V_{P\text{-}P}R_{FB}f_0\sqrt{L}}$$

In Equation 33, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 7 and "Electrical Specifications" on page 6.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 20). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading-edge jitter problem is noted.

Once selected, the compensation values in Equation 33 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equation 33 unless some performance issue is noted.

COMPENSATION WITHOUT LOAD-LINE REGULATION

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the LC resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 20, provides the necessary compensation.

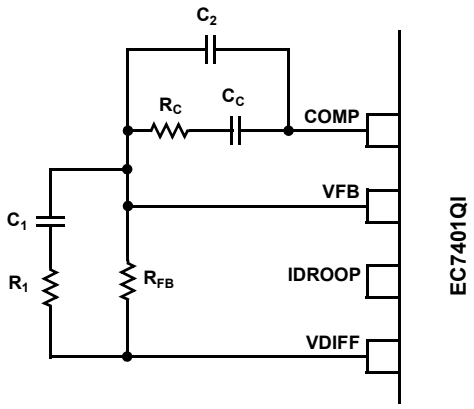


FIGURE 20. COMPENSATION CIRCUIT FOR EC7401QI BASED CONVERTER WITHOUT LOAD-LINE REGULATION

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 34, R_{FB} is selected arbitrarily. The remaining compensation components are then selected according to Equation 34.

$$R_1 = R_{FB}\frac{C(ESR)}{\sqrt{LC} - C(ESR)}$$

$$C_1 = \frac{\sqrt{LC} - C(ESR)}{R_{FB}}$$

$$C_2 = \frac{0.75V_{IN}}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{P\text{-}P}}$$

$$R_C = \frac{V_{P\text{-}P}(2\pi)^2 f_0 f_{HF} LCR_{FB}}{0.75V_{IN}\left[\left(2\pi f_{HF}\sqrt{LC} - 1\right)\right]}$$

$$C_C = \frac{0.75V_{IN}\left(2\pi f_{HF}\sqrt{LC} - 1\right)}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{P\text{-}P}} \quad \textbf{(EQ. 34)}$$

In Equation 34, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and $V_{P\text{-}P}$ is the peak-to-peak sawtooth signal amplitude as described in Figure 7 and “Electrical Specifications” on page 6.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance (ESR) and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \qquad \textbf{(EQ. 35)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see “Interleaving” on page 11 and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,P-P}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR)\frac{\left(V_{IN} - N V_{OUT}\right) V_{OUT}}{f_{SW} V_{IN} V_{PP(MAX)}} \qquad \textbf{(EQ. 36)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 37 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 38 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2NCV_O}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right] \qquad \textbf{(EQ. 37)}$$

$$L \leq \frac{(1.25)NC}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right]\left(V_{IN} - V_O\right) \qquad \textbf{(EQ. 38)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in “MOSFETs” on page 36, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in “Output Filter Design” on page 40. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T (see the figure labelled Typical Application on page 5). Equation 39 is provided to assist in selecting the correct value for R_T.

$$R_T = \frac{2.5X10^{10}}{f_{SW}} \qquad \textbf{(EQ. 39)}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

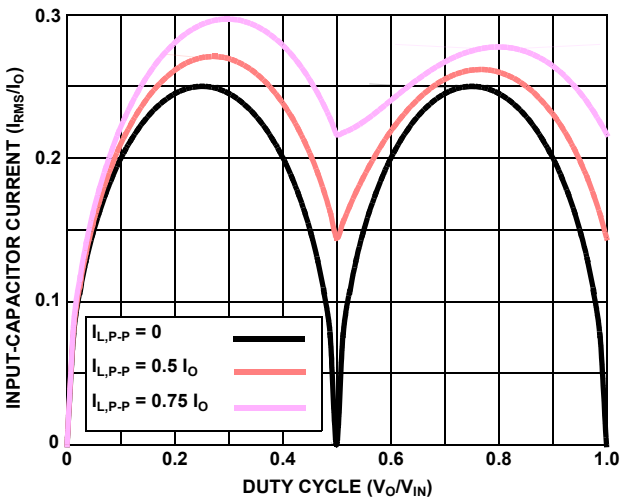


FIGURE 21. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

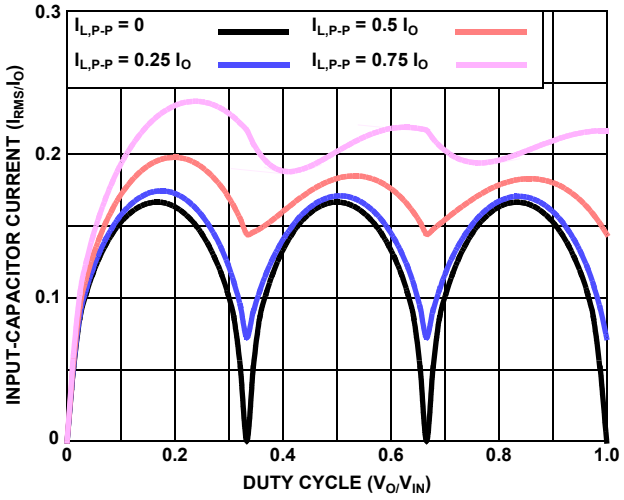


FIGURE 22. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

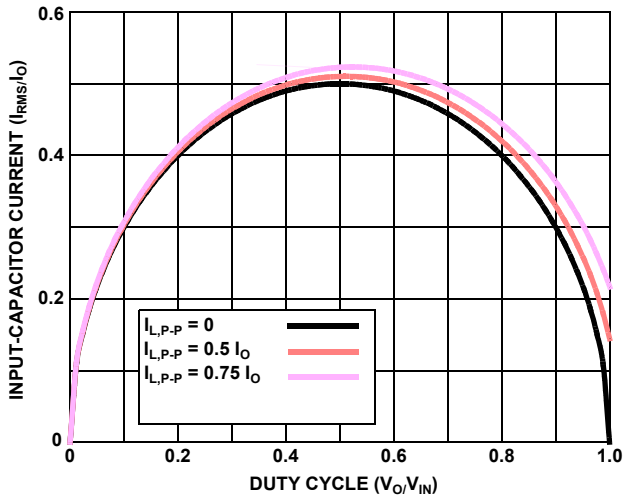


FIGURE 23. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

For a two phase design, use Figure 21 to determine the input-capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L,P-P}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

Figures 22 and 23 provide the same input RMS current information for three and four phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as described above.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize suppression.

Multiphase RMS improvement

Figure 23 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a two-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{L,P-P}$ to I_O of 0.5. The single phase converter would require $17.3A_{RMS}$ current capacity while the two-phase converter would only require $10.9A_{RMS}$. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

Layout Considerations

The following layout strategies are intended to minimize the impact of board parasitic impedances on converter performance and to optimize the heat-dissipating capabilities of the printed-circuit board. These sections highlight some important practices which should not be overlooked during the layout process.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position one high-frequency ceramic input capacitor next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

The EC7401QI can be placed off to one side or centered relative to the individual phase switching components. Routing of sense lines and PWM signals will guide final placement. Critical small signal components to place close to the controller include the ISEN resistors, R_T resistor, feedback resistor, and compensation components.

Bypass capacitors for the EC7401QI and ISL66XX driver bias supplies must be placed next to their respective pins. Trace parasitic impedances will reduce their effectiveness.

Plane Allocation and Routing

Dedicate one solid layer, usually a middle layer, for a ground plane. Make all critical component ground connections with vias to this plane. Dedicate one additional layer for power planes; breaking the plane up into smaller islands of common voltage. Use the remaining layers for signal wiring.

Route phase planes of copper filled polygons on the top and bottom once the switching component placement is set. Size the trace width between the driver gate pins and the MOSFET gates to carry 4A of current. When routing components in the switching path, use short wide traces to reduce the associated parasitic impedances.

Document Revision History

The table lists the revision history for this document.

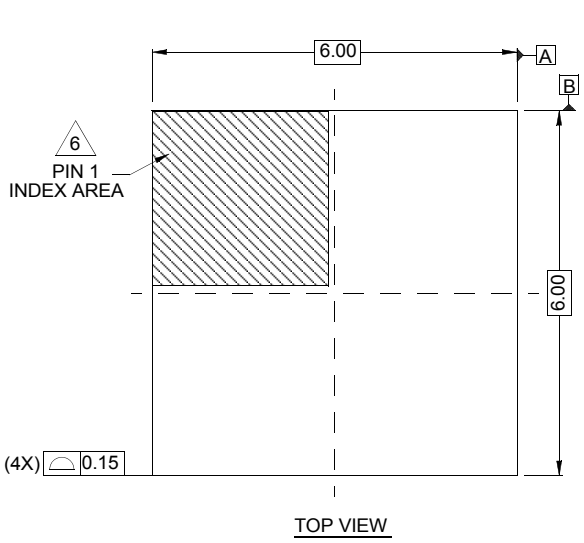
Date	Version	Changes
March 2014	1.0	Initial release.

Package Outline Drawing

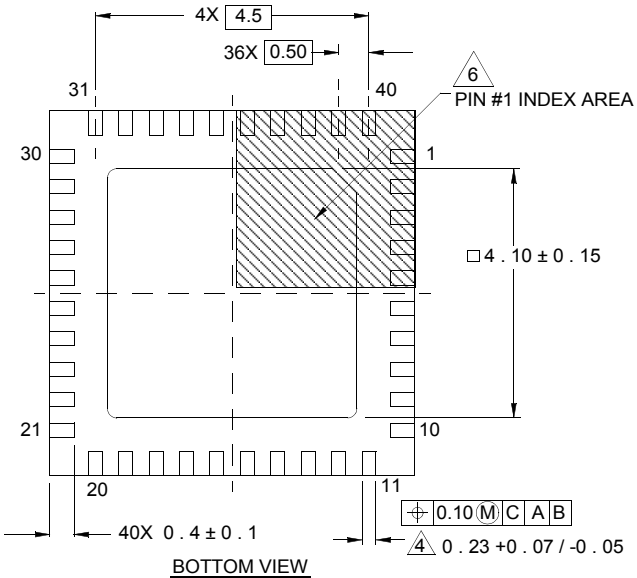
L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

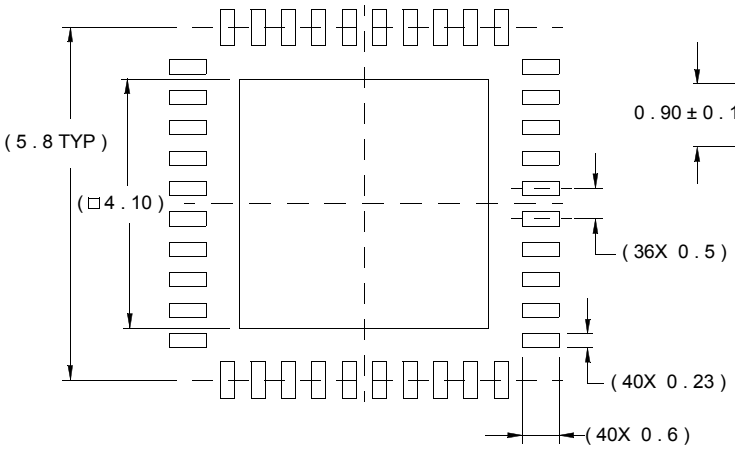
Rev 3, 10/06



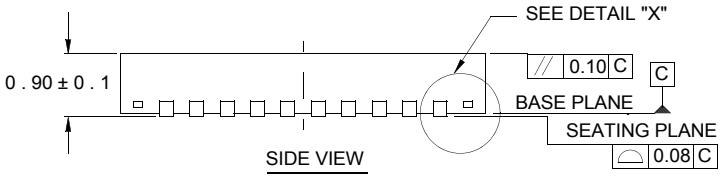
TOP VIEW



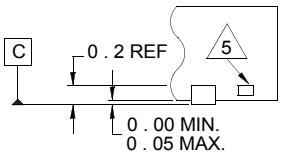
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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