Enpirion® Power Datasheet

ET4040QI 40A Power Stage High Speed MOSFET with Integrated Current and Temperature Sense

Description

The ET4040QI is a 40A, high speed, high density, monolithic power stage IC with integrated sensing features in a 5.5mm x 7.5mm x 0.95mm, 46 pin QFN package. It is targeted for low duty cycle operation, supplying low voltages for processor, DDR memory, and GPU core applications. The ET4040QI maintains very high efficiency at operating frequencies of 1MHz or greater. The ET4040QI enables 35% higher power density by utilizing 50-75% less inductance and significantly less output capacitance than current generation multi-phase power supply solutions. It integrates a current sense and temperature measurement function.

The device has a pin-selectable diode emulation mode to improve efficiency under PS2 and PS3 low power modes.

The ET4040QI is designed to interface with multi-phase PWM controllers and enables high efficiency delivery of up to 240 Amps for next generation CPU, DDR memory, and GPU core memory applications.

All Altera Enpirion products are RoHS compliant, halogen free and are compatible with lead-free manufacturing environments.

Features

- 40A continuous Operating Current
- 96.4% Peak Efficiency at 500KHz (3.3V at 12A)
- 3MHz Maximum Operating Frequency
- 1.8°C/W Junction-to-Top Thermal Resistance
- 35% Higher Power Density
- No POSCAP or Electrolytic Capacitors Needed
- Thermally Enhanced Low Inductance Package
- Integrated Gate Drive Independent of Drive Voltage
- Integrated Inductor-less Current Sense
- Integrated Die Temperature Sense
- Tri-state Control Option
- Diode Emulation Mode for Light Load Efficiency
- Top-side Cooling for Heat-sink Attachment
- RoHS Compliant, MSL Level 3, 260°C Reflow

Applications

- High Density Power Stage in Conjunction with Multi-phase Controllers
- CPU Core, Non-core, Peripheral and DDR Memory Core Power Supplies
- GPU Core Regulation
- Servers, Desktops, Telecommunications, Equipment, Industrial and Embedded computing

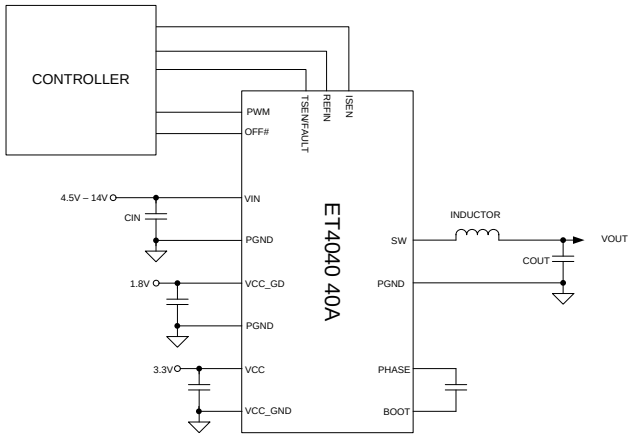


Figure 1. Simplified Applications Circuit

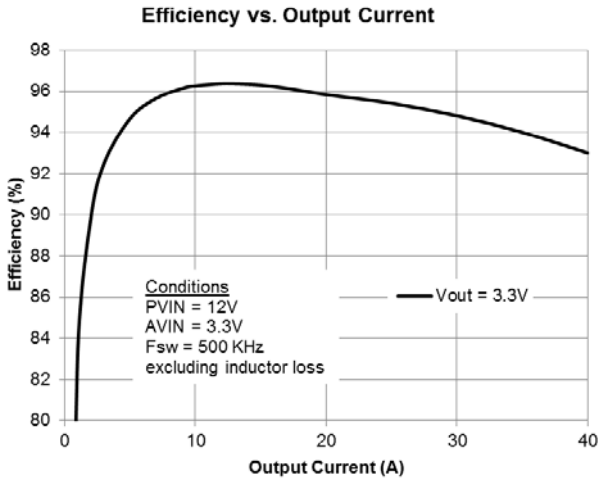


Figure 2. Highest Efficiency

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
ET4040QI	ET4040QI	-40 to +85	46-pin (5.5mm x 7.5mm x 0.95mm) QFN T&R
ET4040QI-E	Evaluation Board		

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

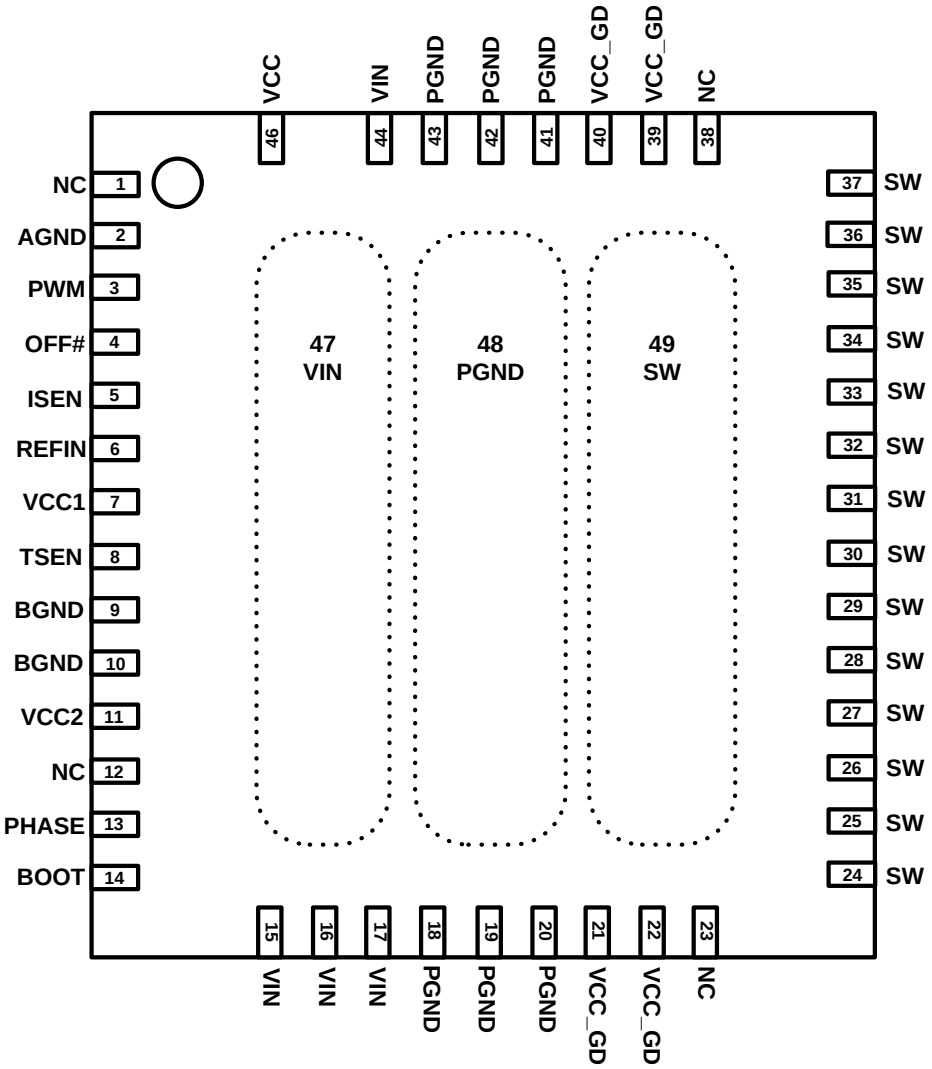


Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. All pins including NC pins must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: The dotted outlines in the center of the package represent the exposed pads on the bottom of the package for VIN, PGND, and SW which are required to be soldered to the PCB.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

I/O Legend: P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/Output

PIN	NAME	I/O	FUNCTION
1,12, 23,38	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
2	AGND	G	Analog ground. This is the ground return for the controller. All AGND pins need to be connected to a quiet ground.
3	PWM	I	PWM control signal. Logic LOW = Low-side FET enabled. Logic HIGH = high-side FET enabled. FLOAT = Tri-state, both LS and HS FETs disabled. See PWM Pin Characteristics table for additional details.
4	OFF#		Low-side OFF signal. Logic LOW = low-side FET disabled. Logic HIGH = normal PWM operation, LS FET enabled. OFF# is used to turn off the low-side driver during PS2 and PS3 low-power modes, where diode emulation is used to improve efficiency.
5	ISEN	I	Current Monitor Output. Provides a bandwidth limited (nominally 3.6 MHz) replica of the current waveform at the SW node. See Current Monitor Characteristics section for more details. Use 5 kΩ low TC resistor between ISEN and REFIN.
6	REFIN		Reference level shift voltage for the ISEN pin. Provided by the controller. See Current Monitor Characteristics section for more details.
7	VCC1		Connect VCC1 to VCC pin.
8	TSEN		Temperature monitor output. See Electrical Characteristics table and Functionality and Features section for description.
9, 10	BGND		Connect to AGND.
11	VCC2		Connect VCC2 to VCC pin.
13	PHASE		Bottom plate of High-Side FET boot capacitor. Use X5R ceramic on top-side of PCB only and critically located very close to device pins (PHASE and BOOT).
14	BOOT		Top plate of High-Side FET boot capacitor. Use X5R ceramic on top-side of PCB only and critically located very close to device pins (PHASE and BOOT).
15-17, 44	VIN	I	Power input supply for drivers.
18-20, 41-43	PGND	G	Input/output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
21, 22, 39, 40	VCC_GD	I	1.8V supply for gate drivers.
24-37	SW		Driver drain/switch node pins. Connect an external inductor from SW to the output.
46	VCC	I	3.3V supply for analog control circuits.
47	VIN	I	Not a perimeter pin. Power input supply for drivers. This VIN is exposed on the package underside. Tie to VIN plane on EVB with buried vias. High-quality connection to VIN plane critical for thermal and electrical performance.
48	PGND	G	Not a perimeter pin. Input/output power ground. This PGND is exposed on package underside. Tie to PGND plane on EVB with buried VIAs. High-quality connection to PGND plane critical for thermal and electrical performance.
49	SW		Not a perimeter pin. Driver drain/switch node. This SW is exposed on package underside. Tie to SW node/plane on EVB with wide copper on top layer. High-quality connection to inductor is critical.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on Power MOSFET Input Supply VIN	VIN	-0.3	16	V
VIN Slew Rate (Note 1)	VIN_{SLEW}	0.3	10	V/ms
Voltages on gate drive input supply VCC_GD	VCC_GD	-0.3	2.1	V
Voltages on logic input supply VCC	VCC	-0.3	5.5	V
Voltages on control pin OFF#,	OFF#	-0.3	5.5	V
Voltages on ISEN, TSEN		-0.3	5.5	V
Voltages on BOOT	BOOT	-0.3	16	V
Voltages on PHASE	PHASE	-0.3	2.1	
Voltages on REFIN	REFIN	-0.3	5.5	V
Voltages on PWM input signal	PWM	-0.3	5.5	V
Voltages on PGND	PGND	-0.3	0.3	V
Voltages on logic ground AGND	AGND	-0.3	0.3	V
Voltages on switch (common drain) node	SW	-2.0	VIN+0.3	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temperature, 10 sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)		2000		V
ESD Rating (based on CDM)		500		V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage to Power MOSFETs	VIN	4.5	12	14.5	V
Supply voltage to the MOSFETs gate driver	VCC_GD	1.6	1.8	2.0	V
Supply voltage to logic circuits	VCC	3.0	3.3	3.6	V
Operating junction temperature		0		+125	^{o}C
Continuous load current	I_{LOAD}			40	A
Operating ambient temperature		-40		+85	^{o}C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Top-side (0 LFM)	θ_{JT}	1.8	°C/W
Thermal Resistance: Junction to Bottom-side (0 LFM)	θ_{JB}	2.0	°C/W

Note 1: PVIN rising and falling slew rates cannot be outside of specification. For accurate power up sequencing, use a fast ENABLE logic after both AVIN and PVIN is high.

Electrical Characteristics

NOTE: V_{IN}=12V, Minimum and Maximum values are over operating ambient temperature range (-40°C ≤ T_A ≤ +85°C) unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE LEVEL CHARACTERISTICS						
Operating VIN Voltage Range	V_{VIN}		4.5		14.5	V
Operating VCC Voltage Range	V_{PVCC}		3.0	3.3	3.6	V
Operating VCC_GD Voltage Range	V_{PVCC_GD}		1.5	1.8	2.0	V
VCC Quiescent Current	I_{QVCC}	PWM = Low	1.4	1.8	2.3	mA
VIN Quiescent Current – No Switching	I_{QVIN_NS}	PWM = Low	2.5	3.3	4.2	mA
VIN Quiescent Current – Switching	I_{QVIN}	Freq(PWM) = 600 kHz, Duty Cycle = 20%	45	60	75	mA
VCC_GD Quiescent Current – No Switching	$I_{QVCC\_GD\_NS}$	PWM = Low, VCC_GD = 1.8V	340	450		µA
VCC_GD Quiescent Current – Switching	I_{QVCC_GD}	Freq(PWM) = 600 kHz VCC_GD = 1.8V	22	30	50	mA
Low-Side Rds_on				1.4	1.6	mΩ
High-Side Rds_on				6.6	8	mΩ
CURRENT MONITORING (ISEN) CHARACTERISTICS						
Trans-impedance Gain		R_ISEN = 5KΩ		5.5		mV/A
ISEN Output Resistor	R_ISEN	External Resistor between ISEN and REFIN pins. 0.1% tolerance recommended.		1.5		kΩ
ISEN Output Resistor – Temperature Coefficient	TC_RISEN	Use 0TC Resistor		0		mΩ/°C
ISEN External Parasitic or LOAD Capacitance	C_ISEN	External parasitic capacitance reduces ISEN replica bandwidth			5	pF
ISEN – Zero-current DC Output Voltage		ILOAD = 0A, REFIN=1.8V, R_ISEN=5KΩ Referenced to AGND	1.785	1.8		V
ISEN – Maximum Output Voltage			2.5			V
ISEN – Output Current (into REFIN)		REFIN = 1.8V REFIN must be capable of sinking or sourcing this current.	-200	0	200	µA
REFIN Allowable Voltage Range		Referenced to AGND	0.8		2.1	V
THERMAL MONITORING (TSEN)						
Thermal Gain			7.8	8	8.2	mV/C
0C Output Voltage		Temp = 0C	0.582	0.6	0.618	V
150C Output Voltage		Temp = 150C	1.746	1.8	1.854	V

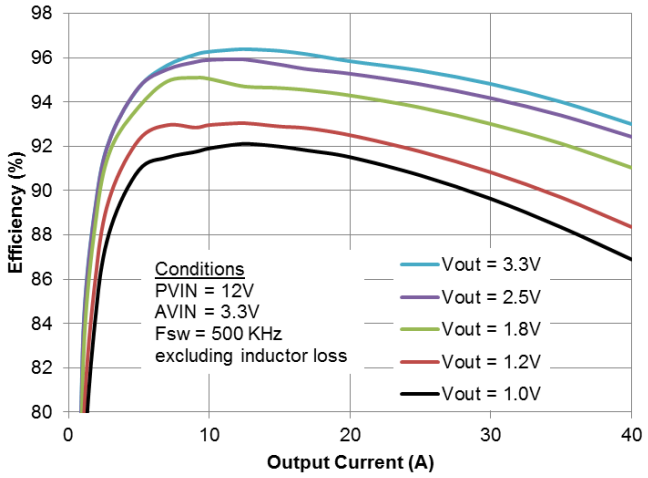
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance					10	pF
Output Resistance, Sourcing					100	Ω
Source Current			1			mA
Sink Current			100			µA
Maximum Number of ORed Phases					7	Phases
Maximum Load Capacitance					1000	pF
PWM PIN CHARACTERISTICS						
Equivalent Input Resistance				6		kΩ
Input Capacitance					10	pF
Input Current		VPWM = VCC = 3.3V		250	330	µA
Logic Low Level		VCC = 3.3V, Relative to AGND	-0.3		+0.8	V
Logic High Level		VCC = 3.3V	2.4V		3.6	V
Logic Low Hysteresis		VCC = 3.3V		110		mV
Logic High Hysteresis		VCC = 3.3V		180		mV
Tri-State Thresholds		VCC = 3.3V	1.2		2	V
Floating Tri-State Voltage		PWM floated/driven with high impedance (>10 MΩ)		VCC/ 2		V
Input Rise Time (note 2)					5	ns
Input Fall Time (note 2)					5	ns
Turn-off Propagation Delay (note 2)		Delay from PWM input HIGH to LOW to beginning of SW transition		24		ns
Turn-on Propagation Delay (note 2)		Delay from PWM input LOW to HIGH to beginning of SW transition		22		ns
Tri-state Hold-Off Time (note 2)		Delay from Tri-State active level transition on PWM to beginning of transition to tri-state on SW		50		ns
Tri-state to Active High - SW Rising Propagation Delay (note 2)		Delay - PWM transition high from tri-state mode to start of high-side assertion		22		ns
Tri-state to Active Low – SW Assertion Low Propagation Delay (note 2)		Delay - PWM transitions to low state from tri-state mode to start of low-side assertion		22		ns
OFF# PIN CHARACTERISTICS						
Logic Low		Relative to AGND	-0.3		0.8	V
Logic High		VCC=3.3V	2.3		VCC + 0.3	V
Hysteresis				800		mV
Input Resistance		(pull-up to VCC)	150	300	450	kΩ
Input Capacitance					10	pF
Input Rise Time					5	ns
Input Fall Time					5	ns
Delay – Logic LOW to				30		ns

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
NFET OFF						
Delay – Logic HIGH to NFET ON		PWM=0		30		ns
VCC_GD UVLO CHARACTERISTICS						
Operating VCC_GD Voltage Range	V_{PVCC_GD}		1.6		2.0	V
UVLO Falling Threshold	UVLO_FALL		0.9			V
UVLO Rising Threshold	UVLO_RISE				1.55	V
UVLO Hysteresis				150		mV

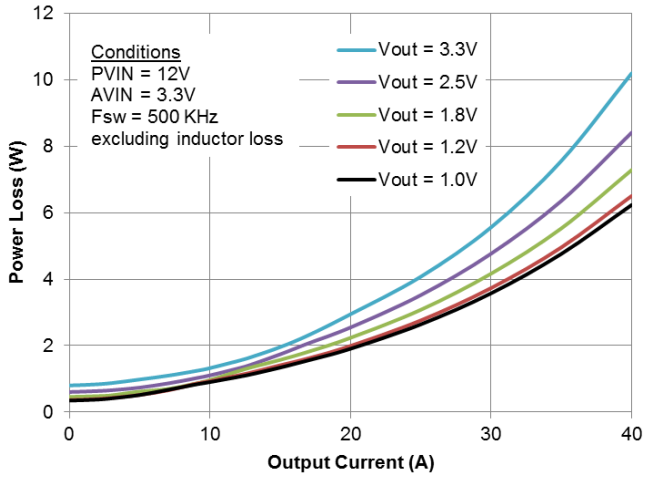
Note 2: Parameter not production tested but is guaranteed by design.

Typical Performance Curves

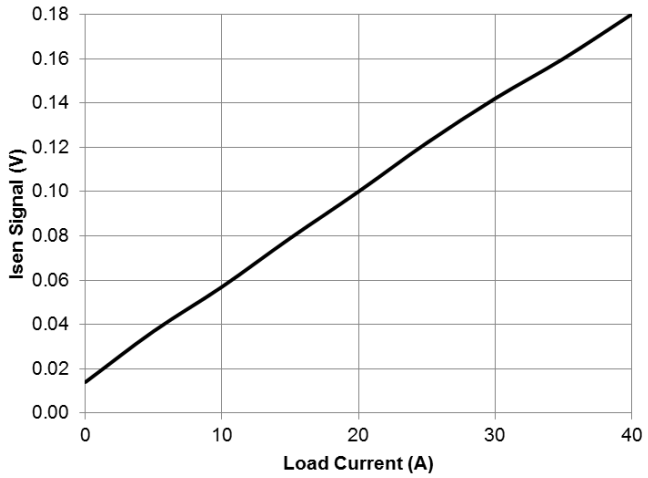
Efficiency vs. Output Current



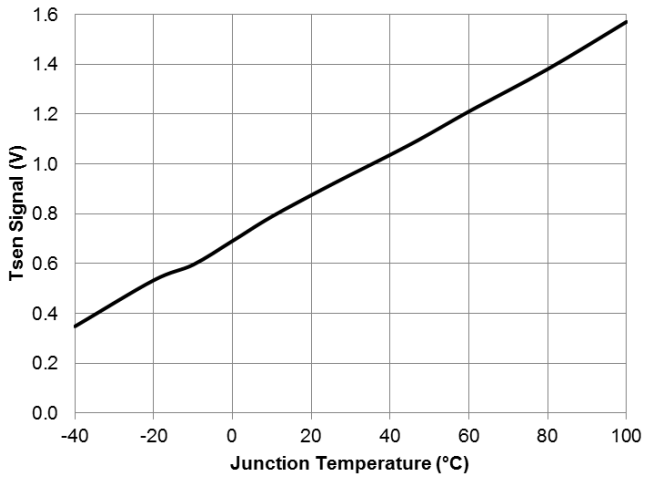
Power Loss vs. Output Current

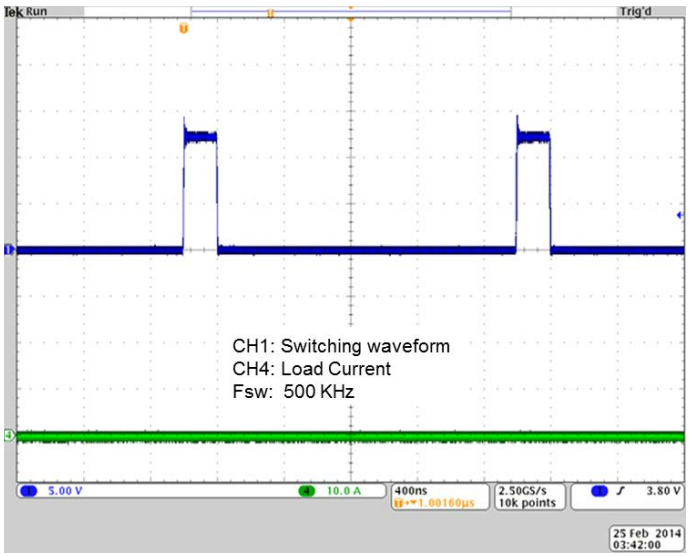


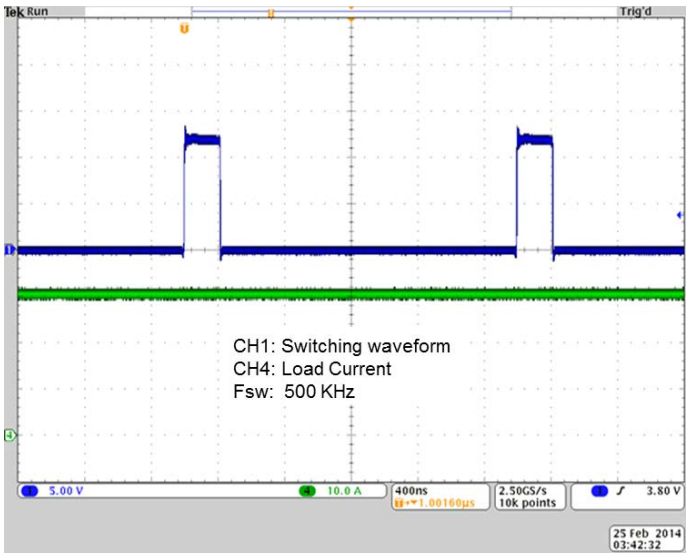
Isen vs. Output Current



Tsen vs. Temperature







Functional Block Diagram

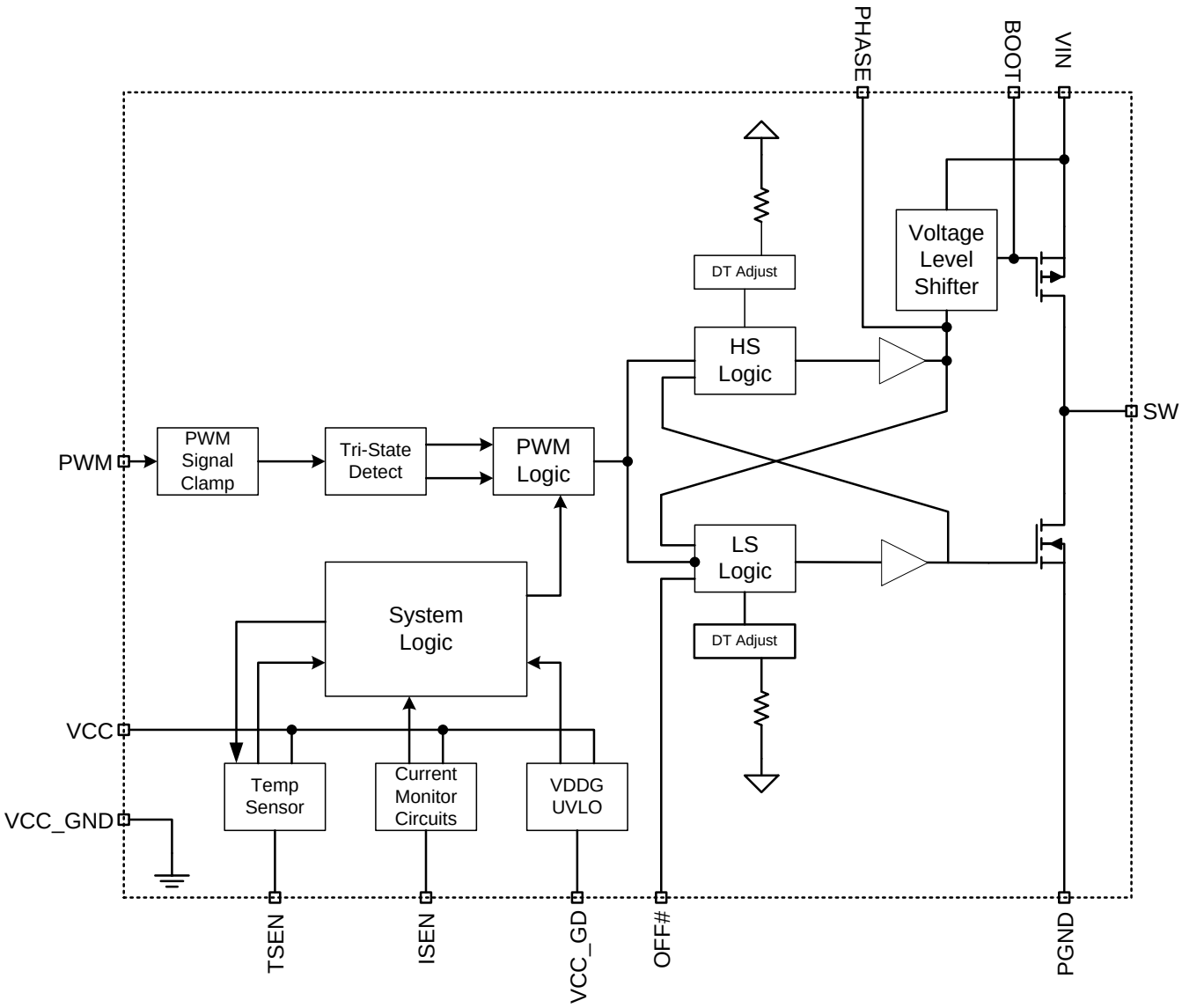


Figure 4: Functional Block Diagram

Functional Description

ET4040QI Power Train

The ET4040QI is a monolithic 40A driver stage that integrates P-Channel high side power MOSFET, N-Channel low side power MOSFET and an optimized high speed gate driver. The device also includes die temperature monitoring, current sensing, and high side MOSFET short circuit detection circuitry. The ET4040QI also has a pin-selectable diode emulation mode for improved efficiency under light load conditions.

The ET4040QI utilizes Enpirion's advanced high frequency LDMOS process to enable high switching frequency and high efficiency. The ET4040QI has industry leading figure of merit (FOM) providing for very low switching loss hence enabling high switching frequency for small external inductor and capacitors.

Configured properly, the ET4040QI does not require any bulk electrolytic or POSCAPs. Only low cost Ceramic MLCC capacitors are required.

ET4040QIQI Power Train

Pulse Width Modulator (PWM) pin is a Tri-state input signal. Floating or “tri-stating” this pin will turn off both high side and low side MOSFETs.

When PWM is placed in tri-state mode, the PWM signal is internally pulled to 1.6V. This simplifies the tri-state operation and prevents indeterminate states from occurring.

Table 1. PWM Logic state table.

PWM	High Side MOSFET	Low Side MOSFET
Low	OFF	ON
High	ON	OFF
Float	OFF	OFF

Shoot Through Protection

The ET4040QIQI employs an advanced shoot through protection scheme. Feedback is used from each gate to ensure that both MOSFETs are never on simultaneously.

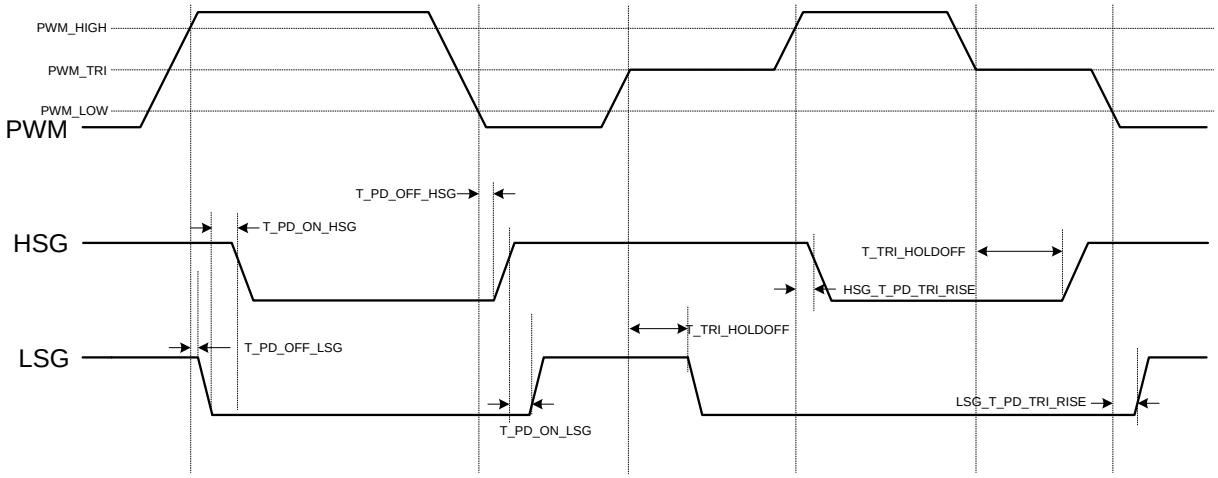


Figure 1. PWM, LSG (Low Side Gate) and HSG (High Side Gate) timing. Note: HSG is active low, LSG is active high.

ISEN Current Sense Output

The current monitoring function provides a voltage based replica of the dynamic inductor current waveform, including both static output current and dynamic ripple current contributions. The nominal replication bandwidth is 3.6 MHz – given the nominal output resistance of 5kΩ, parasitic loading on this pin should be minimized. The voltage on ISEN is the sum of the current monitoring output voltage and the REFIN pin, allowing ISEN to be summed with REFIN. The ISEN control and sensing circuits are internally temperature compensated, allowing the ISEN indication to correctly track output current even as internal junction temperature changes due to self-heating and due to changes in ambient temperature.

TSEN Temperature Monitor

The ET4040QI provides a thermal monitor that indicates the internal junction temperature of the device with a conversion factor of ~8 mV/C – this indication occurs on the TSEN pin. Additional specifications relative to TSEN are provided in the corresponding Electrical Characteristics section. The TSEN pin of multiple devices/phases can be wired-ORed together, allowing the hottest phase with the highest temperature to control the temperature indication. The maximum number of phases that can be ORed together is seven.

Application Information

Under Voltage Lock Out

The gate driver supply rail, VCC_GD, is monitored to ensure a valid supply voltage is present that allows the gate driver control and driver circuitry to properly function. If the VCC_GD supply drops below UVLO_FALL or fails to rise above UVLO_RISE, the UVLO monitor counts 3 PWM pulses or a nominal maximum persistence of 15 uSec, at which point switching is disabled at the next immediate ON cycle. When the UVLO condition clears, the driver allows switching to continue. An UVLO event is NOT and indicated fault and therefore does not toggle the TSEN/FAULT pin or latch into the FAULT latch

Diode Emulation Mode

The ET4040QI diode emulation mode enables increased light load efficiency by preventing negative inductor current from flowing through the low-side (synchronous) MOSFET. Diode emulation mode is controlled with the active low OFF# signal. When the OFF# pin is asserted low, the low side MOSFET will be turned off. The high side MOSFET will be continue to follow the PWM signal commands.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Altera Enpirion PowerSoC helps alleviate some of those concerns.

The Altera Enpirion ET4040QI Power Train is packaged in an 5.5x7.5mm 46-pin QFN package. The exposed ground pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability.

The ET4040QI is guaranteed to support the full 40A output current up to 85°C ambient temperature. The following example and calculations illustrate the thermal performance of the ET4040QI.

Example:

V_{IN} = 12V

V_{OUT} = 1.0V

I_{OUT} = 40A

First calculate the output power.

P_{OUT} = 1.0V x 40A = 40W

Next, determine the input power based on the efficiency (η) shown in Figure 11.

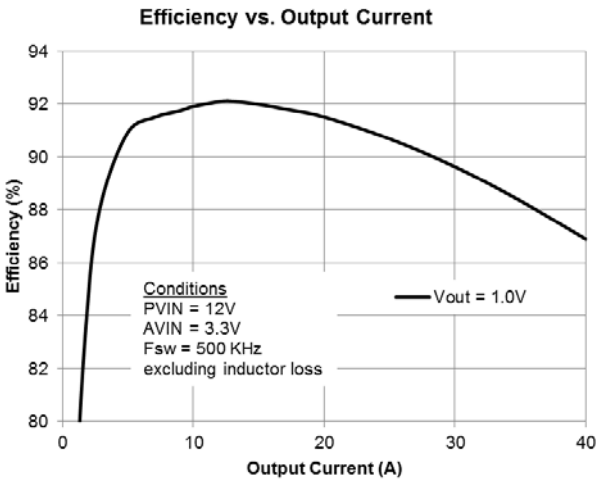


Figure 11: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 1.0V at 40A, η ≈ 86.9%

η = P_{OUT} / P_{IN} = 86.9% = 0.869

P_{IN} = P_{OUT} / η

P_{IN} ≈ 40W / 0.869 ≈ 46W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 46W – 40W ≈ 6.0W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JPCB value (θ_{JPCB}). The θ_{JPCB} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The ET4040QI Evaluation Board has a θ_{JPCB} value of 6 ºC/W without airflow and heatsink (the PCB board temperature is measured 3cm from the device).

Determine the change in temperature (ΔT) based on P_D and θ_{JPCB}.

ΔT = P_D x θ_{JPCB}

ΔT ≈ 6.0W x 6°C/W = 36°C

The junction temperature (T_J) of the device is approximately the PCB board temperature (T_B) plus the change in temperature.

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the maximum board temperature (T_{BMAX}) allowed can be calculated.

T_{BMAX} = T_{JMAX} – P_D x θ_{JPCB}

≈ 125°C – 36°C ≈ 89°C

The maximum board temperature the device can reach is 89°C given the input and output voltage at no airflow and no heatsink conditions. Note that larger size PCB board, heatsink and airflow will greatly improve the thermal performance.

Engineering Schematic

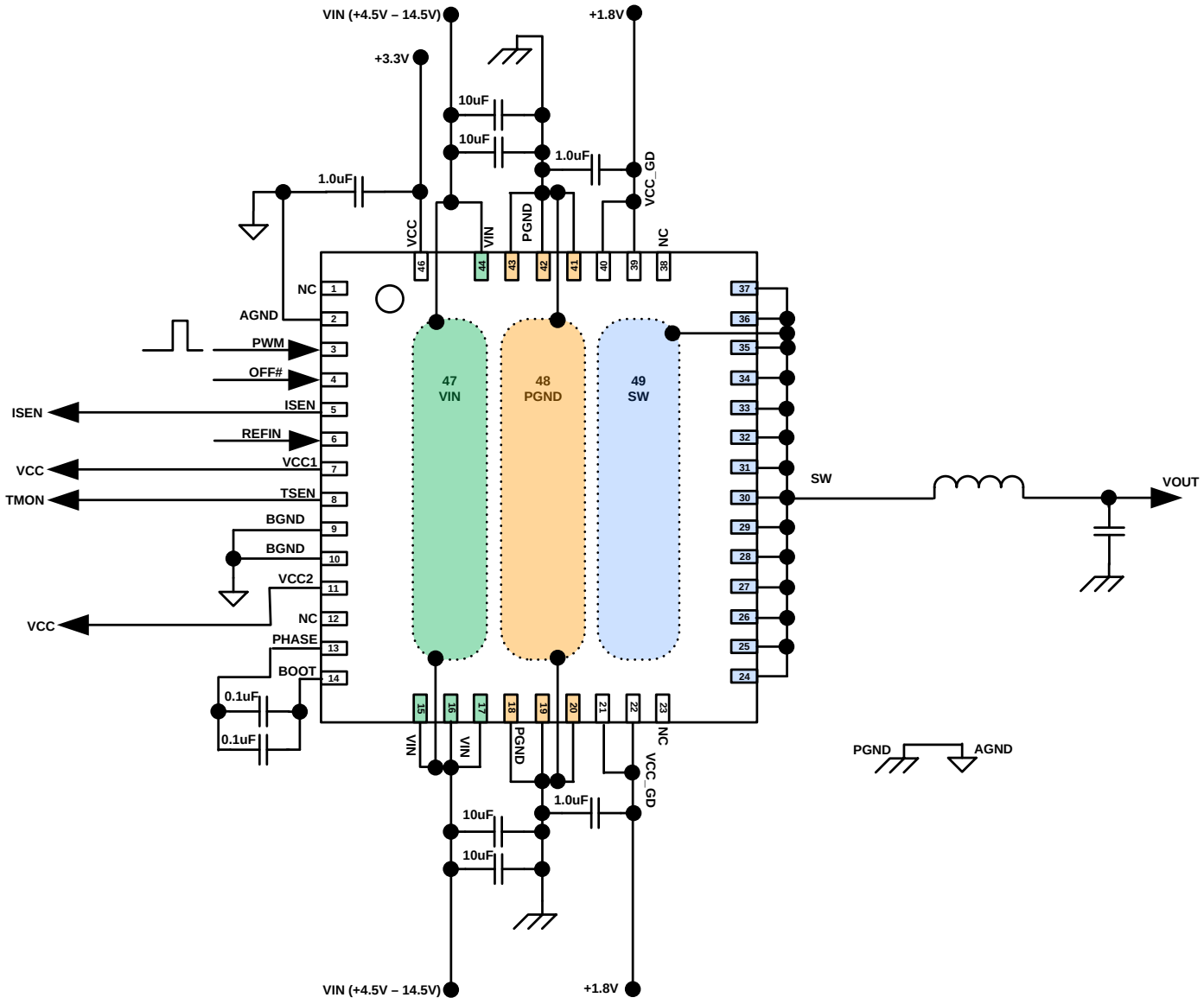


Figure12. Pin interconnection diagram.

Recommended PCB Footprint

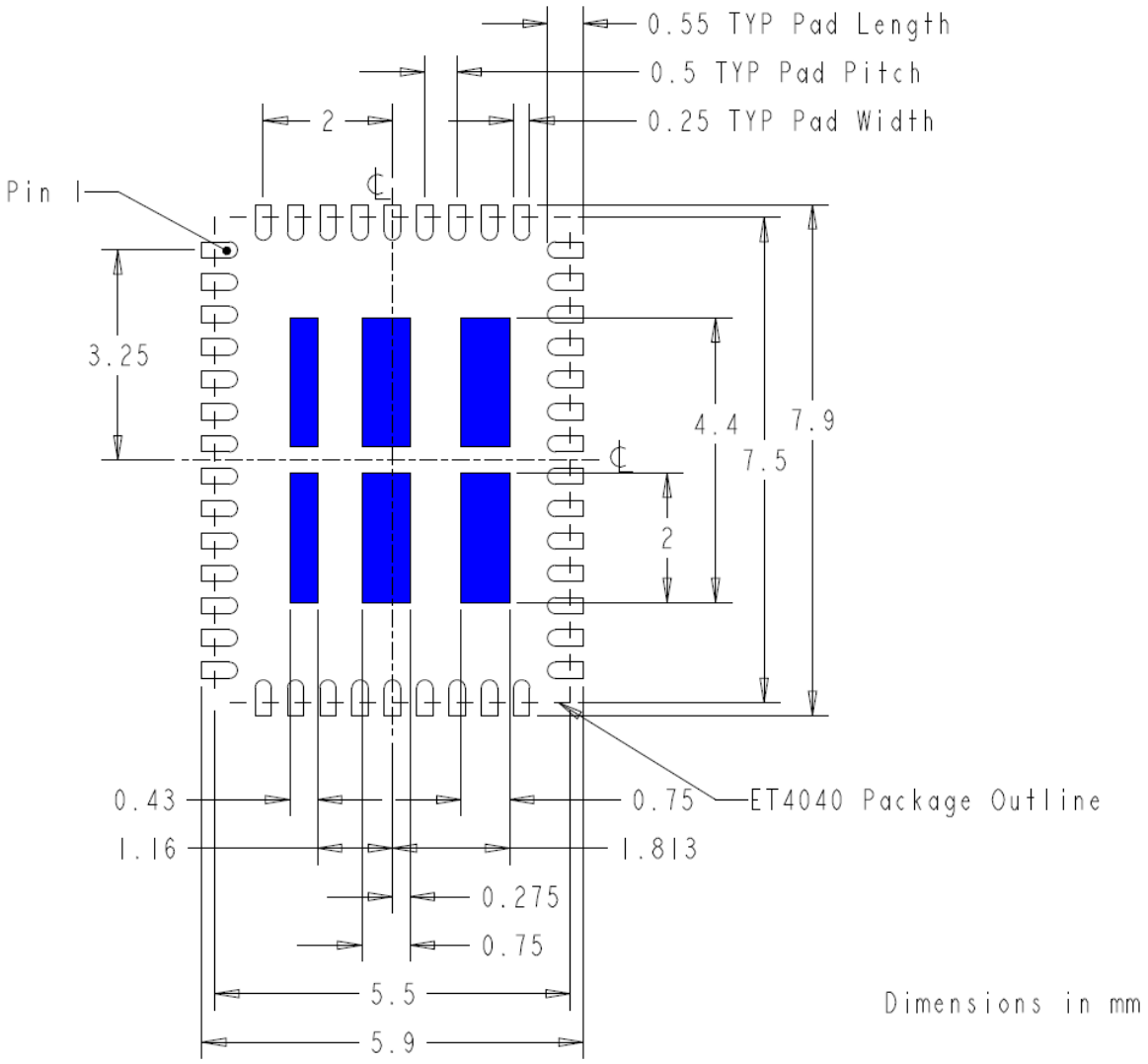


Figure 14: ET4040QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad (shown in blue) is based on Altera's manufacturing recommendations

Package and Mechanical

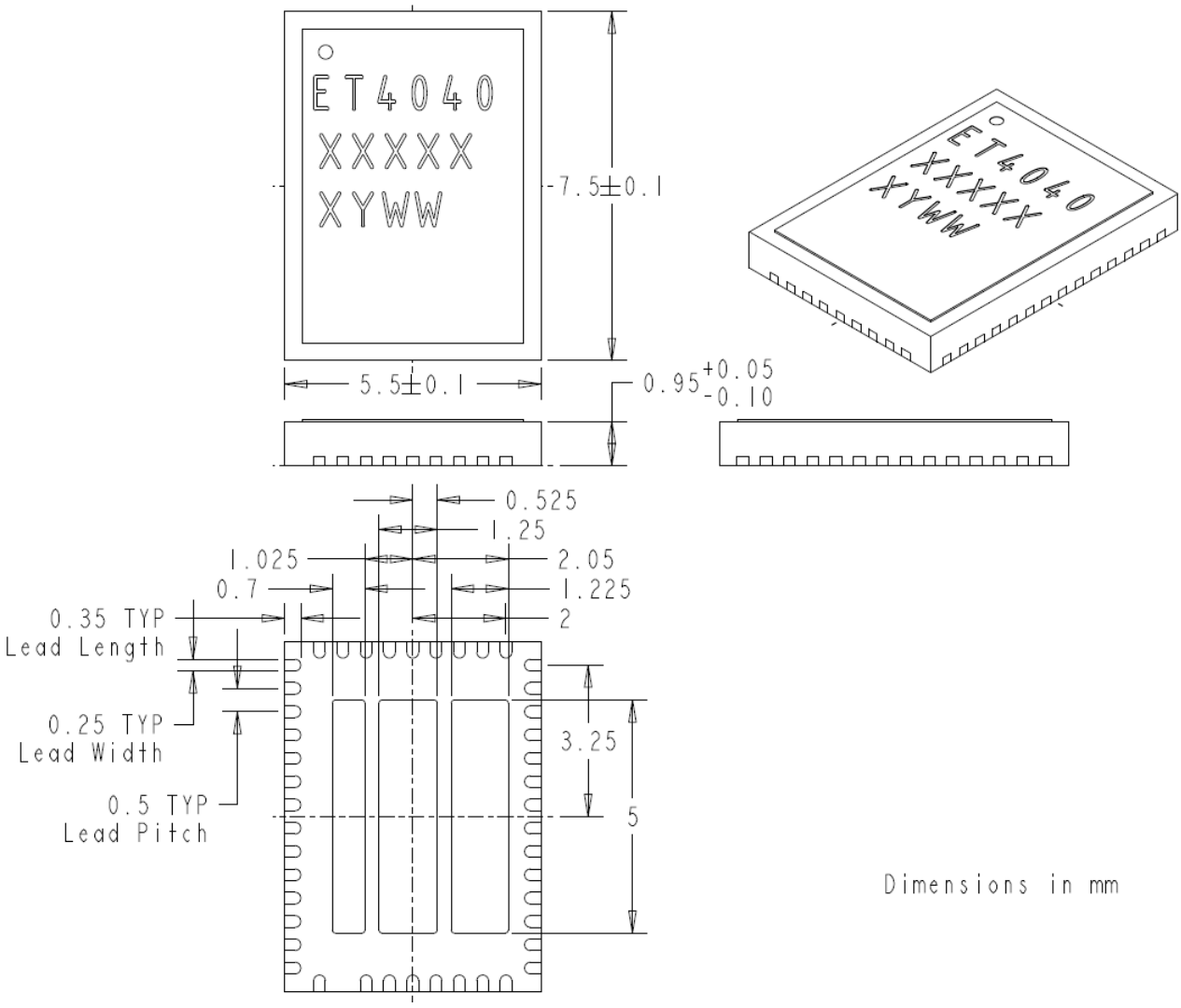


Figure 15: ET4040QI Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Contact Information

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Mouser Electronics

Authorized Distributor

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