Advanced Double-Ended PWM Controller

ISL6742B

The ISL6742B is a high-performance double-ended PWM controller with advanced synchronous rectifier control and current limit features. It is suitable for both current- and voltage-mode control methods.

The ISL6742B includes complemented PWM outputs for synchronous rectifier (SR) control. The complemented outputs may be dynamically advanced or delayed relative to the main outputs using an external control voltage.

Its advanced current sensing circuitry employs sample and hold methods to provide a precise average current signal. Suitable for average current limiting, a technique which virtually eliminates the current tail-out common to peak current limiting methods, it is also applicable to current sharing circuits and average current mode control.

This advanced BiCMOS design features an adjustable oscillator frequency up to 2MHz, internal over-temperature protection, precision deadtime control, and short propagation delays. Additionally, Multi-Pulse Suppression ensures alternating output pulses at low duty cycles where pulse skipping may occur.

Ordering Information

PART # (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6742BAAZA	ISL6742 BAAZ	-40 to +105	16 Ld QSOP	M16.15A

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6742B. For more information on MSL, please see tech brief TB363.

Features

- Synchronous rectifier control outputs with adjustable delay/advance
- Adjustable average current signal
- 3% tolerance cycle-by-cycle peak current limit
- Fast current sense to output delay
- Adjustable oscillator frequency up to 2MHz
- Adjustable deadtime control
- Voltage- or current-mode operation
- Separate RAMP and CS inputs for voltage feed-forward or current-mode applications
- Tight tolerance error amplifier reference over line, load, and temperature
- 175µA start-up current
- Supply UVLO
- Adjustable soft-start
- 70ns leading edge blanking
- Multi-pulse suppression
- Internal over-temperature protection
- Pb-Free (RoHS compliant)

Applications

- Half-bridge, full-bridge, interleaved forward, and push-pull converters
- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems

Related Literature

- See AN1890, "ISL6742BEVAL3Z Power Converter 36V to 75V Input, 12V Output Up to 10A"

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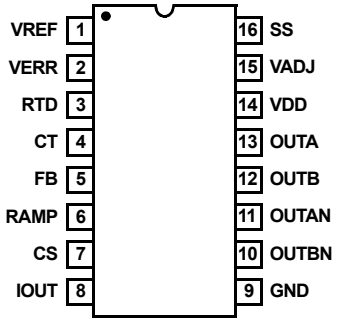
Pin Configuration

ISL6742B
(16 LD QSOP)
TOP VIEW



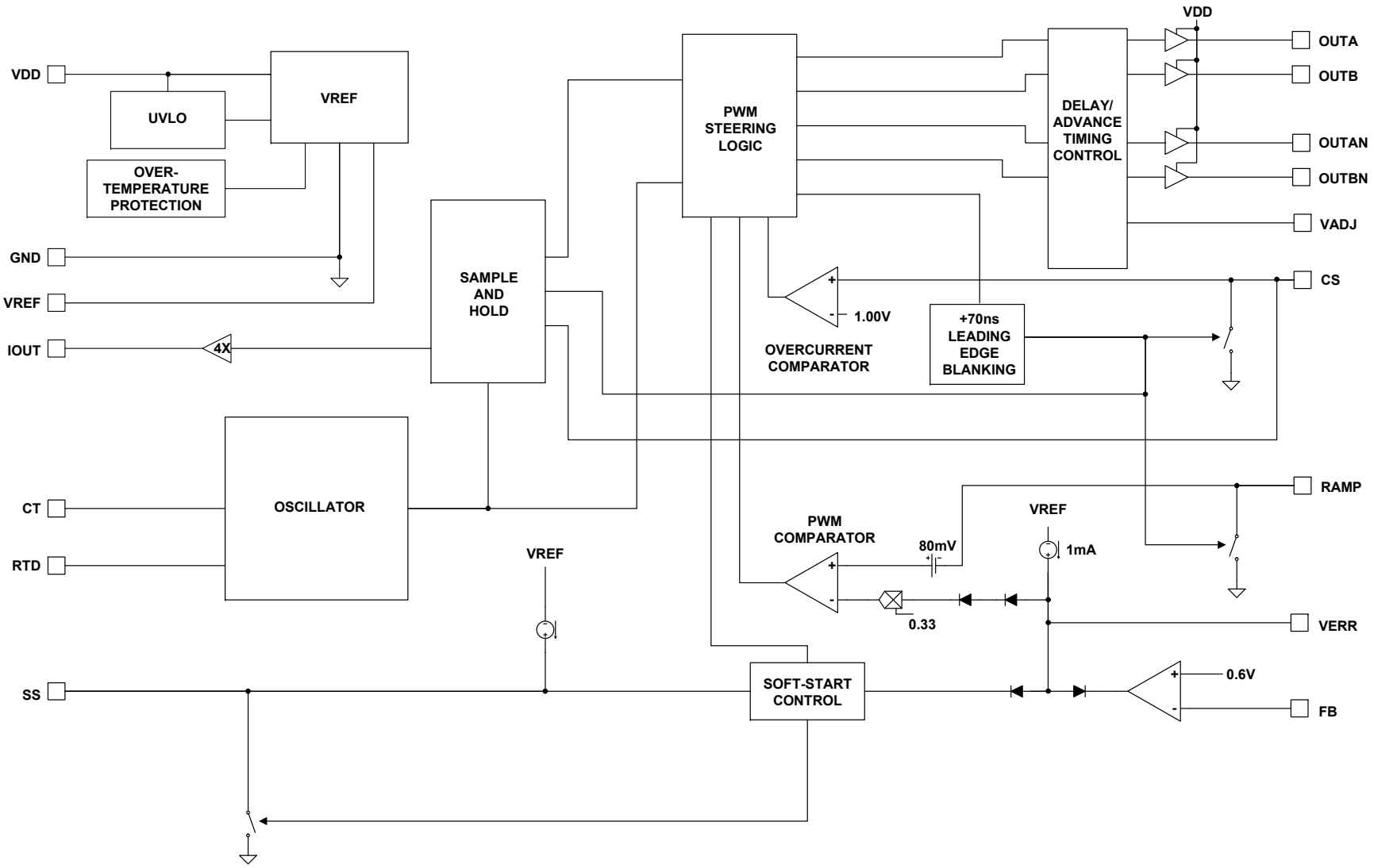
Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	VREF	The 5V reference voltage output having 3% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 2.2µF low ESR capacitor.
2	VERR	The VERR pin is the output of the error amplifier and controls the inverting input of the PWM comparator. Feedback compensation components connect between VERR and FB. There is a nominal 1mA pull-up current source connected to VERR. Soft-start is implemented as a voltage clamp on the VERR signal. The outputs, OUTA and OUTB, reduce to 0% duty cycle when VERR is pulled below 0.6V. OUTAN and OUTBN, the complements of OUTA and OUTB, respectively, go to 100% duty cycle when this occurs.
3	RTD	This is the oscillator timing capacitor discharge current control pin. The current flowing in a resistor connected between this pin and GND determines the magnitude of the current that discharges CT. The CT discharge current is nominally 20x the resistor current. The PWM deadtime is determined by the timing capacitor discharge duration. The voltage at RTD is nominally 2V. The minimum recommended value of RTD is 2.00kΩ.
4	CT	The oscillator timing capacitor is connected between this pin and GND. It is charged through an internal 200µA current source and discharged with a user adjustable current source controlled by RTD.
5	FB	FB is the inverting input to the error amplifier (EA). The amplifier may be used as the error amplifier for voltage feedback or used as the average current limit amplifier (IEA). If the amplifier is not used, FB should be grounded.
6	RAMP	This is the input for the sawtooth waveform for the PWM comparator. The RAMP pin is shorted to GND at the termination of the PWM signal. A sawtooth voltage waveform is required at this input. For current-mode control this pin is connected directly to CS and the current loop feedback signal is applied to both inputs. For voltage-mode control, the oscillator sawtooth waveform may be buffered and used to generate an appropriate signal, or RAMP may be connected to the input voltage through an RC network for voltage feed forward control, or RAMP may be connected to VREF through an RC network to produce the desired sawtooth waveform.
7	CS	This is the input to the overcurrent comparator and the average current sample and hold circuit. The overcurrent comparator threshold is set at 1V nominal. The CS pin is shorted to GND at the termination of either PWM output. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch. This delay may result in CS being discharged prior to the power switching device being turned off.
8	IOUT	Output of the 4x buffer amplifier of the sample and hold circuitry that captures and averages the CS signal.
9	GND	Signal and power ground connections for this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.
11, 10	OUTAN and OUTBN	These outputs are the complements of OUTA and OUTB, respectively. These outputs are suitable for control of synchronous rectifiers. The phase relationship between each output and its complement is set by a control voltage applied to VADJ.
13, 12	OUTA and OUTB	These paired outputs are the pulse width modulated outputs for controlling the switching FETs in alternate sequence.

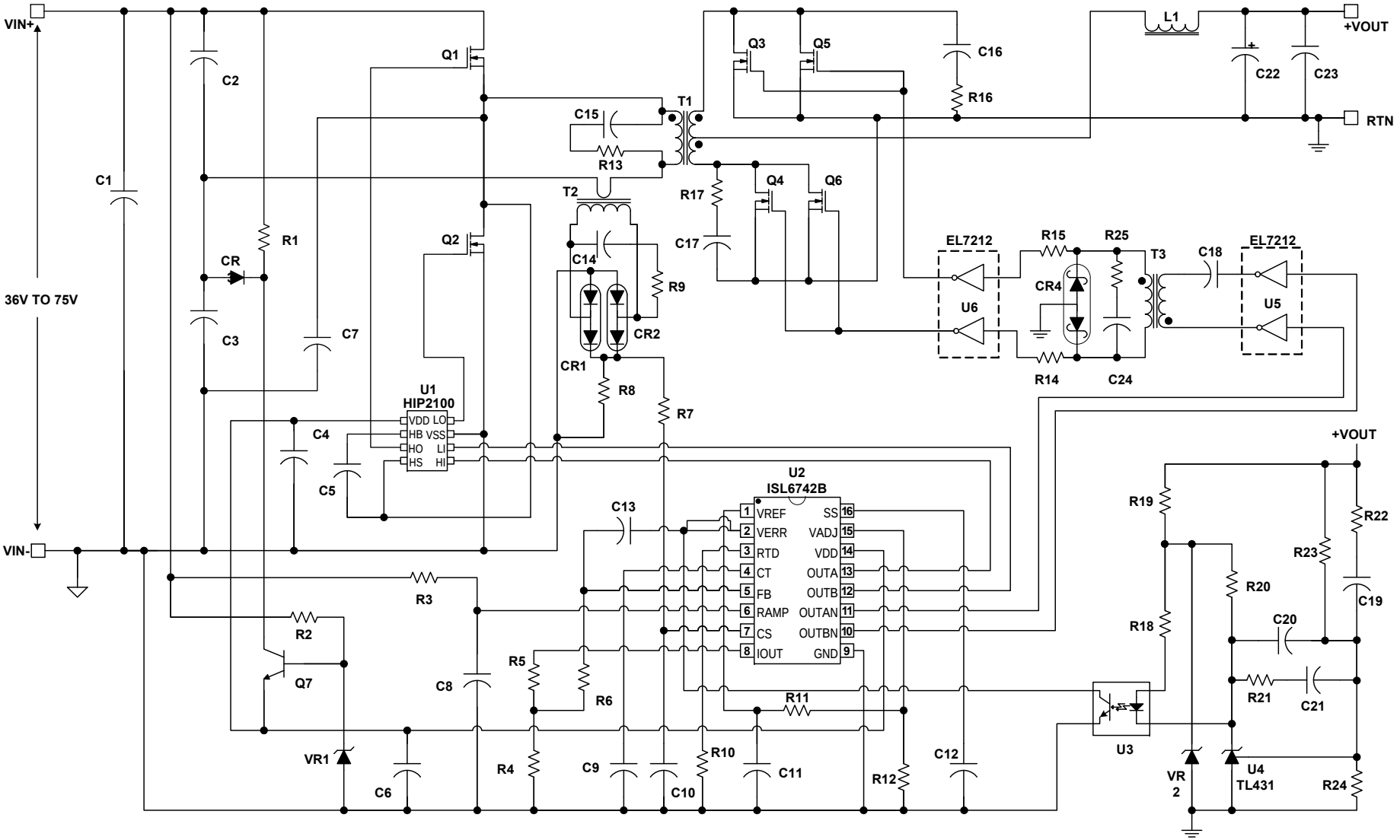
Pin Descriptions (Continued)

PIN #	SYMBOL	DESCRIPTION
14	VDD	VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a 0.1µF or larger high frequency ceramic capacitor as close to the VDD and GND pins as possible. VDD is monitored for supply voltage undervoltage lock-out (UVLO). The start and stop thresholds track each other resulting in relatively constant hysteresis.
15	VADJ	A 0V to 5V control voltage applied to this input sets the relative delay or advance between OUTA/OUTB and OUTAN/OUTBN. Voltages below 2.425V result in OUTAN/OUTBN being advanced relative to OUTA/OUTB. Voltages above 2.575V result in OUTAN/OUTBN being delayed relative to OUTA/OUTB. A voltage of 2.50V ±75mV results in zero phase difference. A weak internal 50% divider from VREF results in no phase delay if this input is left floating. The range of phase delay/advance is either zero or 40ns to 300ns with the phase differential increasing as the voltage deviation from 2.5V increases. The relationship between the control voltage and phase differential is non-linear. The gain ($\Delta t/\Delta V$) is low for control voltages near 2.5V and rapidly increases as the voltage approaches the extremes of the control range. This behavior provides the designer increased accuracy when selecting a shorter delay/advance duration. When the PWM outputs are delayed relative to the SR outputs (VADJ < 2.425V), the delay time should not exceed 90% of the deadtime as determined by RTD and CT.
16	SS	Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start. The value of the capacitor determines the rate of increase of the duty cycle during start-up. Although no minimum value of capacitance is required, it is recommended that a value of at least 100pF be used for noise immunity. SS may also be used to inhibit the outputs by grounding through a small transistor in an open collector/drain configuration.

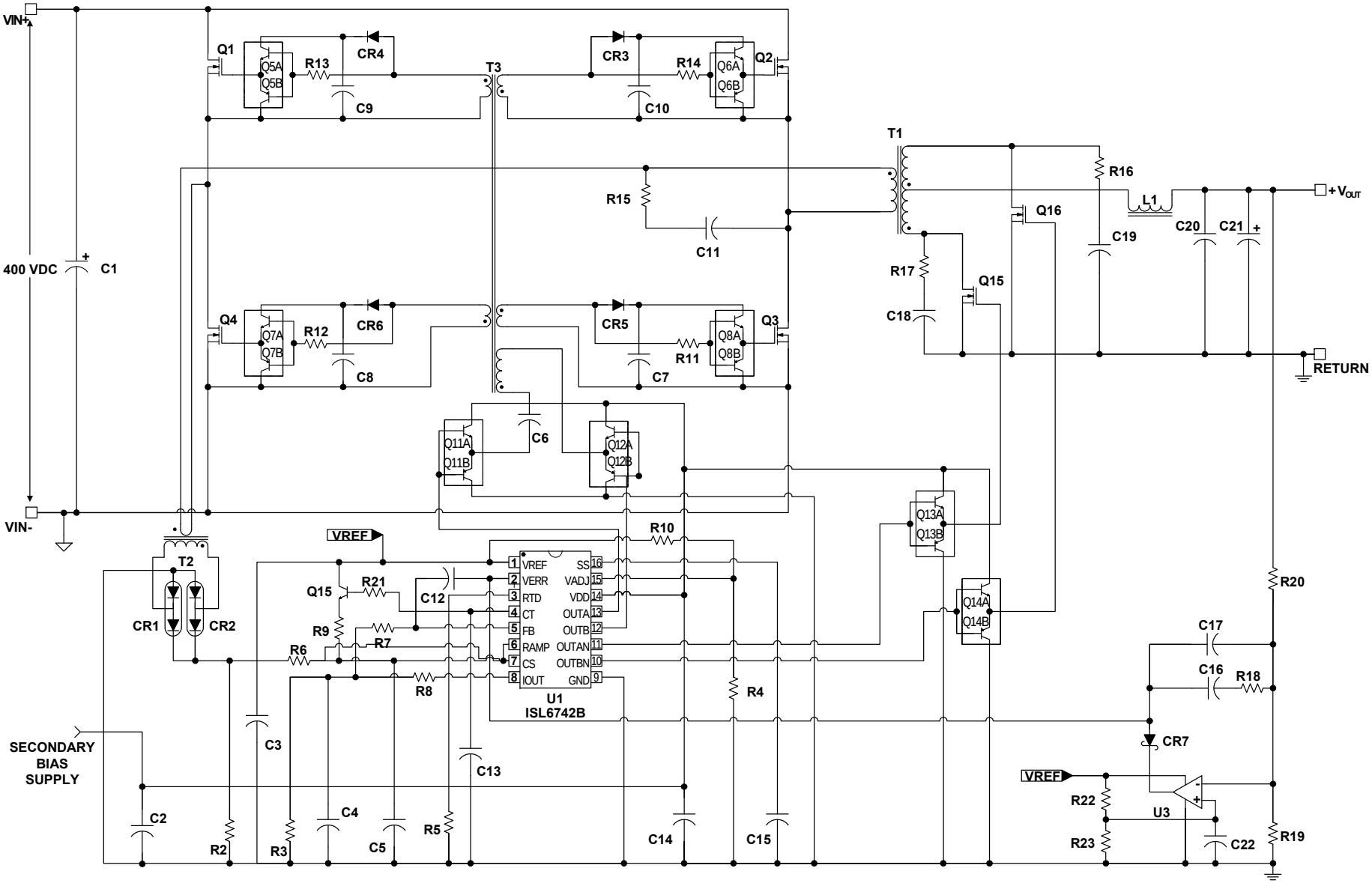
Functional Block Diagram



Typical Application - Telecom Primary Side Control Half-Bridge Converter with Synchronous Rectification



Typical Application - High Voltage Input Secondary Side Control Full-Bridge Converter



Absolute Maximum Ratings (Note 4)

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUTxx . . . . . GND - 0.3V to V_{DD}
Signal Pins. . . . . GND - 0.3V to V_{REF} + 0.3V
VREF . . . . . .GND - 0.3V to 6.0V
Peak GATE Current 0.1A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7). 2000V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93). 1000V
Machine Model (Per EIA/JESD22-A115-A) 75V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Lead QSOP (Notes 5, 6)	90	48

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
Supply Voltage Range (Typical). . . . . 9VDC to 16VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. All voltages are with respect to GND.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 5, "Typical Application - Telecom Primary Side Control Half-Bridge Converter with Synchronous Rectification" on page 6 and "Typical Application - High Voltage Input Secondary Side Control Full-Bridge Converter" on page 7. 9V < VDD < 16V, RTD = 10.0kΩ, CT = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY VOLTAGE					
Supply Voltage		-	-	**20**	V
Start-Up Current, I_{DD}	VDD = 5.0V	-	175	**400**	µA
Operating Current, I_{DD}	R_{LOAD}, C_{OUT} = 0	-	7.5	**12.0**	mA
UVLO START Threshold		**8.00**	8.75	**9.00**	V
UVLO STOP Threshold		**6.50**	7.00	**7.50**	V
Hysteresis		-	1.75	-	V
REFERENCE VOLTAGE					
Overall Accuracy	I_{VREF} = 0mA to 10mA	**4.850**	5.000	**5.150**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 8)	-	3	-	mV
Operational Current (Source)		**-10**	-	-	mA
Operational Current (Sink)		**5**	-	-	mA
Current Limit	VREF = 4.00V	**-15**	-	**-100**	mA
CURRENT SENSE					
Current Limit Threshold	VERR = VREF	**0.97**	1.00	**1.03**	V
CS to OUT Delay	Excl. LEB (Note 8)	-	35	**50**	ns
Leading Edge Blanking (LEB) Duration	(Note 8)	**50**	70	**100**	ns
CS to OUT Delay + LEB	T_A = +25°C	-	-	130	ns
CS Sink Current Device Impedance	V_{CS} = 0.7V	-	-	**20**	Ω
Input Bias Current	V_{CS} = 0.3V	**-1.0**	-	**1.0**	µA
IOUT Sample and Hold Buffer Amplifier Gain	T_A = +25°C	4.00	4.09	4.15	V/V
IOUT Sample and Hold VOH	V_{CS} = 1.00V, I_{LOAD} = -300µA	**3.9**	-	-	V
IOUT Sample and Hold VOL	V_{CS} = 0.00V, I_{LOAD} = 10µA	-	-	**0.3**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 5, "Typical Application - Telecom Primary Side Control Half-Bridge Converter with Synchronous Rectification" on page 6 and "Typical Application - High Voltage Input Secondary Side Control Full-Bridge Converter" on page 7. 9V < VDD < 16V, RTD = 10.0kΩ, CT = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
RAMP					
RAMP Sink Current Device Impedance	V_{RAMP} = 0.2V	-	-	**20**	Ω
RAMP to PWM Comparator Offset	T_A = +25°C	65	80	95	mV
Bias Current	V_{RAMP} = 0.3V	**-5.0**	-	**-2.0**	µA
Clamp Voltage	(Note 8)	**6.5**	-	**8.0**	V
SOFT-START					
Charging Current	SS = 3V	**-60**	-70	**-80**	µA
SS Clamp Voltage		**4.410**	4.500	**4.590**	V
SS Discharge Current	SS = 2V	**10**	-	-	mA
Reset Threshold Voltage	T_A = +25°C	0.23	0.27	0.33	V
ERROR AMPLIFIER					
Input Common Mode (CM) Range	(Note 8)	**0**	-	**VREF**	V
GBWP	(Note 8)	**5**	-	-	MHz
VERR VOL	I_{LOAD} = 2mA	-	-	**0.4**	V
VERR VOH	I_{LOAD} = 0mA	**4.20**	-	-	V
VERR Pull-Up Current Source	VERR = 2.50V	**0.8**	1.0	**1.3**	mA
EA Reference	T_A = +25°C	0.594	0.600	0.606	V
EA Reference + EA Input Offset Voltage		**0.590**	0.600	**0.612**	V
PULSE WIDTH MODULATOR					
Minimum Duty Cycle	VERR < 0.6V	-	-	**0**	%
Maximum Duty Cycle (Per Half-cycle)	VERR = 4.20V, V_{RAMP} = 0V, V_{CS} = 0V (Note 9)	-	94	-	%
	RTD = 2.00kΩ, CT = 220pF	-	97	-	%
	RTD = 2.00kΩ, CT = 470pF	-	99	-	%
Zero Duty Cycle VERR Voltage		**0.85**	-	**1.20**	V
VERR to PWM Comparator Input Offset	T_A = +25°C	0.7	0.8	0.9	V
VERR to PWM Comparator Input Gain		**0.31**	0.33	**0.35**	V/V
Common Mode (CM) Input Range	(Note 8)	**0**	-	**4.45**	V
OSCILLATOR					
Frequency Accuracy, Overall	(Note 8)	**165**	183	**201**	kHz
		-10	-	**+10**	%
Frequency Variation with VDD	T_A = +25°C, $(F_{20V} - F_{10V})/F_{10V}$	-	0.3	1.7	%
Temperature Stability	VDD = 10V, $\lvert F_{-40°C} - F_{0°C} \rvert / F_{0°C}$ (Note 8)	-	4.5	-	%
	$\lvert F_{0°C} - F_{105°C} \rvert / F_{25°C}$ (Note 8)	-	1.5	-	%
Charge Current	T_A = +25°C, V_{CS} = 1.8V	-189	-200	-211	µA
Discharge Current Gain		**19**	21	**23**	µA/µA
CT Valley Voltage	Static Threshold	**0.75**	0.80	**0.88**	V
CT Peak Voltage	Static Threshold	**2.75**	2.80	**2.88**	V
CT Pk-Pk Voltage	Static Value	**1.92**	2.00	**2.05**	V
RTD Voltage		**1.97**	2.00	**2.03**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 5, "Typical Application - Telecom Primary Side Control Half-Bridge Converter with Synchronous Rectification" on page 6 and "Typical Application - High Voltage Input Secondary Side Control Full-Bridge Converter" on page 7. 9V < VDD < 16V, RTD = 10.0kΩ, CT = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
OUTPUT					
High Level Output Voltage (VOH)	I_{OUT} = -10mA, VDD - VOH	-	0.5	**1.0**	V
Low Level Output Voltage (VOL)	I_{OUT} = 10mA, VOL - GND	-	0.5	**1.0**	V
Rise Time	C_{OUT} = 220pF, VDD = 15V (Note 8)	-	110	**200**	ns
Fall Time	C_{OUT} = 220pF, VDD = 15V (Note 8)	-	90	**150**	ns
UVLO Output Voltage Clamp (Note 8)	VDD = 7V, I_{LOAD} = 1mA (Note 10)	-	-	**1.25**	V
Output Delay/Advance Range OUTAN/OUTBN Relative to OUTA/OUTB	V_{ADJ} = 2.50V (Note 8)	-	-	**3**	ns
	V_{ADJ} < 2.425V	**-40**	-	**-300**	ns
	V_{ADJ} > 2.575V	**40**	-	**300**	ns
Delay Control Voltage Range OUTAN/OUTBN Relative to OUTA/OUTB	OUTxN Delayed	**2.575**	-	**5.000**	V
	OUTx Delayed	**0**	-	**2.425**	V
VADJ Delay Time	T_A = +25°C (OUTx Delayed) (Note 11)				
	VADJ = 0	280	300	320	ns
	VADJ = 0.5V	92	105	118	ns
	VADJ = 1.0V	61	70	80	ns
	VADJ = 1.5V	48	55	65	ns
	VADJ = 2.0V	41	50	58	ns
	T_A = +25°C (OUTxN Delayed)				
	VADJ = VREF	280	300	320	ns
	VADJ = VREF - 0.5V	86	100	114	ns
	VADJ = VREF - 1.0V	59	68	77	ns
	VADJ = VREF - 1.5V	47	55	62	ns
	VADJ = VREF - 2.0V	41	48	55	ns
THERMAL PROTECTION					
Thermal Shutdown	(Note 8)	**130**	140	**150**	°C
Thermal Shutdown Clear	(Note 8)	**115**	125	**135**	°C
Hysteresis, Internal Protection	(Note 8)	-	15	-	°C

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Limits established by characterization and are not production tested.
9. This is the maximum duty cycle achievable using the specified values of RTD and CT. Larger or smaller maximum duty cycles may be obtained using other values for these components. See Equations 1 through 3.
10. Adjust VDD below the UVLO stop threshold prior to setting at 7V.
11. When OUTx is delayed relative to OUTLxN (VADJ < 2.425V), the delay duration as set by VADJ should not exceed 90% of the CT discharge time (deadtime) as determined by CT and RTD.

Typical Performance Curves

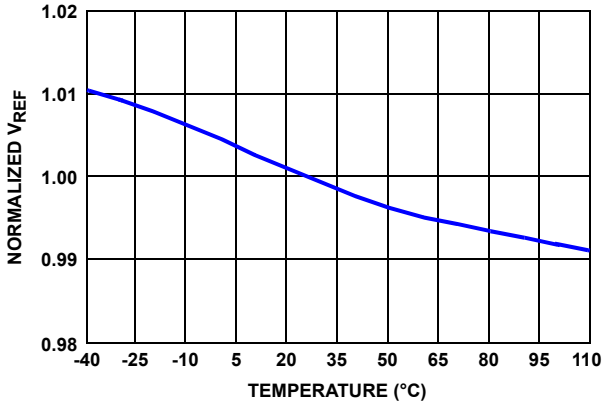


FIGURE 1. REFERENCE VOLTAGE vs TEMPERATURE

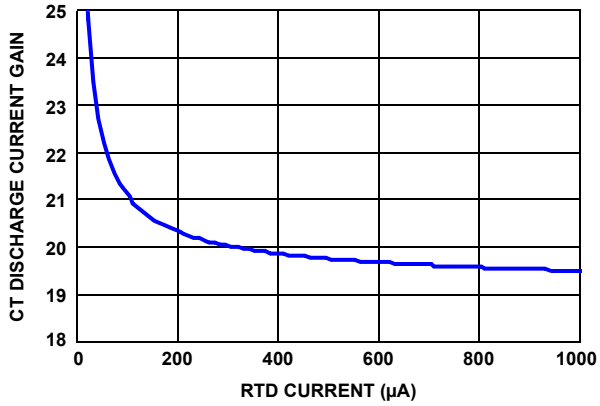


FIGURE 2. CT DISCHARGE CURRENT GAIN vs RTD CURRENT

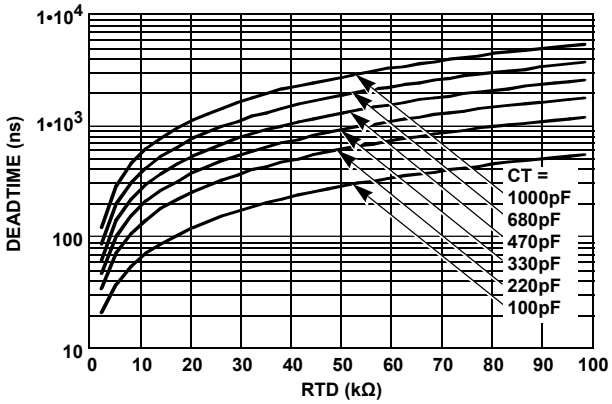


FIGURE 3. DEADTIME (DT) vs CAPACITANCE

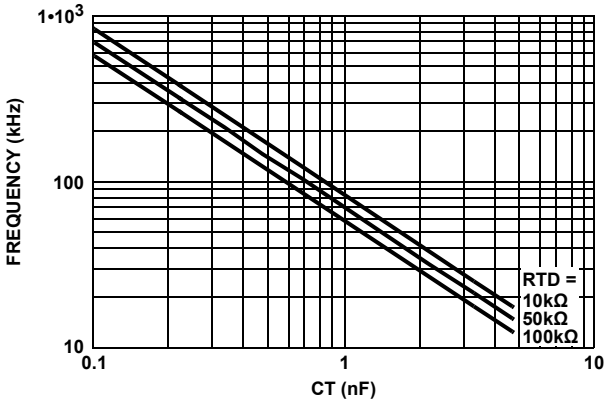


FIGURE 4. CAPACITANCE vs FREQUENCY

Functional Description

Features

The ISL6742B PWM is an excellent choice for low cost bridge and push-pull topologies in applications requiring accurate duty cycle and deadtime control. With its many protection and control features, a highly flexible design with minimal external components is possible. Among its many features are current- or voltage-mode control, adjustable soft-start, peak and average overcurrent protection, thermal protection, synchronous rectifier outputs with variable delay/advance timing, and adjustable oscillator frequency.

Oscillator

The ISL6742B oscillator, with a programmable frequency range to 2MHz, is set with only an external resistor and capacitor.

The switching period is the sum of the timing capacitor charge and discharge durations. The charge duration is determined by CT and a fixed 200µA internal current source. The discharge duration is determined by RTD and CT.

$$t_C \approx 11.5 \cdot 10^3 \cdot CT \quad S \qquad \text{(EQ. 1)}$$

$$t_D \approx (0.06 \cdot RTD \cdot CT) + 50 \cdot 10^{-9} \quad S \qquad \text{(EQ. 2)}$$

$$t_{SW} = t_C + t_D = \frac{1}{F_{SW}} \quad S \qquad \text{(EQ. 3)}$$

where t_C and t_D are the charge and discharge times, respectively, t_{SW} is the oscillator period, and F_{SW} is the oscillator frequency. Since the ISL6742B is a double-ended controller, one output switching cycle requires two oscillator cycles. The actual charge and discharge times will be slightly longer than calculated due to internal propagation delays of approximately 10ns/transition. This delay adds directly to the switching duration, but also causes slight overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low discharge currents are used, there will be increased error due to the input impedance at the CT pin.

The maximum duty cycle, D, and percent deadtime, DT, can be calculated from:

$$D = \frac{t_C}{t_{SW}} \quad \text{(EQ. 4)}$$

$$DT = 1 - D \quad \text{(EQ. 5)}$$

Soft-Start Operation

The ISL6742B features a soft-start using an external capacitor in conjunction with an internal current source. Soft-start reduces component stresses and surge currents during start-up.

Upon start-up, the soft-start circuitry limits the error voltage input (VERR) to a value equal to the soft-start voltage. The output pulse width increases as the soft-start capacitor voltage increases. This has the effect of increasing the duty cycle from zero to the regulation pulse width during the soft-start period. When the soft-start voltage exceeds the error voltage, soft-start is completed. Soft-start occurs during start-up and after recovery from a fault condition. The soft-start charging period may be calculated using Equation 6:

$$t = 64.3 \cdot C \quad ms \quad \text{(EQ. 6)}$$

where t is the charging period in ms and C is the value of the soft-start capacitor in µF. The soft-start duration experienced by the power supply will be less than or equal to this value, depending on when the feedback loop takes control.

The soft-start voltage is clamped to 4.50V with an overall tolerance of 2%. It is suitable for use as a “soft-started” reference provided the current draw is kept well below the 70µA charging current.

The outputs may be inhibited by using the SS pin as a disable input. Pulling SS below 0.25V forces all outputs low. An open collector/drain configuration may be used to couple the disable signal to the SS pin.

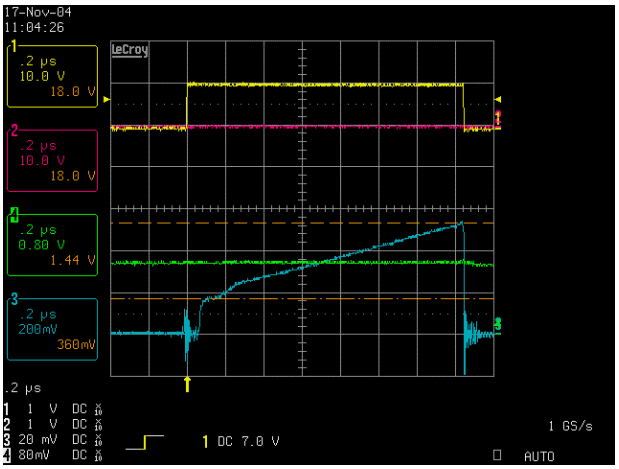
Gate Drive

The ISL6742B outputs are capable of sourcing and sinking 10mA (at rated VOH, VOL) and are intended to be used in conjunction with integrated FET drivers or discrete bipolar totem pole drivers. The typical ON-resistance of the outputs is 50Ω.

Overcurrent Operation

Two overcurrent protection mechanisms are available to the power supply designer. The first method is cycle-by-cycle peak overcurrent protection, which provides fast response. The second method is a slower, averaging method, which produces constant or “brick-wall” current limit behavior. If voltage-mode control is used, the average overcurrent protection also maintains flux balance in the transformer by maintaining duty cycle symmetry between half-cycles.

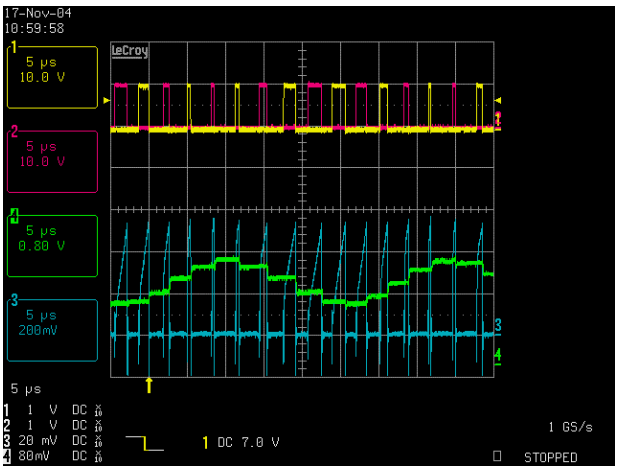
The current sense signal applied to the CS pin connects to the peak current comparator and a sample and hold averaging circuit. After a 70ns leading edge blanking (LEB) delay, the current sense signal is actively sampled during the on-time, the average current for the cycle is determined, and the result is amplified by 4x and output on the IOUT pin. If an RC filter is placed on the CS input, its time constant should not exceed ~50ns or significant error may be introduced on IOUT.



CHANNEL 1 (YELLOW): OUTA CHANNEL 2 (RED): OUTB
CHANNEL 3 (BLUE): CS CHANNEL 4 (GREEN): IOUT

FIGURE 5. CS INPUT vs IOUT

Figure 5 shows the relationship between the CS signal and IOUT under steady state conditions. IOUT is 4x the average of CS. Figure 6 shows the dynamic behavior of the current averaging circuitry when CS is modulated by an external sine wave. Notice IOUT is updated by the sample and hold circuitry at the termination of the active output pulse.



CHANNEL 1 (YELLOW): OUTA CHANNEL 2 (RED): OUTB
CHANNEL 3 (BLUE): CS CHANNEL 4 (GREEN): IOUT

FIGURE 6. DYNAMIC BEHAVIOR OF CS vs IOUT

The average current signal on IOUT remains accurate provided that the output inductor current is continuous (CCM operation). Once the inductor current becomes discontinuous (DCM operation), IOUT represents 1/2 the peak inductor current rather than the average current. This occurs because the sample and hold circuitry is active only during the on-time of the switching cycle. It is unable to detect when the inductor current reaches zero during the off-time.

If average overcurrent limit is desired, IOUT may be used with the available error amplifier of the ISL6742B. Typically, IOUT is divided down and filtered as required to achieve the desired amplitude. The resulting signal is input to the current error

amplifier (IEA). The IEA is similar to the voltage EA found in most PWM controllers, except it cannot source current. Instead, VERR has a separate internal 1mA pull-up current source.

Configure the IEA as an integrating (Type I) amplifier using the internal 0.6V reference. The voltage applied at FB is integrated against the 0.6V reference. The resulting signal, VERR, is applied to the PWM comparator where it is compared to the sawtooth voltage on RAMP. If FB is less than 0.6V, the IEA will be open loop (can't source current), VERR will be at a level determined by the voltage loop, and the duty cycle is unaffected. As the output load increases, IOUT will increase, and the voltage applied to FB will increase until it reaches 0.6V. At this point the IEA will reduce VERR as required to maintain the output current at the level that corresponds to the 0.6V reference. When the output current again drops below the average current limit threshold, the IEA returns to an open loop condition, and the duty cycle is again controlled by the voltage loop.

The average current control loop behaves much the same as the voltage control loop found in typical power supplies except it regulates current rather than voltage.

The EA available on the ISL6742B may also be used as the voltage EA for the voltage feedback control loop rather than the current EA as described previously. An external op amp may be used as either the current or voltage EA providing the circuit is not allowed to source current into VERR. The external EA must only sink current, which may be accomplished by adding a diode in series with its output.

The 4x gain of the sample and hold buffer allows a range of 150mV to 1000mV peak on the CS signal, depending on the resistor divider placed on IOUT. The overall bandwidth of the average current loop is determined by the integrating current EA compensation and the divider on IOUT.

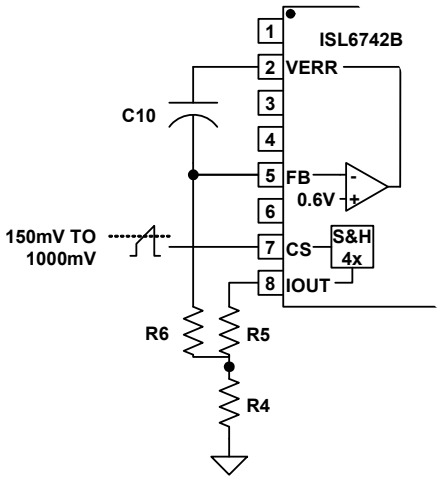


FIGURE 7. AVERAGE OVERCURRENT IMPLEMENTATION

The current EA crossover frequency, assuming R6 >> (R4||R5), is expressed in Equation 7:

$$f_{CO} = \frac{1}{2\pi \cdot R6 \cdot C10} \quad Hz \qquad \text{(EQ. 7)}$$

where f_{CO} is the crossover frequency. A capacitor in parallel with R4 may be used to provide a double-pole roll-off.

The average current loop bandwidth is normally set to be much less than the switching frequency, typically less than 5kHz and often as slow as a few hundred hertz or less. This is especially useful if the application experiences large surges. The average current loop can be set to the steady state overcurrent threshold and have a time response that is longer than the required transient. The peak current limit can be set higher than the expected transient so that it does not interfere with the transient, but still protects for short-term larger faults. In essence, a 2-stage overcurrent response is possible.

The peak overcurrent behavior is similar to most other PWM controllers. If the peak current exceeds 1V, the active output pulse is terminated immediately.

If voltage-mode control is used in a bridge topology, it should be noted that peak current limit results in inherently unstable operation. DC blocking capacitors used in voltage-mode bridge topologies become unbalanced, as does the flux in the transformer core. The average overcurrent circuitry prevents this behavior by maintaining symmetric duty cycles for each half-cycle. If the average current limit circuitry is not used, a latching overcurrent shutdown method using external components is recommended.

The CS to output propagation delay is increased by the leading edge blanking (LEB) interval. The effective delay is the sum of the two delays and is 130ns maximum.

Voltage Feed-Forward Operation

Voltage feed-forward is a technique used to regulate the output voltage for changes in input voltage without the intervention of the control loop. Voltage feed-forward is often implemented in voltage-mode control loops, but is redundant and unnecessary in peak current-mode control loops.

Voltage feed-forward operates by modulating the sawtooth ramp in direct proportion to the input voltage. Figure 8 demonstrates the concept.

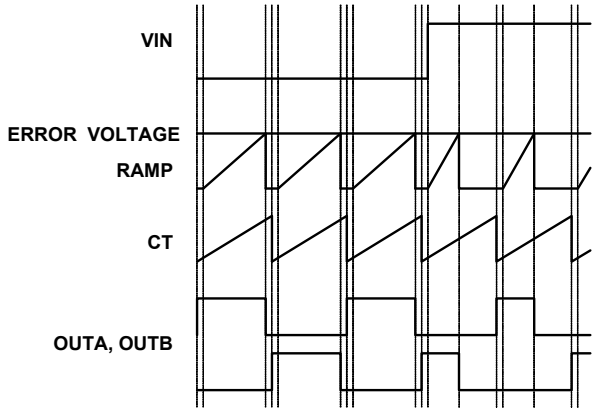


FIGURE 8. VOLTAGE FEED FORWARD BEHAVIOR

Input voltage feed-forward may be implemented using the RAMP input. An RC network connected between the input voltage and ground, as shown in Figure 9, generates a voltage ramp proportional to the amplitude of the source voltage. At the termination of the active output pulse, RAMP is discharged to ground so that a repetitive sawtooth waveform is created. The

RAMP waveform is compared to the VERR voltage to determine duty cycle. The selection of the RC components depends upon the desired input voltage operating range and the frequency of the oscillator. In typical applications, the RC components are selected so that the ramp amplitude reaches 1V at minimum input voltage within the duration of one half-cycle.

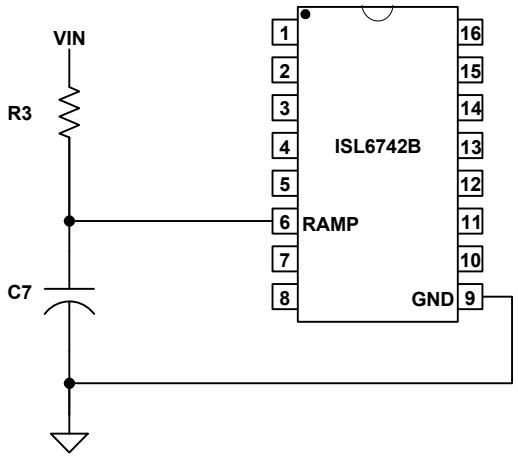


FIGURE 9. VOLTAGE FEED-FORWARD CONTROL

Referring to Figure 9, the charging time of the ramp capacitor is expressed in Equation 8:

$$t = -R3 \cdot C7 \cdot \ln\left(1 - \frac{V_{RAMP(PEAK)}}{V_{IN(MIN)}}\right) \quad s \qquad \text{(EQ. 8)}$$

For optimum performance, the maximum value of the capacitor should be limited to 10nF. The DC current through the resistor should be limited to 3mA. For example, if the oscillator frequency is 400kHz, the minimum input voltage is 300V and a 4.7nF ramp capacitor is selected. The value of the resistor can be determined by rearranging Equation 8.

$$R3 = \frac{-t}{C7 \cdot \ln\left(1 - \frac{V_{RAMP(PEAK)}}{V_{IN(MIN))}}\right)} = \frac{-2.5 \cdot 10^{-6}}{4.7 \cdot 10^{-9} \cdot \ln\left(1 - \frac{1}{300}\right)}$$

$$= 159k\Omega \qquad \text{(EQ. 9)}$$

where t is equal to the oscillator period minus the deadtime. If the deadtime is short relative to the oscillator period, it can be ignored for this calculation.

When implemented, the voltage feed-forward feature also provides a volt-second clamp on the transformer. The maximum duty cycle is determined by the lesser of the oscillator period or the RAMP charge time. As the input voltage increases, the RAMP charge time decreases, limiting the duty cycle proportionately.

If feed-forward operation is not desired, the RC network may be connected to VREF or a buffered CT signal rather than the input voltage. Regardless, a sawtooth waveform must be generated on RAMP as it is required for proper PWM operation.

Implementing Synchronization

Synchronization to an external clock signal may be accomplished in the same manner as many PWM controllers that do not have a separate synchronization input. By injecting a short pulse across a small resistor in series with the timing capacitor, the oscillator sawtooth waveform may be terminated prematurely.

The injected pulse width should be narrower than the sawtooth discharge duration.

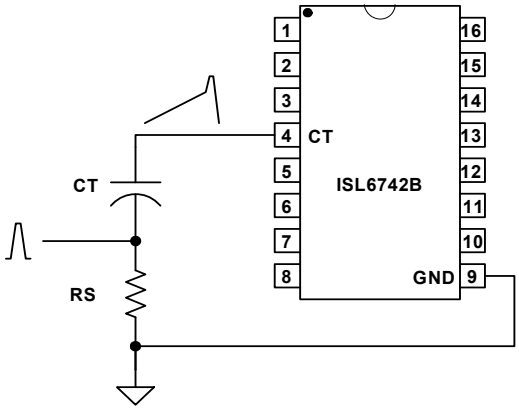


FIGURE 10. SYNCHRONIZATION TO AN EXTERNAL CLOCK

Synchronous Rectifier Outputs and Control

The ISL6742B provides double-ended PWM outputs, OUTA and OUTB, and synchronous rectifier (SR) outputs, OUTAN and OUTBN. The SR outputs are the complements of the PWM outputs. It should be noted that complemented outputs are used in conjunction with the opposite PWM output, i.e., OUTA and OUTBN are paired together and OUTB and OUTAN are paired together.

Referring to Figure 11, the SRs alternate between being both on during the free-wheeling portion of the cycle (OUTA/OUTB off), and one or the other being off when OUTA or OUTB is on. If OUTA is on, its corresponding SR must also be on, indicating that OUTBN is the correct SR control signal. Likewise, if OUTB is on, its corresponding SR must also be on, indicating that OUTAN is the correct SR control signal.

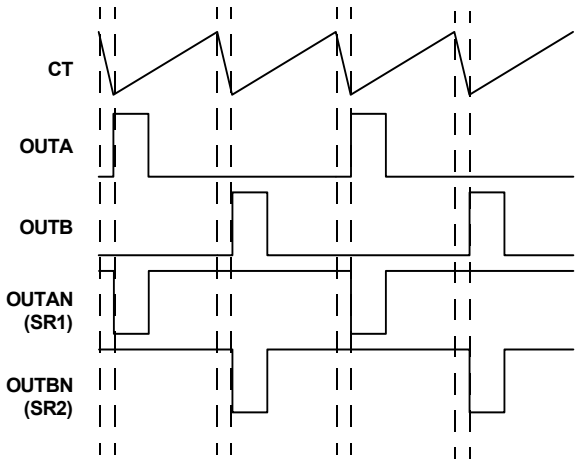


FIGURE 11. BASIC WAVEFORM TIMING

A useful feature of the ISL6742B is the ability to vary the phase relationship between the PWM outputs (OUTA, OUTB) and their complements (OUTAN, OUTBN) by ±300ns. This feature allows the designer to compensate for differences in the signal

propagation delays between the PWM FETs and the SR FETs. A voltage applied to VADJ controls the phase relationship. Figures 12 and 13 demonstrate the delay relationships.

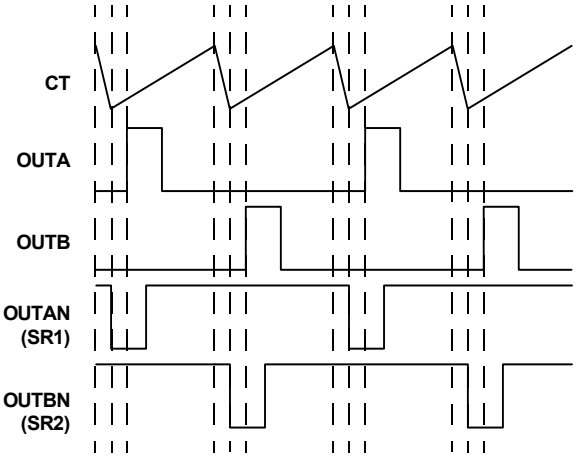


FIGURE 12. WAVEFORM TIMING WITH PWM OUTPUTS DELAYED, 0V < VADJ < 2.425V

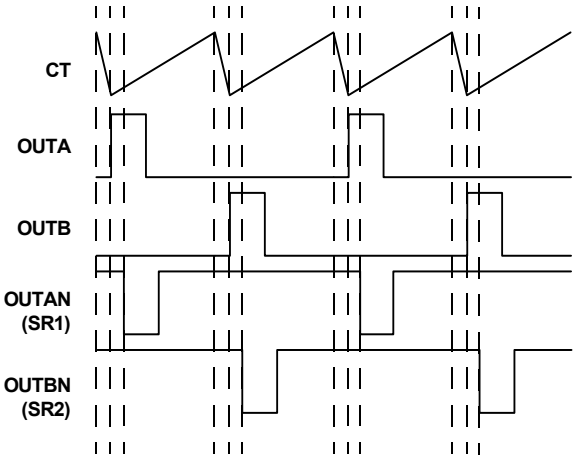


FIGURE 13. WAVEFORM TIMING WITH SR OUTPUTS DELAYED, 2.575V < VADJ < 5.00V

Setting VADJ to VREF/2 results in no delay on any output. The no delay voltage has a ±75mV tolerance window. Control voltages below the VREF/2 zero delay threshold cause the PWM outputs, OUTA/OUTB, to be delayed. Control voltages greater than the VREF/2 zero delay threshold cause the SR outputs, OUTAN/OUTBN, to be delayed. It should be noted that when the PWM outputs, OUTA/OUTB, are delayed, the CS to output propagation delay is increased by the amount of the added delay.

The delay feature is provided to compensate for mismatched propagation delays between the PWM and SR outputs as may be experienced when one set of signals crosses the primary-secondary isolation boundary. If required, individual output pulses may be stretched or compressed as required using external resistors, capacitors, and diodes.

Slope Compensation

Peak current-mode control requires slope compensation to improve noise immunity, particularly at lighter loads, and to prevent current loop instability, particularly for duty cycles greater than 50%. Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, F_m, without slope compensation, is expressed in Equation 10:

$$F_m = \frac{1}{S_n S_n} \quad \text{(EQ. 10)}$$

where S_n is the slope of the sawtooth signal and t_{SW} is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 11:

$$F_m = \frac{1}{(S_n + S_e)t_{SW}} = \frac{1}{m_c S_n t_{SW}} \quad \text{(EQ. 11)}$$

where S_e is slope of the external ramp and:

$$m_c = 1 + \frac{S_e}{S_n} \quad \text{(EQ. 12)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at half the oscillator frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for Q > 1, and under-damped for Q < 1. An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D)-0.5)} \quad \text{(EQ. 13)}$$

where D is the percent of on-time during a half cycle (half period duty cycle). Setting Q = 1 and solving for S_e yields Equation 14:

$$S_e = S_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1-D} - 1\right) \quad \text{(EQ. 14)}$$

Since S_n and S_e are the on-time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON}.

$$V_e = V_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1-D} - 1\right) \quad \text{(EQ. 15)}$$

where V_n is the change in the current feedback signal during the on time and V_e is the voltage that must be added by the external ramp.

V_n can be solved for in terms of input voltage, current transducer components, and output inductance yielding Equation 16:

$$V_e = \frac{t_{SW} \cdot V_O \cdot R_{CS}}{N_{CT} \cdot L_O} \cdot \frac{N_S}{N_P}\left(\frac{1}{\pi} + D - 0.5\right) \quad V \quad \text{(EQ. 16)}$$

where R_{CS} is the current sense burden resistor, N_{CT} is the current transformer turns ratio, L_O is the output inductance, V_O is the output voltage, and N_S and N_P are the secondary and primary turns, respectively.

The current sense signal, which represents the inductor current after it has been reflected through the isolation and current sense transformers, and passed through the current sense burden resistor, is expressed in Equation 17:

$$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P \cdot N_{CT}}\left(I_O + \frac{D \cdot t_{SW}}{2L_O}\left(V_{IN} \cdot \frac{N_S}{N_P} - V_O\right)\right) \quad V \qquad \text{(EQ. 17)}$$

where V_{CS} is the voltage across the current sense resistor and I_O is the output current at current limit.

Since the peak current limit threshold is 1V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold.

$$V_e + V_{CS} = 1 \qquad \text{(EQ. 18)}$$

Substituting Equations 16 and 17 into Equation 18 and solving for R_{CS} yields Equation 19:

$$R_{CS} = \frac{N_P \cdot N_{CT}}{N_S} \cdot \frac{1}{I_O + \frac{V_O}{L_O} t_{SW}\left(\frac{1}{\pi} + \frac{D}{2}\right)} \quad \Omega \qquad \text{(EQ. 19)}$$

For simplicity, idealized components have been used for this discussion, but the effect of magnetizing inductance must be considered when determining the amount of external ramp to add. Magnetizing inductance provides a degree of slope compensation and reduces the amount of external ramp required. The magnetizing inductance adds primary current in excess of what is reflected from the inductor current in the secondary.

$$\Delta I_P = \frac{V_{IN} \cdot Dt_{SW}}{L_m} \quad A \qquad \text{(EQ. 20)}$$

where V_{IN} is the input voltage that corresponds to the duty cycle D and Lm is the primary magnetizing inductance. The effect of the magnetizing current at the current sense resistor, R_{CS}, is expressed in Equation 21:

$$\Delta V_{CS} = \frac{\Delta I_P \cdot R_{CS}}{N_{CT}} \quad V \qquad \text{(EQ. 21)}$$

If ΔV_{CS} is greater than or equal to Ve, then no additional slope compensation is needed and R_{CS} becomes Equation 22:

$$R_{CS} = \frac{N_{CT}}{\frac{N_S}{N_P} \cdot \left(I_O + \frac{Dt_{SW}}{2L_O} \cdot \left(V_{IN} \cdot \frac{N_S}{N_P} - V_O\right)\right) + \frac{V_{IN} \cdot Dt_{SW}}{L_m}} \qquad \text{(EQ. 22)}$$

If ΔV_{CS} is less than V_e, then Equation 19 is still valid for the value of R_{CS}, but the amount of slope compensation added by the external ramp must be reduced by ΔV_{CS}.

Adding slope compensation is accomplished in the ISL6742B using an external buffer and the CT signal. A typical application sums the buffered CT signal with the current sense feedback and applies the result to the CS pin as shown in Figure 14.

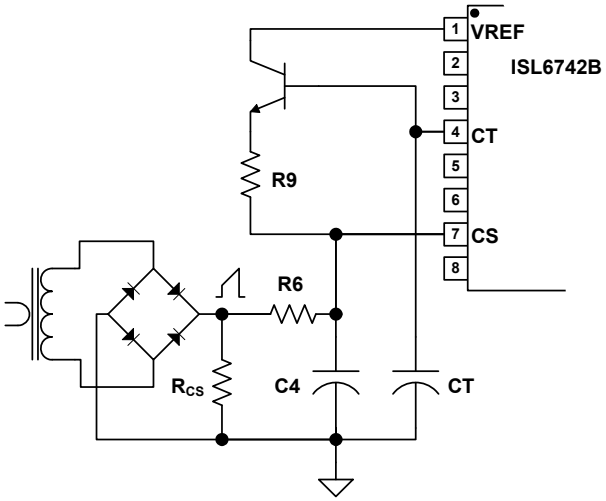


FIGURE 14. ADDING SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter (R6 and C4) placed on the CS pin, the value of R9 required to add the appropriate external ramp can be found by superposition.

$$V_e - \Delta V_{CS} = \frac{2D \cdot R6}{R6 + R9} \quad V \qquad \text{(EQ. 23)}$$

Rearranging to solve for R9 yields:

$$R9 = \frac{(2D - V_e + \Delta V_{CS}) \cdot R6}{V_e - \Delta V_{CS}} \quad \Omega \qquad \text{(EQ. 24)}$$

The value of R_{CS} determined in Equation 19 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 17. The divider created by R6 and R9 makes this necessary.

$$R'_{CS} = \frac{R6 + R9}{R9} \cdot R_{CS} \qquad \text{(EQ. 25)}$$

Example:

V_{IN} = 280V

V_O = 12V

L_O = 2.0µH

N_P/N_S = 20

Lm = 2mH

I_O = 55A

Oscillator Frequency, F_{SW} = 400kHz

Duty Cycle, D = 85.7%

N_{CT} = 50

R6 = 499Ω

Solve for the current sense resistor, R_{CS}, using Equation 19.

R_{CS} = 15.1Ω.

Determine the amount of voltage, V_e, that must be added to the current feedback signal using Equation 16.

V_e = 153mV

Next, determine the effect of the magnetizing current from Equation 21.

ΔV_{CS} = 91mV

Using Equation 24, solve for the summing resistor, R9, from CT to CS.

R9 = 13.2kΩ

Determine the new value of R_{CS}, R'_{CS}, using Equation 25.

R'_{CS} = 15.7Ω

Additional slope compensation may be considered for design margin. This discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from CT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into CT and will reduce the oscillator frequency.

Parallel Operation

Parallel operation of converters using the ISL6742B may be accomplished using the average current signal, IOUT. IOUT provides a very accurate representation of the output current and may be used for active current sharing with many sharing techniques commonly used including master-slave and average current sharing methods.

Since IOUT represents the average inductor current (CCM operation), sharing errors introduced by techniques using peak inductor current are reduced. In particular, the current sharing error introduced by mismatched switching frequencies is eliminated.

Figure 15 illustrates a master-slave current sharing method.

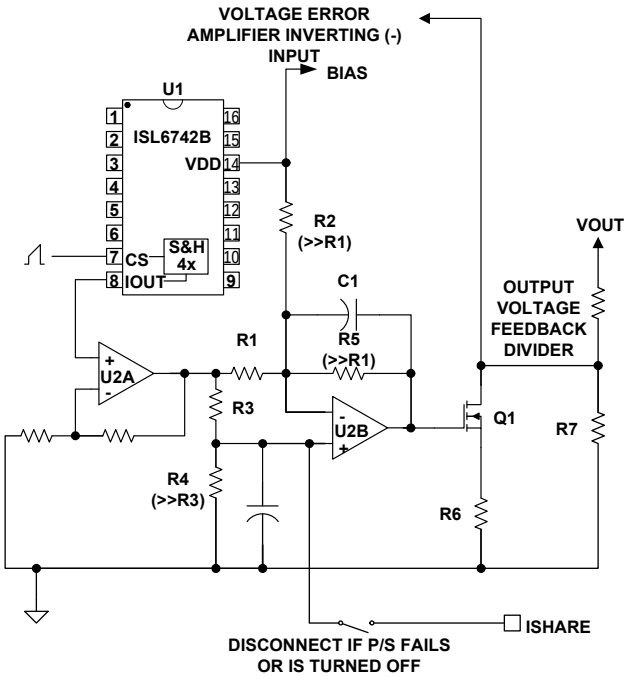


FIGURE 15. MASTER-SLAVE CURRENT SHARING USING AVERAGE CURRENT

In parallel and redundant applications, the IShare signals from each power supply are connected together. Each power supply produces a voltage proportional to its average output current on IOUT, and through limiting resistor R3, on IShare. The unit with the highest IShare signal (and highest output current) sources current onto the IShare Bus, and is identified as the master unit. The units with lower IShare signals do not source current onto IShare, and are identified as slave units. Each slave unit compares the master's IShare signal with its own, and if there is sufficient difference, turns Q1 on, which pulls down on the feedback voltage. Reducing the feedback voltage causes the output voltage to appear low; the feedback loop compensates by increasing the output voltage, and the output current increases. Each slave unit will increase its output voltage until its output current is nearly equal to that of the master.

The difference between the master's output current and that of a slave unit is set by R1 and R2. Some difference is required to prevent undesirable switching of master and slave roles. This difference also prevents operation of the current sharing circuitry when a power supply is operating stand alone.

The maximum output voltage that a slave can induce in its output is controlled by R6 and the output voltage feedback divider. Typically, the maximum allowed output voltage increase is limited to a few percent, but must be greater than the tolerance of the feedback and reference components and any distribution drops between units. If remote sensing is used, the adjustment range must also include the difference in distribution drops between the power supply outputs and the remote sensing location. The current limit circuit must limit the voltage change to less than the output overvoltage threshold or an overvoltage condition can be induced.

Amplifier U2A sets the scaling factor from IOUT to IShare and increases the current sourcing capability of IShare. U2B is a low bandwidth amplifier that sets the frequency response and gain of the current share circuitry. The current share bandwidth must be much lower than the voltage feedback loop bandwidth to ensure overall stability. The gain is set by R1 and R5, and the bandwidth by R5 and C1.

The disconnect in series with IShare may be omitted for power systems that do not require fault isolation. The disconnect switch is normally implemented with MOSFET or JFET devices.

Average Current Mode Control

The average current signal produced on IOUT may also be used for average current mode control rather than peak current mode control. There are many advantages to average current mode control, most notably, improved noise immunity and greater design flexibility of the current feedback loop compensation. Figure 16 portrays the concept.

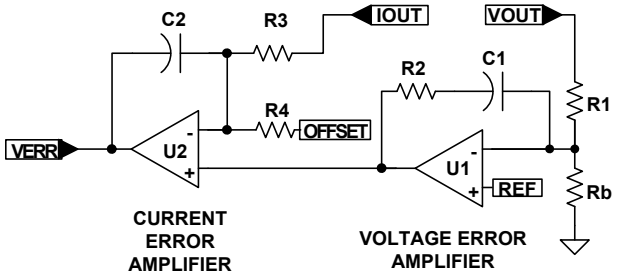


FIGURE 16. AVERAGE CURRENT MODE CONTROL

Instead of being compared to a peak current sense signal as it would be in a peak current mode control configuration, the voltage amplifier output is integrated against the average output current. The voltage loop compensation and the current loop compensation may be adjusted independently.

The voltage error amplifier programs the average output current of the supply, and its maximum output level determines the maximum output current. Either IOUT or the voltage EA output must be scaled appropriately to achieve the desired current limit setpoint. The offset voltage shown in Figure 16 must be provided to compensate for input offset voltage of the current amplifier to ensure that zero duty cycle operation is achievable.

Depending on the performance requirements of the control loop, compensation networks other than shown may be required.

Fault Conditions

A fault condition occurs if VREF or VDD fall below their undervoltage lockout (UVLO) thresholds or if the thermal protection is triggered. When a fault is detected, the soft-start capacitor is quickly discharged, and the outputs are disabled low. When the fault condition clears and the soft-start voltage is below the reset threshold, a soft-start cycle begins.

An overcurrent condition is not considered a fault and does not result in a shutdown.

Thermal Protection

Internal die over temperature protection is provided. An integrated temperature sensor protects the device should the junction temperature exceed +140°C. There is approximately +15°C of hysteresis.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. VDD and VREF should be bypassed directly to GND with good high frequency capacitance.

References

[1] Ridley, R., “A New Continuous-Time Model for Current Mode Control”, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 31, 2014	FN8565.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

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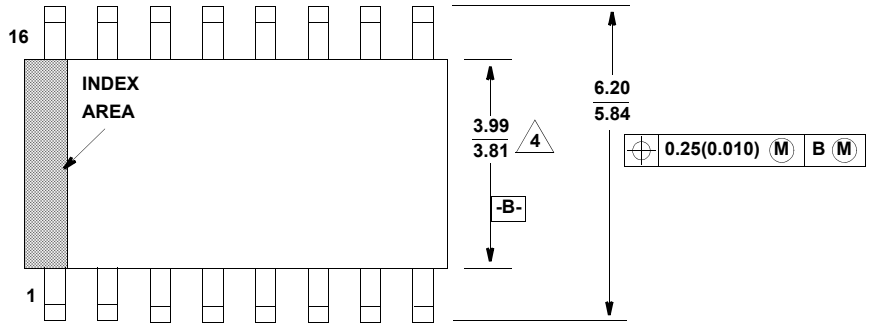
Package Outline Drawing

M16.15A

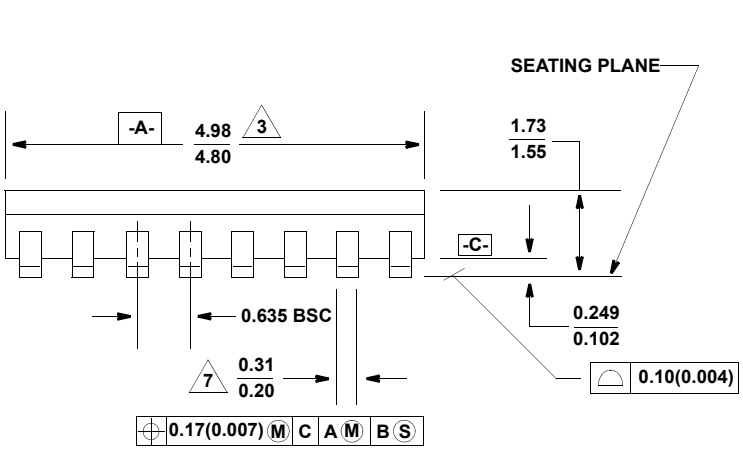
16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (QSOP/SSOP)

0.150" WIDE BODY

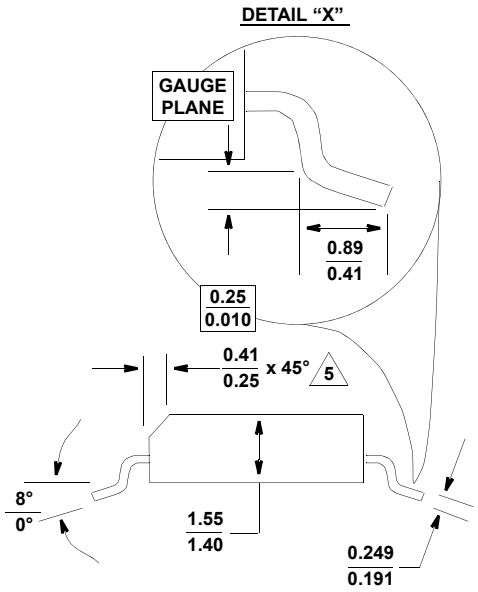
Rev 3, 8/12



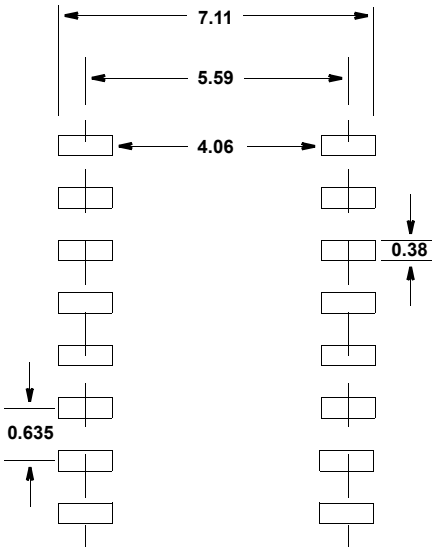
TOP VIEW



SIDE VIEW 1



SIDE VIEW 2



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Terminal numbers are shown for reference only.
7. Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
8. Controlling dimension: MILLIMETER.

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