40V 2.5A Regulator with Integrated High-side MOSFET for Synchronous Buck or Boost Buck Converter

ISL78201

The ISL78201 is an AEC-Q100 qualified 40V, 2.5A synchronous buck or boost buck controller with a high-side MOSFET and low-side driver integrated. In buck mode, the ISL78201 supports a wide input range of 3V to 40V. In boost-buck mode, the input range can be extended down to 2.5V and output regulation can be maintained when V_{IN} drops below V_{OUT}, enabling sensitive electronics to remain on during cold-cranking and start-stop applications.

The ISL78201 has a flexible selection of operation modes including forced PWM mode and an optional switch to PFM mode for light loads. In PFM mode, the quiescent input current is as low as 300µA and can be further reduced to 180µA with AUXVCC connected to V_{OUT} under 12V V_{IN} and 5V V_{OUT} application. The load boundary between PFM and PWM can be programmed to cover wide applications.

The low-side driver can be either used to drive an external low-side MOSFET for a synchronous buck, or left unused for a standard non-synchronous buck. The low-side driver can also be used to drive a boost converter as a pre-regulator that greatly expands the operating input voltage range down to 2.5V or lower (refer to "Typical Application Schematic III - Boost Buck Converters" on page 5).

The ISL78201 offers the most robust current protections. It uses peak current mode control with cycle-by-cycle current limiting. It is implemented with frequency foldback undercurrent limit condition; in addition, the hiccup overcurrent mode is also implemented to guarantee reliable operations under harsh short conditions. The ISL78201 has comprehensive protections against various faults including overvoltage and over-temperature protections, etc.

Features

- Buck Mode: input voltage range 3V to 40V (refer to "Input Voltage" on page 15 for more details)
- Boost mode expands operating input voltage lower than 2.5V (refer to "Input Voltage" on page 15 for more details)
- Selectable forced PWM mode or PFM mode
- 300µA IC quiescent current (PFM, no load); 180µA input quiescent current (PFM, no load, V_{OUT} tied to AUXVCC)
- Less than 5µA (MAX) shutdown input current (IC disabled)
- Operational topologies
  - Synchronous buck
  - Non-synchronous buck
  - Two stage boost buck
  - Non-inverting single inductor buck boost
- Programmable frequency from 200kHz - 2.2MHz and frequency synchronization capability
- ±1% Tight voltage regulation accuracy
- Reliable cycle-by-cycle overcurrent protection
  - Temperature compensated current sense
  - Programmable OC limit
  - Frequency foldback and hiccup mode protection
- 20 Ld HTSSOP package
- AEC-Q100 qualified
- Pb-free (RoHS compliant)

Applications

- Automotive applications
- General purpose power regulator
- 24V Bus power
- Battery power
- Embedded processor and I/O supplies

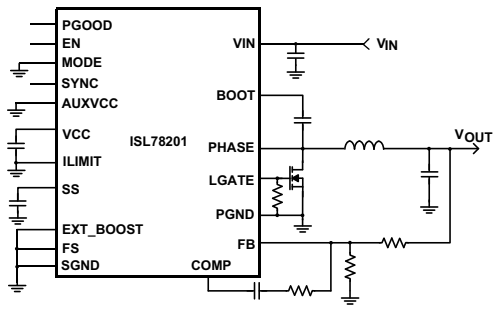


FIGURE 1. TYPICAL APPLICATION

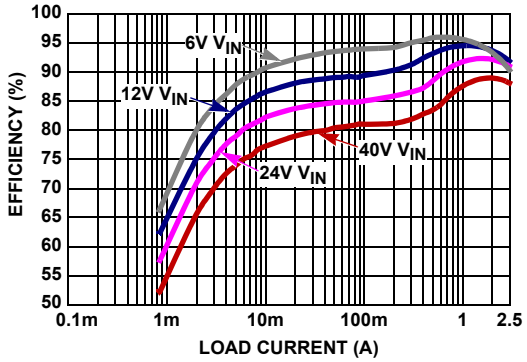
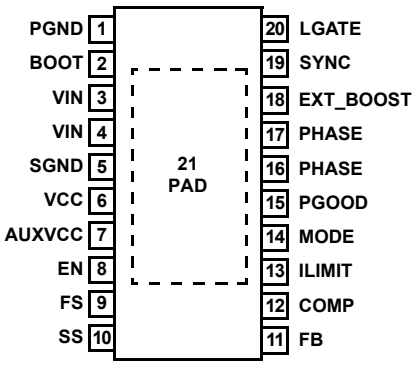


FIGURE 2. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, V_{OUT} 5V, T_A = +25°C

Pin Configuration

ISL78201
(20 LD HTSSOP)
TOP VIEW



Functional Pin Description

PIN NAME	PIN #	DESCRIPTION
PGND	1	This pin is used as the ground connection of the power flow including driver.
BOOT	2	This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot charge circuitries are integrated inside the IC. No external boot diode is needed. A 1µF ceramic capacitor is recommended to be used between BOOT and PHASE pin.
VIN	3, 4	Connect the input rail to these pins that are connected to the drain of the integrated high-side MOSFET, as well as the source for the internal linear regulator that provides the bias of the IC. Range: 3V to 40V. With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding Absolute Maximum Ratings.
SGND	5	This pin provides the return path for the control and monitor portions of the IC.
VCC	6	This pin is the output of the internal linear regulator that supplies the bias for the IC including the driver. A minimum 4.7µF decoupling ceramic capacitor is recommended between VCC to ground.
AUXVCC	7	This pin is the input of the auxiliary internal linear regulator which can be supplied by the regulator output after power-up. With such a configuration, the power dissipation inside the IC is reduced. The input range for this LDO is 3V to 20V. In boost mode operation, this pin works as boost output overvoltage detection pin. It detects the boost output through a resistor divider. When the voltage on this pin is above 0.8V, the boost PWM is disabled; and when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled. Range: 3V to 20V.
EN	8	The controller is enabled when this pin is pulled HIGH or left floating. The IC is disabled when this pin is pulled LOW. Range: 0V to 5.5V.
FS	9	To connect this pin to VCC, or GND, or left open will force the IC to have 500kHz switching frequency. The oscillator switching frequency can also be programmed by adjusting the resistor from this pin to GND.
SS	10	Connect a capacitor from this pin to ground. This capacitor, along with an internal 5µA current source, sets the soft-start interval of the converter. Also this pin can be used to track a ramp on this pin.
FB	11	This pin is the inverting input of the voltage feedback error amplifier. With a properly selected resistor divider connected from V_{OUT} to FB, the output voltage can be set to any voltage between the input rail (reduced by maximum duty cycle and voltage drop) and the 0.8V reference. Loop compensation is achieved by connecting an RC network across COMP and FB. The FB pin is also monitored for overvoltage events.
COMP	12	Output of the voltage feedback error amplifier.
ILIMIT	13	Programmable current limit pin. With this pin connected to VCC pin, or to GND, or left open, the current limit threshold is set to default 3.6A; the current limit threshold can be programmed with a resistor from this pin to GND.
MODE	14	Mode selection pin. Pull this pin to GND for forced PWM mode; to have it floating or connected to VCC will enable PFM mode when the peak inductor current is below the default threshold of 700mA. The current boundary threshold between PFM and PWM can also be programmed with a resistor at this pin to ground. For more details on PFM Mode Operation refer to the "Functional Description" on page 14.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
PGOOD	15	PGOOD is an open drain output and pull-up this pin with a resistor to VCC for proper function. PGOOD will be pulled low under the events when the output is out of regulation (OV or UV) or EN pin is pulled low. PGOOD rising has a fixed 128 cycles delay.
PHASE	16, 17	These pins are the PHASE nodes that should be connected to the output inductor. These pins are connected to the source of the high-side N channel MOSFET.
EXT_BOOST	18	This pin is used to set boost mode and monitor the battery voltage that is the input of the boost converter. After VCC POR, the controller will detect the voltage on this pin, if voltage on this pin is below 200mV, the controller is set in synchronous/non-synchronous buck mode and latch in this state unless VCC is below the POR falling threshold; if the voltage on this pin after VCC POR is above 200mV, the controller is set in boost mode and latch in this state. In boost mode, this pin is used to monitor input voltage through a resistor divider. By setting the resistor divider, the high threshold and hysteresis can be programmed. When voltage on this pin is above 0.8V, the PWM output (LGATE) for the boost converter is disabled, and when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled. In boost mode operation, PFM is disabled when boost PWM is enabled. Check Boost Mode Operation in the "Functional Description" on page 14 for more details.
SYNC	19	This pin can be used to synchronize two or more ISL78201 controllers. Multiple ISL78201s can be synchronized with their SYNC pins connected together. 180 degree phase shift is automatically generated between the master and slave ICs. The internal oscillator can also lock to an external frequency source applied on this pin with square pulse waveform (with frequency 10% higher than the IC's local frequency, and pulse width higher than 150ns). This pin should be left floating if not used. Range: 0V to 5.5V.
LGATE	20	In synchronous buck mode, this pin is used to drive the lower side MOSFET to improve efficiency. A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise. In non-synchronous buck when a diode is used as the bottom side power device, this pin should be connected to VCC through a resistor (less than 5k) before VCC start-up to have low-side driver (LGATE) disabled. In boost mode, it can be used to drive the boost power MOSFET. The boost control PWM is the same with the buck control PWM.
PAD	21	Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout it must be connected to PCB ground copper plane with an area as large as possible to effectively reduce the thermal impedance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL78201AVEZ	78201 AVEZ	-40 to +105	20 Ld HTSSOP	M20.173A
ISL78201EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78201. For more information on MSL please see techbrief TB363.

Block Diagram

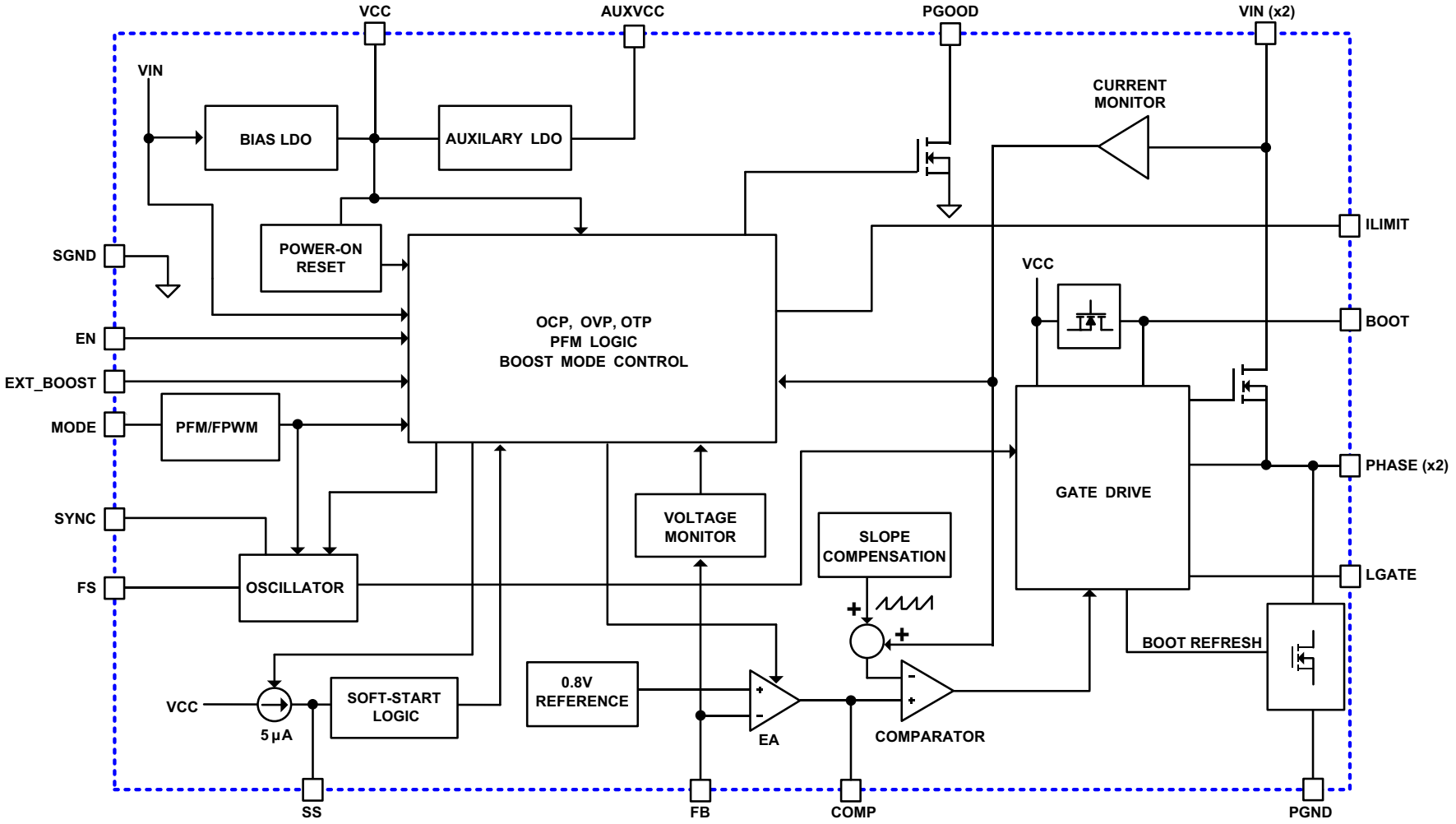


FIGURE 3. BLOCK DIAGRAM

Typical Application Schematic I

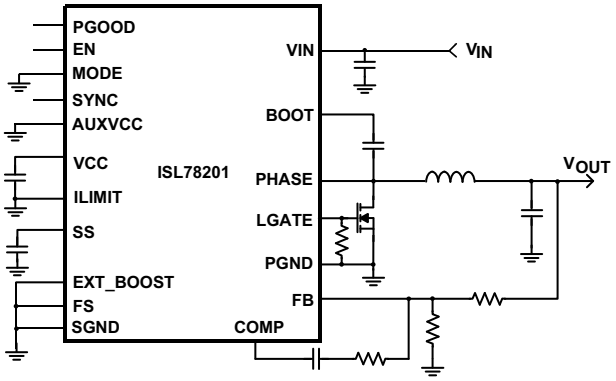


FIGURE 4A. SYNCHRONOUS BUCK

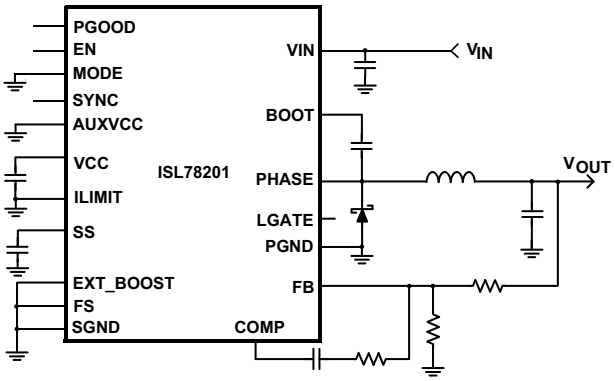


FIGURE 4B. NON-SYNCHRONOUS BUCK

Typical Application Schematic II - V_{CC} Switch Over to V_{OUT}

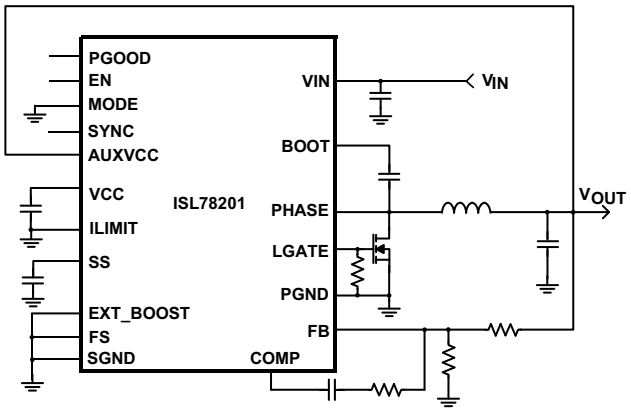


FIGURE 5A. SYNCHRONOUS BUCK

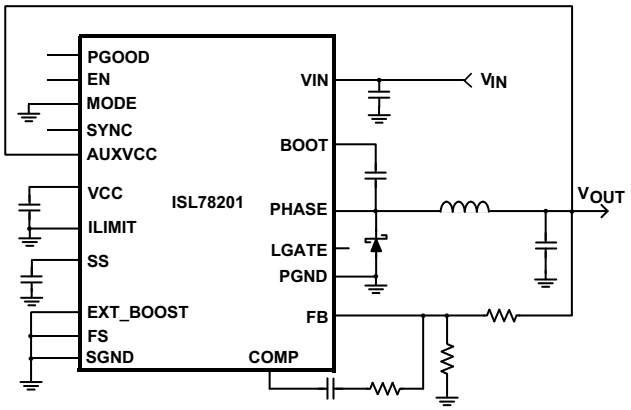


FIGURE 5B. NON-SYNCHRONOUS BUCK

Typical Application Schematic III - Boost Buck Converters

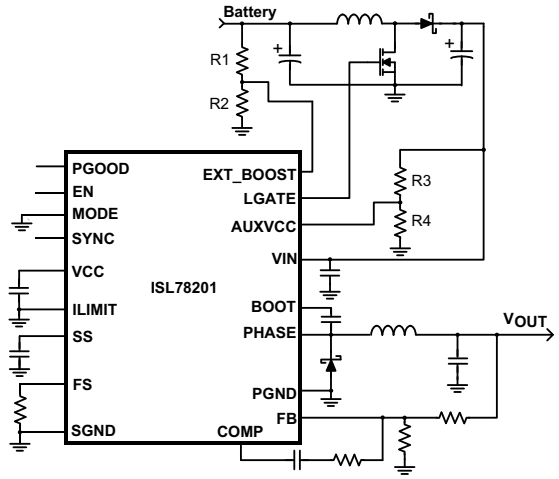


FIGURE 6A. 2-STAGE BOOST BUCK

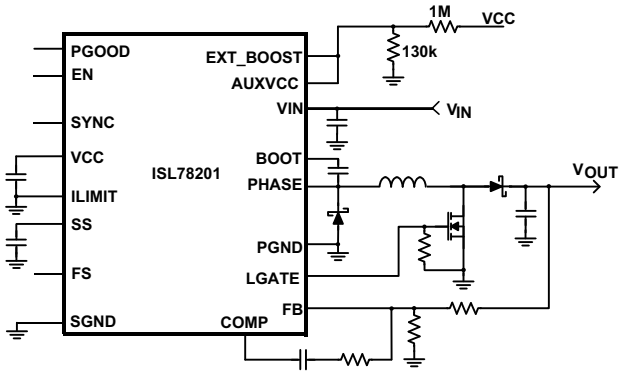


FIGURE 6B. NON-INVERTING SINGLE INDUCTOR BUCK BOOST

Absolute Maximum Ratings

VIN, PHASE . . . . . GND - 0.3V to +44V
VCC . . . . . GND - 0.3V to +6.0V
AUXVCC . . . . . GND - 0.3V to +22V
Absolute Boot Voltage, V_{BOOT} . . . . . +50.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . +6.0V
All Other Pins . . . . . GND - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2000V
Machine Model (Tested per JESD22-A115C) 250V
Charged Device Model (Tested per AEC-Q100-011) 1000V
Latch-up Rating (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
HTSSOP Package (Notes 4, 5)	35	3.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage on VIN . . . . . 3V to 40V
AUXVCC . . . . . GND - 0.3V to +20V
Ambient Temperature Range (Automotive) . . . . . -40°C to +105°C
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Refer to the Block Diagram (page 4) and Typical Application Schematics (page 5). Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +105°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{IN} SUPPLY						
V_{IN} Pin Voltage Range		V_{IN} pin	**3.05**		**40**	V
		V_{IN} connected to VCC	**3.05**		**5.5**	V
Operating Supply Current	I_Q	MODE = VCC/FLOATING (PFM), no load at the output		300		µA
		MODE = GND (Forced PWM), V_{IN} = 12V, IC Operating, not including driving current		1.3		mA
Shutdown Supply Current	I_{IN_SD}	EN connected to GND, V_{IN} = 12V		2.8	**4.5**	µA
INTERNAL MAIN LINEAR REGULATOR						
MAIN LDO V_{CC} Voltage	V_{CC}	V_{IN} > 5V	**4.2**	4.5	**4.8**	V
MAIN LDO Dropout Voltage	$V_{DROPOUT\_MAIN}$	V_{IN} = 4.2V, I_{VCC} = 35mA		0.3	**0.52**	V
		V_{IN} = 3V, I_{VCC} = 25mA		0.25	**0.42**	V
V_{CC} Current Limit of MAIN LDO				60		mA
INTERNAL AUXILIARY LINEAR REGULATOR						
AUXVCC Input Voltage Range	V_{AUXVCC}		**3**		**20**	V
AUX LDO V_{CC} Voltage	V_{CC}	V_{AUXVCC} > 5V	**4.2**	4.5	**4.8**	V
LDO Dropout Voltage	$V_{DROPOUT\_AUX}$	V_{AUXVCC} = 4.2V, I_{VCC} = 35mA		0.3	**0.52**	V
		V_{AUXVCC} = 3V, I_{VCC} = 25mA		0.25	**0.42**	V
Current Limit of AUX LDO				60		mA
AUX LDO Switch-over Rising Threshold	V_{AUXVCC_RISE}	AUXVCC voltage rise, switch to auxiliary LDO	**2.97**	3.1	**3.2**	V
AUX LDO Switch-over Falling Threshold	V_{AUXVCC_FALL}	AUXVCC voltage fall, switch back to main BIAS LDO	**2.73**	2.87	**2.97**	V
AUX LDO Switch-over Hysteresis	V_{AUXVCC_HYS}	AUXVCC switch-over hysteresis		0.2		V
POWER-ON RESET						
Rising V_{CC} POR Threshold	V_{PORH_RISE}		**2.82**	2.9	**3.05**	V
Falling V_{CC} POR Threshold	V_{PORL_FALL}			2.6	**2.8**	V

Electrical Specifications

Refer to the Block Diagram (page 4) and Typical Application Schematics (page 5). Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{CC} POR Hysteresis	V_{PORL_HYS}			0.3		V
ENABLE						
Required Enable On Voltage	V_{ENH}		**1.7**			V
Required Enable Off Voltage	V_{ENL}				**1**	V
EN Pull-up Current	I_{EN_PULLUP}	V_{EN} = 1.2V, V_{IN} = 24V		1.5		µA
		V_{EN} = 1.2V, V_{IN} = 12V		1.2		µA
		V_{EN} = 1.2V, V_{IN} = 5V		0.9		µA
OSCILLATOR						
PWM Frequency	F_{OSC}	R_T = 665kΩ	**160**	200	**240**	kHz
		R_T = 51.1kΩ	**1870**	2200	**2530**	kHz
		FS pin connected to VCC or floating or GND	**450**	500	**550**	kHz
MIN ON Time	t_{MIN_ON}			130	**225**	ns
MIN OFF Time	t_{MIN_OFF}			210	**330**	ns
SYNCHRONIZATION						
Input High Threshold	VIH			2		V
Input Low Threshold	VIL			0.5		V
Input Minimum Pulse Width				25		ns
Input Impedance				100		kΩ
Input Minimum Frequency Divided by Free Running Frequency				1.1		
Input Maximum Frequency Divided by Free Running Frequency				1.6		
Output Pulse Width		C_{SYNC} = 100pF		100		ns
Output Pulse High	VOH	R_{LOAD} = 1kΩ		VCC-0.25		V
Output Pulse Low	VOL			GND		V
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}			0.8		V
System Accuracy			**-1.0**		**1.0**	%
FB Pin Source Current				5		nA
SOFT-START						
Soft-Start Current	I_{SS}		**3**	5	**7**	µA
ERROR AMPLIFIER						
Unity Gain-bandwidth		C_{LOAD} = 50pF		10		MHz
DC Gain		C_{LOAD} = 50pF		88		dB
Maximum Output Voltage				3.6		V
Minimum Output Voltage				0.5		V
Slew Rate	SR	C_{LOAD} = 50pF		5		V/µs
PFM MODE CONTROL						

Electrical Specifications

Refer to the Block Diagram (page 4) and Typical Application Schematics (page 5). Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Default PFM Current Threshold		MODE = VCC or floating		700		mA
INTERNAL HIGH-SIDE MOSFET						
Upper MOSFET $r_{DS(ON)}$	$r_{DS(ON)\_UP}$	(Note 7) Limits apply for +25°C		127	140	mΩ
LOW-SIDE MOSFET GATE DRIVER						
LGATE Source Resistance		100mA source current		3.5		Ω
LGATE Sink Resistance		100mA sink current		2.8		Ω
BOOST CONVERTER CONTROL						
EXT_BOOST Boost_Turn-off Threshold Voltage			**0.74**	0.8	**0.86**	V
EXT_BOOST Hysteresis Sink Current	$I_{EXT\_BOOST\_HYS}$		**2.1**	3.2	**4.2**	µA
AUXVCC Boost Turn-off Threshold Voltage			**0.74**	0.8	**0.86**	V
AUXVCC Hysteresis Sink Current	I_{AUXVCC_HYS}		**2.1**	3.2	**4.2**	µA
POWER GOOD MONITOR						
Overvoltage Rising Trip Point	V_{FB}/V_{REF}	Percentage of reference point	**104**	110	**116**	%
Overvoltage Rising Hysteresis	V_{FB}/V_{OVTRIP}	Percentage below OV trip point		3		%
Undervoltage Falling Trip Point	V_{FB}/V_{REF}	Percentage of reference point	**84**	90	**96**	%
Undervoltage Falling Hysteresis	V_{FB}/V_{UVTRIP}	Percentage above UV trip point		3		%
PGOOD Rising Delay	t_{PGOODR_DELAY}			128		cycle
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 4.5V		10		nA
PGOOD Low Voltage	V_{PGOOD}	PGOOD LOW, I_{PGOOD} = 0.2mA		0.10		V
OVERCURRENT PROTECTION						
Default Cycle-by-cycle Current Limit Threshold	I_{OC_1}	ILIMIT = GND or VCC or floating	**3**	3.6	**4.2**	A
Hiccup Current Limit Threshold	I_{OC_2}	Hiccup, I_{OC_2}/I_{OC_1}		115		%
OVERVOLTAGE PROTECTION						
OV 120% Trip Point		Active in and after soft-start Percentage of Reference Point LG = UG = LOW		120		%
OV 120% Release Point		Active in and after soft-start Percentage of reference point		102.5		%
OV 110% Trip Point		Active after soft-start done Percentage of reference point LG = UG = LOW		110		%
OV 110% Release Point		Active after soft-start done Percentage of Reference Point		102.5		%
OVER-TEMPERATURE PROTECTION						
Over-temperature Trip Point				160		°C
Over-temperature Recovery Threshold				140		°C

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Wire bonds included.

Performance Curves

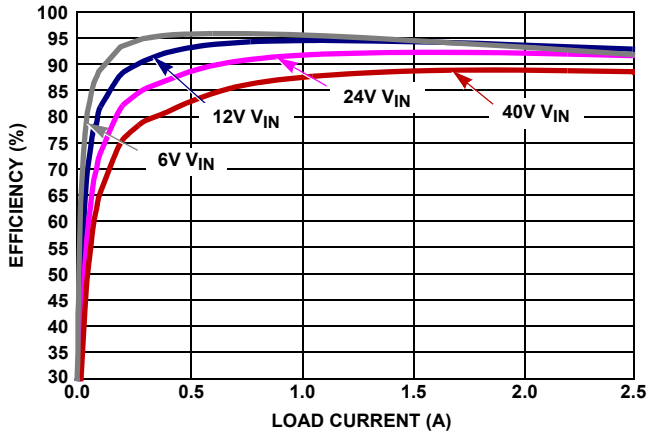


FIGURE 7. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, V_{OUT} 5V, T_A = +25°C

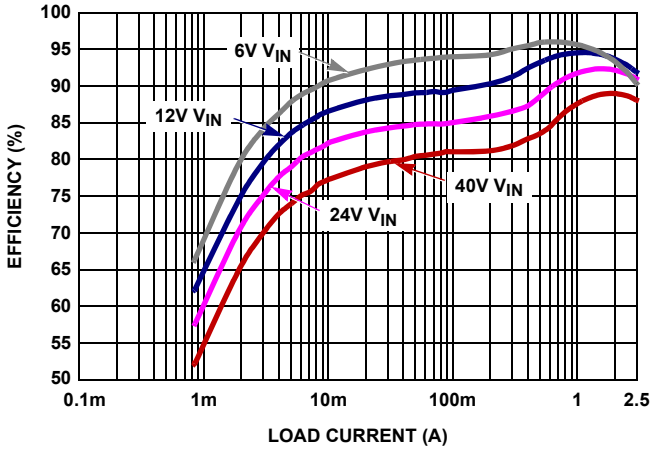


FIGURE 8. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, V_{OUT} 5V, T_A = +25°C

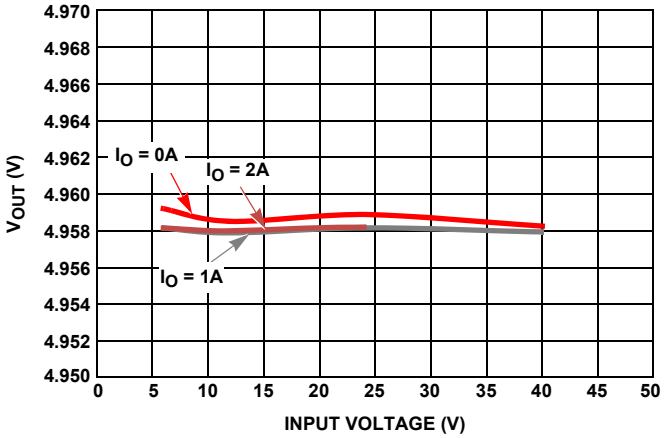


FIGURE 9. LINE REGULATION, V_{OUT} 5V, T_A = +25°C

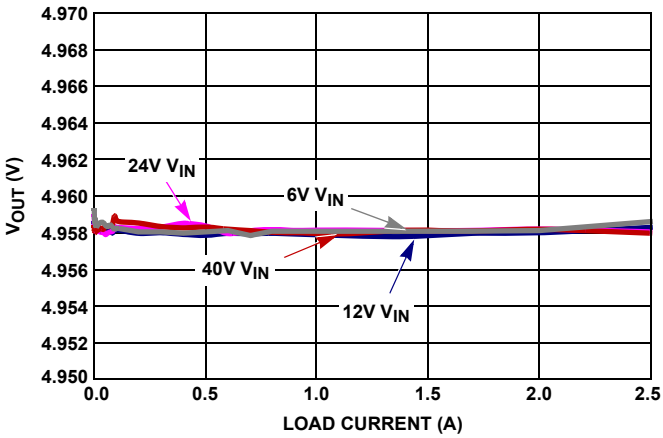


FIGURE 10. LOAD REGULATION, V_{OUT} 5V, T_A = +25°C

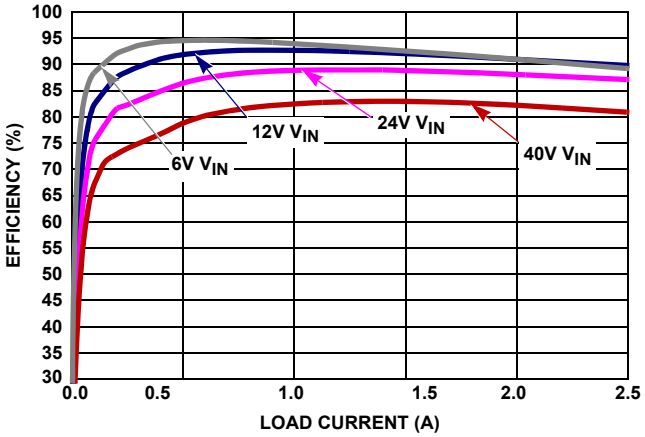


FIGURE 11. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, V_{OUT} 3.3V, T_A = +25°C

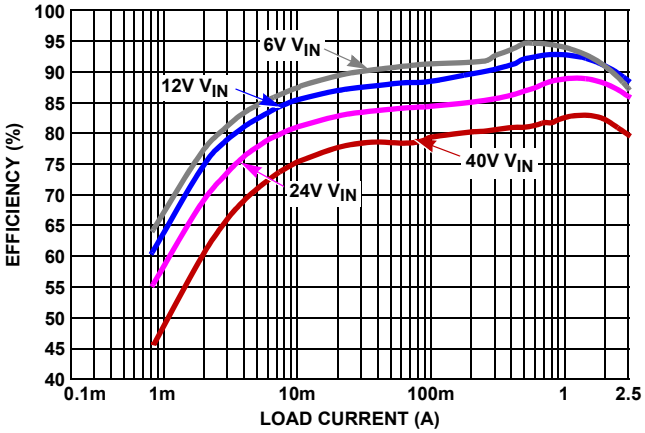


FIGURE 12. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, V_{OUT} 3.3V, T_A = +25°C

Performance Curves (Continued)

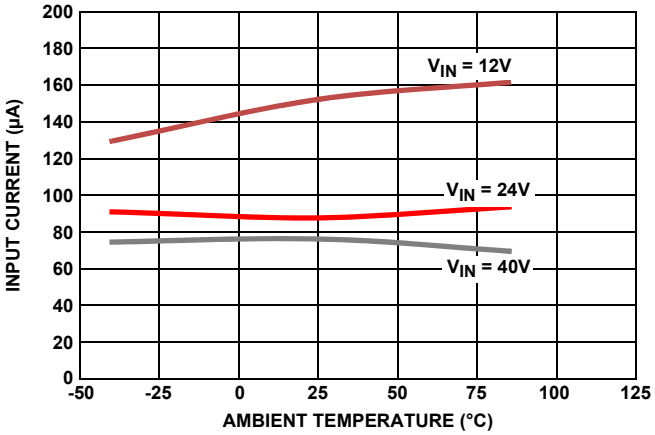


FIGURE 13. INPUT QUIESCENT CURRENT UNDER NO LOAD, PFM MODE, AUXVCC CONNECTED TO V_{OUT}, V_{OUT} = 5V

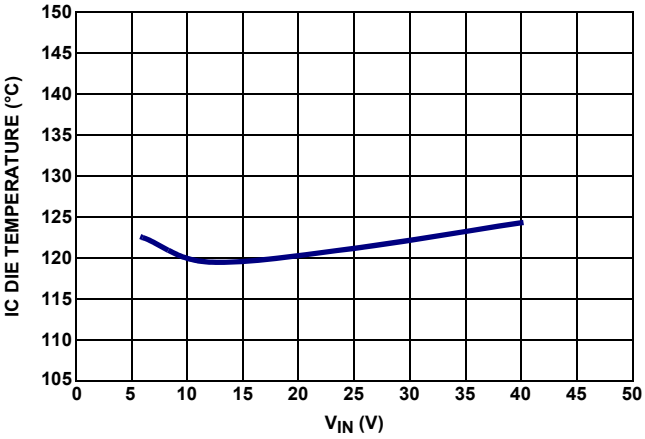


FIGURE 14. IC DIE TEMPERATURE UNDER +105°C AMBIENT TEMPERATURE, 100 CFM, 500kHz, V_{OUT} = 5V, I_O = 2A

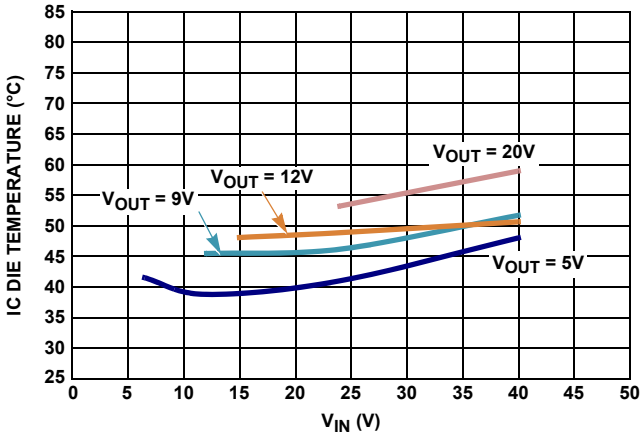


FIGURE 15. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500kHz, I_O = 2A

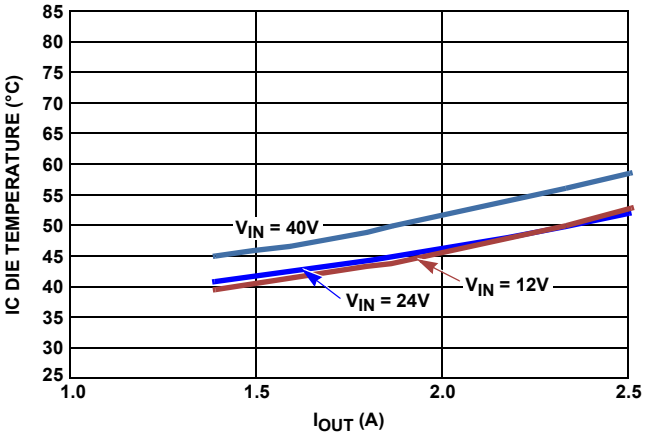


FIGURE 16. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500kHz, V_{OUT} = 9V

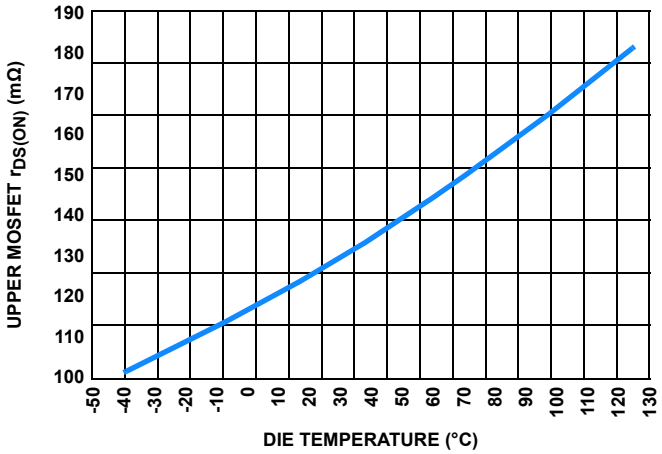


FIGURE 17. UPPER MOSFET $r_{DS(ON)}$ (mΩ) OVER TEMPERATURE

Performance Curves (Continued)

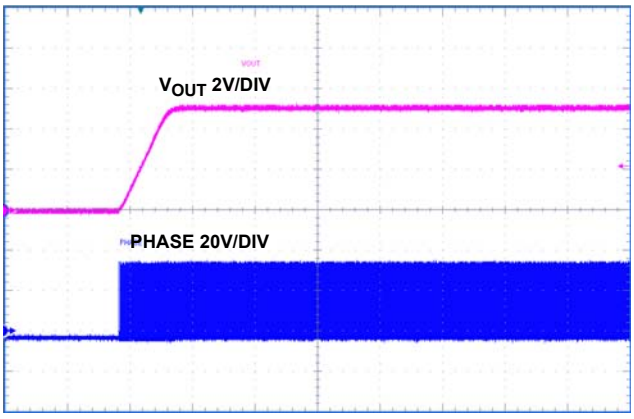


FIGURE 18. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE ON

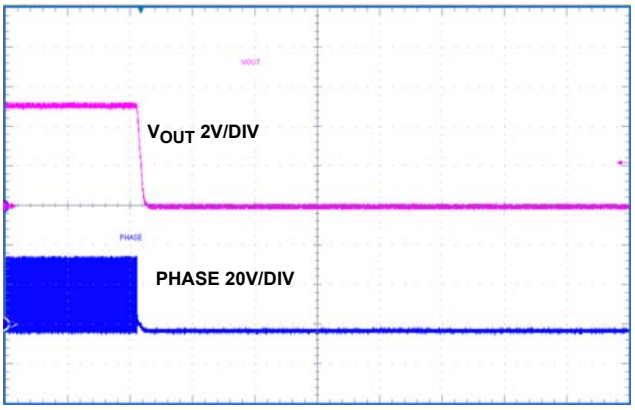


FIGURE 19. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE OFF

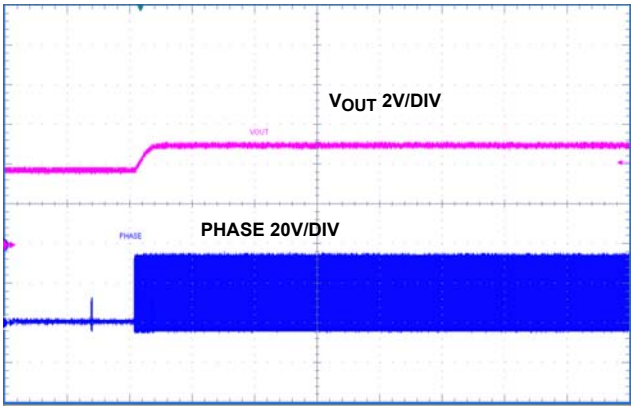


FIGURE 20. V_{IN} 36V, PREBIASED START-UP

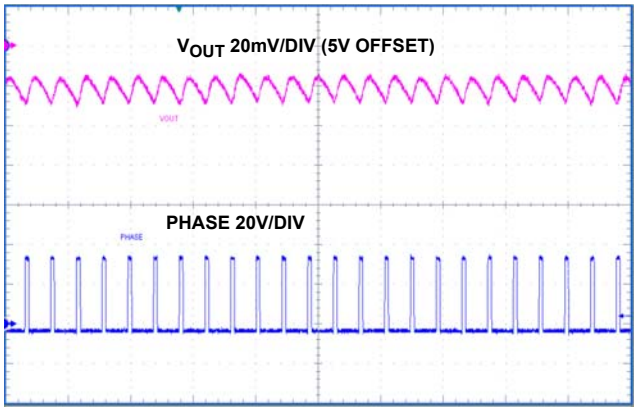


FIGURE 21. SYNCHRONOUS BUCK WITH FORCE PWM MODE, V_{IN} 36V, I_O 2A

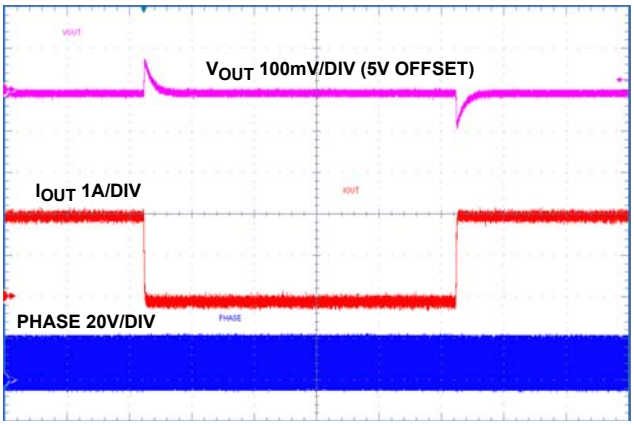


FIGURE 22. V_{IN} 24V, 0 TO 2A STEP LOAD, FORCE PWM MODE

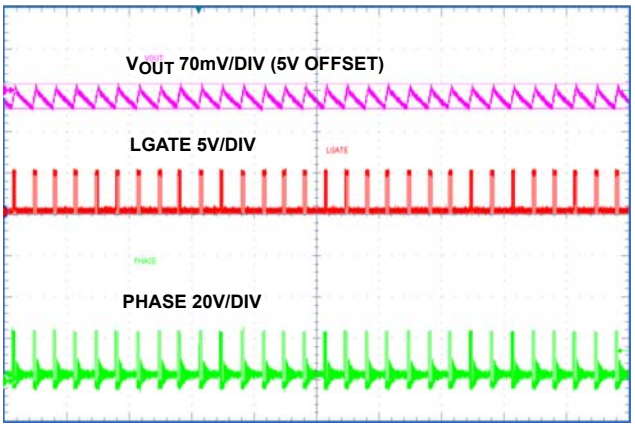


FIGURE 23. V_{IN} 24V, 80mA LOAD, PFM MODE

Performance Curves (Continued)

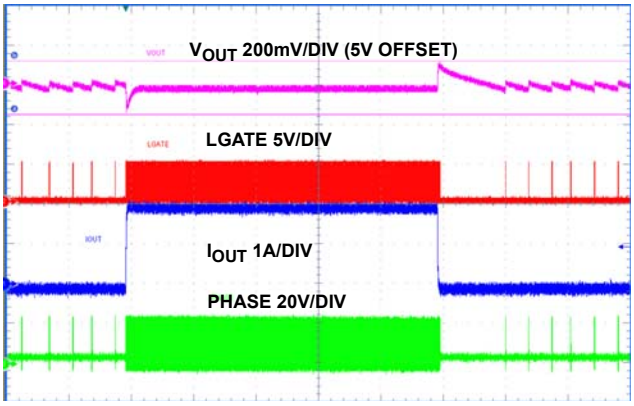


FIGURE 24. V_{IN} 24V, 0 TO 2A STEP LOAD, PFM MODE

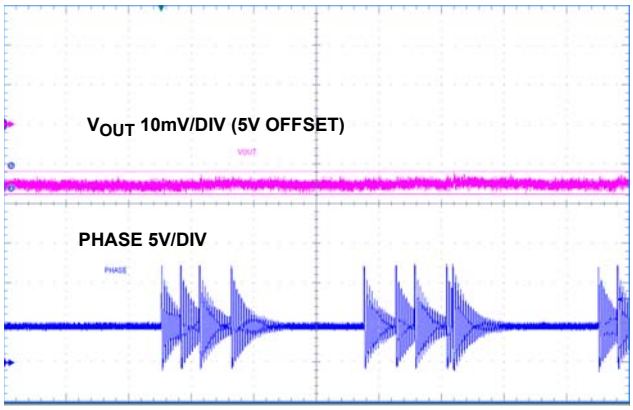


FIGURE 25. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, NO LOAD

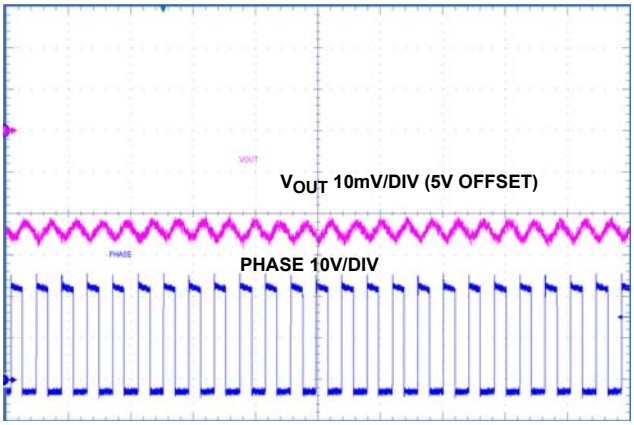


FIGURE 26. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, 2A

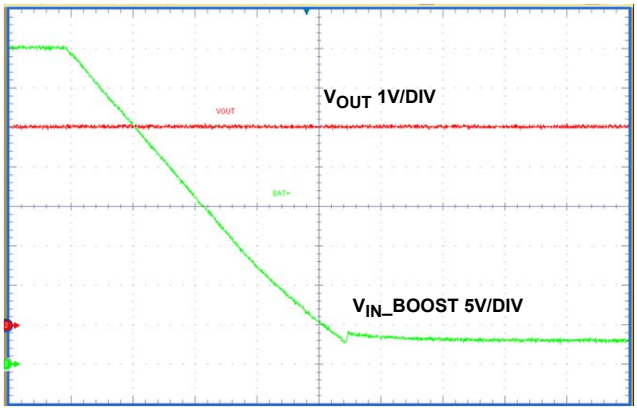


FIGURE 27. BOOST BUCK MODE, BOOST INPUT STEP FROM 40V TO 3V

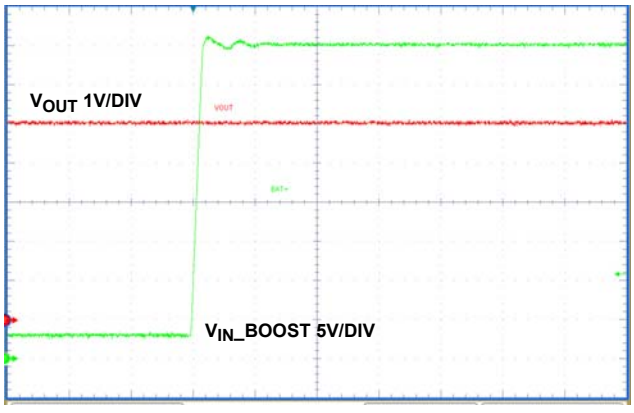


FIGURE 28. BOOST BUCK MODE, BOOST INPUT STEP FROM 3V TO 40V

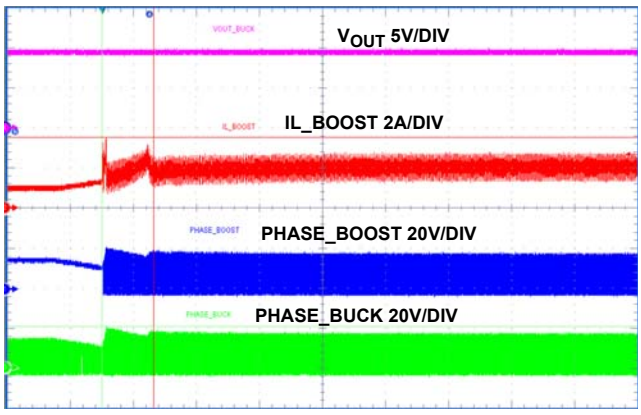


FIGURE 29. BOOST BUCK MODE, V_O = 9V, I_O = 1.8A, BOOST INPUT DROPS FROM 16V TO 9V DC

Performance Curves (Continued)

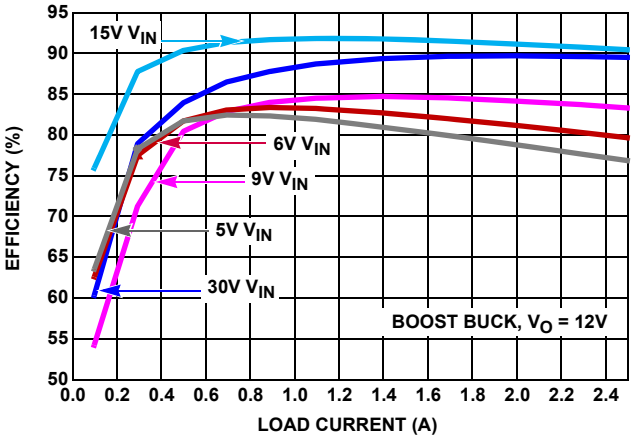


FIGURE 30. EFFICIENCY, BOOST BUCK, 500kHz, V_{OUT} 12V, T_A = +25°C

Functional Description

Initialization

Initially, the ISL78201 continually monitors the voltage at EN pin. When the voltage on EN pin exceeds its rising threshold, the internal LDO will start-up to build up V_{CC}. After Power-On Reset (POR) circuits detect that V_{CC} voltage has exceeded the POR threshold, the soft-start will be initiated.

Soft-Start

The soft-start (SS) ramp is built up in the external capacitor on the SS pin that is charged by an internal 5µA current source.

$$C_{SS}[\mu F] = 6.5 \cdot t_{SS}[S] \quad \text{(EQ. 1)}$$

The SS ramp starts from 0V to a voltage above 0.8V. Once SS reaches 0.8V, the bandgap reference takes over and the IC goes into steady state operation. The soft-start time is referring to the duration for SS pin ramps from 0 to 0.8V while output voltage ramps up with the same rate from 0 to target regulated voltage. The required capacitance at SS pin can be calculated from Equation 1.

The SS plays a vital role in the hiccup mode of operation. The IC works as cycle-by-cycle peak current limiting at overload condition. When a harsh condition occurs and the current in the upper side MOSFET reaches the second overcurrent threshold, the SS pin is pulled to ground and a dummy soft-start cycle is initiated. At the dummy SS cycle, the current to charge the soft-start cap is cut down to 1/5 of its normal value. Therefore, a dummy SS cycle takes 5 times that of the regular SS cycle. During the dummy SS period, the control loop is disabled and no PWM output. At the end of this cycle, it will start the normal SS. The hiccup mode persists until the second overcurrent threshold is no longer reached.

The ISL78201 is capable of start-up with prebiased output.

PWM Control

Pulling the MODE pin to GND will set the IC in forced PWM mode. The ISL78201 employs the peak current mode PWM control for fast transient response and cycle-by-cycle current limiting. See "Block Diagram" on page 4.

The PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on by the clock at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current sense signal and the slope compensation signal reaches the error amplifier output voltage level, the PWM comparator is triggered to shut down the PWM logic to turn off the high-side MOSFET. The high-side MOSFET stays off until the next clock signal comes for the next cycle.

The output voltage is sensed by a resistor divider from V_{OUT} to the FB pin. The difference between the FB voltage and 0.8V reference is amplified and compensated to generate the error voltage signal at the COMP pin. Then the COMP pin signal is compared with the current ramp signal to shut down the PWM.

PFM Mode Operation

To pull the MODE pin HIGH (>2.5V) or leave the MODE pin floating will set the IC to have PFM (Pulse Frequency Modulation) operation in light load. In PFM mode, the switching frequency is dramatically reduced to minimize the switching loss. The ISL78201 enters PFM mode when the MOSFET peak current is lower than the PWM/PFM boundary current threshold. This threshold is 700mA as default when there is no programming resistor at MODE pin. It can also be programmed by a resistor at the MODE pin to ground (see Equation 2).

$$R_{MODE} = \frac{118500}{IPFM + 0.2} \quad \text{(EQ. 2)}$$

where IPFM is the desired PWM/PFM boundary current threshold and R_{MODE} is the programming resistor. The usable resistor value range to program PFM current threshold is 150kΩ to 200kΩ. R_{MODE} value out of this range is not recommended.

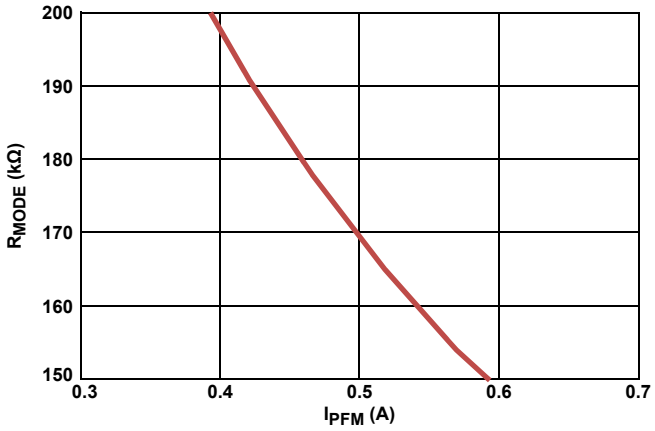


FIGURE 31. R_{MODE} vs IPFM

Synchronous and Non-Synchronous Buck

The ISL78201 supports both Synchronous and non-synchronous buck operations.

In synchronous buck configuration, a 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

For a non-synchronous buck operation when a power diode is used as the low-side power device, the LGATE driver can be disabled with LGATE connected to VCC (before IC start-up). For non-synchronous buck, the phase node will show oscillations after high-side turns off (as shown in Figure 24 - blue trace). This is normal due to the oscillations among the parasitic capacitors at phase node and output inductor. A RC snubber (suggesting 200Ω and 2.2nF as typical) at phase node can reduce this ringing.

AUXVCC Switch-Over

The ISL78201 has an auxiliary LDO integrated as shown in the block diagram on page 4. It is used to replace the internal MAIN LDO function after the IC start-up. "Typical Application Schematic II - V_{CC} Switch Over to V_{OUT}" on page 5 shows its basic application setup with output voltage connected to AUXVCC. After IC soft-start done and the output voltage is built up to steady

state, once the AUXVCC pin voltage is over the AUX LDO Switch-over Rising Threshold, the MAIN LDO is shut off and the AUXILIARY LDO is activated to bias VCC. Since the AUXVCC pin voltage is lower than input voltage V_{IN}, the internal LDO dropout voltage and the consequent power loss is reduced. This feature brings substantial efficiency improvements in light load range especially at high input voltage applications.

When the voltage at AUXVCC falls below the AUX LDO Switch-over Falling Threshold, the AUXILIARY LDO is shut off and the MAIN LDO is re-activated to bias VCC. At the OV/UV fault events, the IC also switch over back from AUXILIARY LDO to MAIN LDO.

The AUXVCC switchover function is offered in buck configuration. It is not offered in boost configuration when the AUXVCC pin is used to monitor the boost output voltage for OVP.

Input Voltage

With the part switching, the operating ISL78201 input voltage must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to part switching while not exceeding 44V as Absolute Maximum Ratings.

The lowest IC operating input voltage (VIN pin) depends on VCC voltage and the Rising and Falling V_{CC} POR Threshold in Electrical Specifications table on page 6. At IC start-up when V_{CC} is just over rising POR threshold, there is no switching yet before the soft-start starts. So the IC minimum start-up voltage on VIN pin is 3.05V (MAX of Rising V_{CC} POR). When the soft-start is initiated, the regulator is switching and the dropout voltage across the internal LDO increases due to driving current. Thus the IC VIN pin shutdown voltage is related to driving current and V_{CC} POR falling threshold. The internal upper side MOSFET has typical 10nC gate drive. For a typical example of synchronous buck with 4nC lower MOSFET gate drive and 500kHz switching frequency, the driving current is 7mA total causing 70mV drop across internal LDO under 3V Vin. Then the IC shut down voltage on VIN pin is 2.87V (2.8V+0.07V). In practical design, extra room should be taken into account with concerns of voltage spikes at VIN.

With boost buck configuration, the input voltage range can be expanded further down to 2.5V or lower depending on the boost stage voltage drop upon maximum duty cycle. Since the boost output voltage is connected to VIN pin as the buck inputs, after the IC starts up, the IC will keep operating and switching as long as the boost output voltage can keep the VCC voltage higher than falling threshold. Refer to "Boost Converter Operation" on page 15 for more details.

Output Voltage

The output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB. For Buck, the maximum achievable voltage is (V_{IN} * D_{MAX} - V_{DROP}), where V_{DROP} is the voltage drop in the power path including mainly the MOSFET $r_{DS(ON)}$ and inductor DCR. The maximum duty cycle D_{MAX} is decided by (1 - Fs * $t_{MIN(OFF)}$).

Output Current

With the high-side MOSFET integrated, the maximum current ISL78201 can support is decided by the package and many operating conditions including input voltage, output voltage, duty cycle, switching frequency and temperature, etc. From the thermal perspective, the die temperature shouldn't be above +125°C with the power loss dissipated inside of the IC.

Figures 14 through 16 show the thermal performance of this part operating in buck at different conditions. The part can output 2.5A under typical buck application condition V_{IN} 8~36V, V_O 5V, 500kHz, still air and +85°C ambient conditions. The output current should be derated under any conditions causing the die temperature to exceed +125°C.

Figure 14 shows a 5V, 2A output application over V_{IN} range under +105°C ambient temperature with 100 CFM air flow.

Figure 15 shows 2A applications under +25°C still air conditions. Different V_{OUT} (5V, 9V, 12V, 20V) applications thermal data are shown over V_{IN} range at +25°C and still air. The temperature rise data in this figure can be used to estimate the die temperature at different ambient temperatures under various operating conditions. Note: More temperature rise is expected at higher ambient temperatures due to more conduction loss caused by $r_{DS(ON)}$ increase.

Figure 16 shows thermal performance under various output currents and input voltages. It shows the temperature rise trend with load and V_{IN} changes.

Basically, the die temperature equals the sum of ambient temperature and the temperature rise resulting from power dissipated from the IC package with a certain junction to ambient thermal impedance θ_{JA}. The power dissipated in the IC is related to the MOSFET switching loss, conduction loss and the internal LDO loss. Besides the load, these losses are also related to input voltage, output voltage, duty cycle, switching frequency and temperature. With the exposed pad at the bottom, the heat of the IC mainly goes through the bottom pad and θ_{JA} is greatly reduced. The θ_{JA} is highly related to layout and air flow conditions. In layout, multiple vias (20) are strongly recommended in the IC bottom pad. In addition, the bottom pad with its vias should be placed in ground copper plane with an area as large as possible connected through multiple layers. The θ_{JA} can be reduced further with air flow.

For applications with high output current and bad operating conditions (compact board size, high ambient temperature, etc.), synchronous buck is highly recommended since the external low-side MOSFET generates smaller heat than external low-side power diode. This helps to reduce PCB temperature rise around the ISL78201 and less junction temperature rise.

Boost Converter Operation

The Typical Application Schematic III on page 5 shows the circuits where the boost works as a pre-stage to provide input to the following Buck stage. This is for applications when the input voltage could drop to a very low voltage in some constants (in some battery powered systems as an example), causing the output voltage drops out of regulation. The boost converter can be enabled to boost the input voltage up to keep the output voltage in regulation. When the system input voltage recovers back to normal, the boost stage is disabled while only the buck stage is switching.

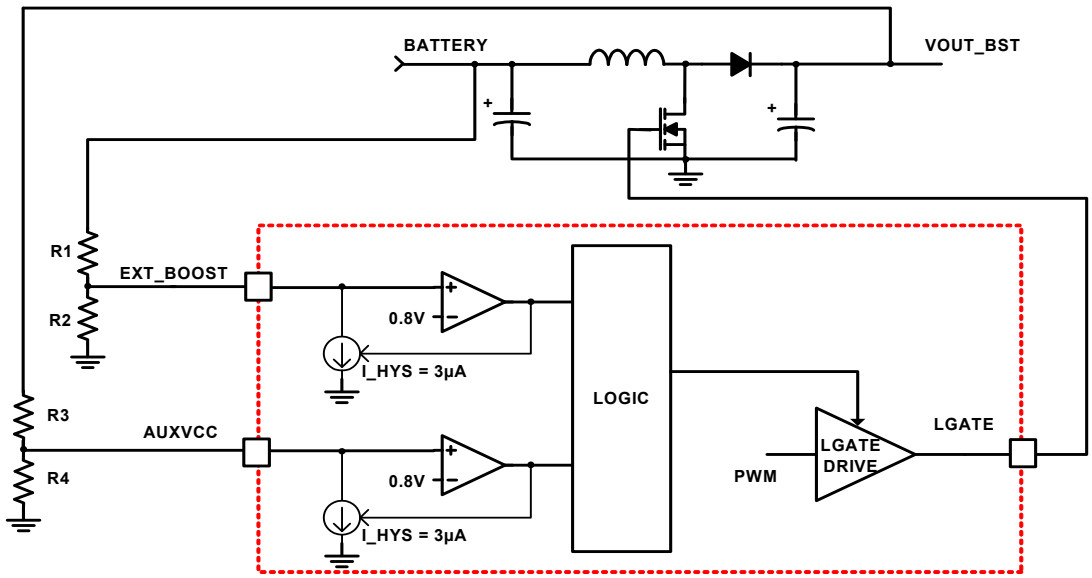


FIGURE 32. BOOST CONVERTER CONTROL

EXT_BOOST pin is used to set boost mode and monitor the boost input voltage. At IC start-up before soft-start, the controller will latch in boost mode when the voltage on this pin is above 200mV; it will latch in synchronous buck mode if voltage on this pin is below 200mV. In boost mode, the low-side driver output PWM has the same PWM signal with the buck regulator.

In boost mode, the EXT_BOOST pin is used to monitor boost input voltage to turn on and turn off the boost PWM. The AUXVCC pin is used to monitor the boost output voltage to turn on and turn off the boost PWM.

Referring to Figure 32, a resistor divider from boost input voltage to the EXT_BOOST pin is used to detect the boost input voltage. When the voltage on the EXT_BOOST pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start when the boost duty cycle increases from t_{MINON}*Fs to ~50% and a 3µA sinking current is enabled at the EXT_BOOST pin for hysteresis purposes. When the voltage on the EXT_BOOST pin recovers to above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor R_{UP} (R1 in Figure 32) for a desired hysteresis VHYS at boost input voltage.

$$R_{UP}[M\Omega] = \frac{VHYS}{3[\mu A]} \quad \text{(EQ. 3)}$$

Use Equation 4 to calculate the lower resistor R_{LOW} (R2 in Figure 32) according to a desired boost enable threshold.

$$R_{LOW} = \frac{R_{UP} \cdot 0.8}{VFTH - 0.8} \quad \text{(EQ. 4)}$$

where VFTH is the desired falling threshold on boost input voltage to turn on the boost, 3µA is the hysteresis current, and 0.8V is the reference voltage to be compared.

Note the boost start-up threshold has to be selected in a way that the buck is operating well at close loop before boost start-up. Otherwise, large inrush current at boost start-up could occur at boost input due to the buck loop saturation. The boost startup input voltage threshold should be set high enough to cover the DC voltage drop of boost inductor and diode, also the buck's maximum duty cycle and voltage conduction drop. This ensures buck is not reaching maximum duty cycle before boost startup.

Similarly, a resistor divider from boost output voltage to the AUXVCC pin is used to detect the boost output voltage. When the voltage on AUXVCC pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start, and a 3µA sinking current is enabled at AUXVCC pin for hysteresis purpose. When the voltage on the AUXVCC pin recovers to above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor R_{UP} (R3 in Figure 32) according to a desired hysteresis VHY at boost output voltage. Use Equation 4 to calculate the lower resistor R_{LOW} (R4 in Figure 32) according to a desired boost enable threshold at boost output.

Assuming VBAT is the boost input voltage, V_{OUTBST} is the boost output voltage and V_{OUT} is the buck output voltage, the steady state transfer functions are:

$$V_{OUTBST} = \frac{1}{1-D} \cdot VBAT \quad \text{(EQ. 5)}$$

$$V_{OUT} = D \cdot V_{OUTBST} = \frac{D}{1-D} \cdot VBAT \quad \text{(EQ. 6)}$$

From Equations 5 and 6, Equation 7 can be derived to estimate the steady state boost output voltage as a function of VBAT and VOUT:

$$V_{OUTBST} = VBAT + VOUT \quad \text{(EQ. 7)}$$

After the IC starts up, the boost buck converters can keep working when the battery voltage drops extremely low because the IC's bias (VCC) LDO is powered by the boost output. For an example of 3.3V output application, when the battery drops to 2V, the VIN pin voltage is powered by the boost output voltage that is 5.2V (Equation 7), meaning the VIN pin (buck input) still needs 5.2V to keep the IC working.

Note in the above mentioned case, the boost input current could be high because the input voltage is very low

(V_{IN} *I_{IN} = V_{OUT} * I_{OUT} / Efficiency). If the design is to achieve the low input operation with full load, the inductor and MOSFET have to be selected to have enough current ratings to handle the high current appearing at boost input. The boost inductor current are the same with the boost input current, which can be estimated in Equation 8, where P_{OUT} is the output power, VBAT is the boost input voltage, and EFF is the estimated efficiency of the whole boost and buck stages.

$$IL_{IN} = \frac{P_{OUT}}{VBAT \cdot EFF} \quad \text{(EQ. 8)}$$

Based on the same concerns of boost input current, the start-up sequence must follow the rule that the IC is enabled after the boost input voltage rise above a certain level. The shutdown sequence must follow the rule that the IC is disabled first before the boost input power source is turned off. At boost mode applications where there is no external control signal to enable/disable the IC, an external input UVLO circuit must be implemented for the start-up and shutdown sequence.

PFM is not available in boost mode.

Non-inverting Single Inductor Buck Boost Converter Operation

In "Typical Application Schematic III - Boost Buck Converters" on page 5, schematic (b) shows non-inverting single inductor buck boost configuration. The recommended setting is to use resistor divider 1MΩ and 130kΩ (as shown in "Typical Application Schematic III - Boost Buck Converters" on page 5 (b) connecting from VCC to both EXT_BOOST and AUXVCC pins (EXT_BOOST and AUXVCC pin are directly connected). In this way, the EXT_BOOST pin voltage is a fixed voltage 0.52V that is higher than the boost mode detection threshold 0.2V to set IC in boost mode and lower than the boost switching threshold 800mV to have boost being constantly switching (during and after soft-start).

As the same in 2-stage boost buck mode, LGATE is switching ON with the same phase of upper FETs switching ON, meaning both upper and lower side FETs are ON and OFF at the same time with the same duty cycle. When both FETs ON, input voltage charges inductor current ramping up for duration of DT; when both FETs OFF, inductor current is free wheeling through the 2 power diodes to output, and output voltage discharge the inductor current ramping down for (1-D)T (in CCM mode). The steady state DC transfer function is:

$$V_{OUT} = \frac{D}{1-D} \cdot V_{IN} \quad \text{(EQ. 9)}$$

where V_{IN} is the input voltage, V_{OUT} is the buck boost output voltage, D is duty cycle.

Another useful equation is to calculate the inductor DC current as shown in Equation 10:

$$IL_{DC} = \frac{1}{1-D} \cdot I_{OUT} \quad \text{(EQ. 10)}$$

where IL_{DC} is the inductor DC current and I_{OUT} is the output DC current.

Equation 10 says the inductor current is charging output only during (1-D)T, which means inductor current has larger DC current than output load current. So for this part with high side FET integrated, the non-inverting buck boost configuration has less load current capability compared with buck and 2-stage boost buck configurations. Its load current capability depends mainly on the duty cycle and inductor current.

Inductor ripple current can be calculated below:

$$IL_{RIPPLE} = \frac{V_{OUT}(1-D)T}{L} \quad \text{(EQ. 11)}$$

The inductor peak current is,

$$IL_{PEAK} = IL_{DC} + \frac{1}{2} \cdot IL_{RIPPLE} \quad \text{(EQ. 12)}$$

In power stage DC calculations, use Equation 9 to calculate D, then use Equation 10 to calculate IL_{DC}. D and IL_{DC} are useful information to estimate the high side FET's power losses and check if the part can meet the load current requirements..

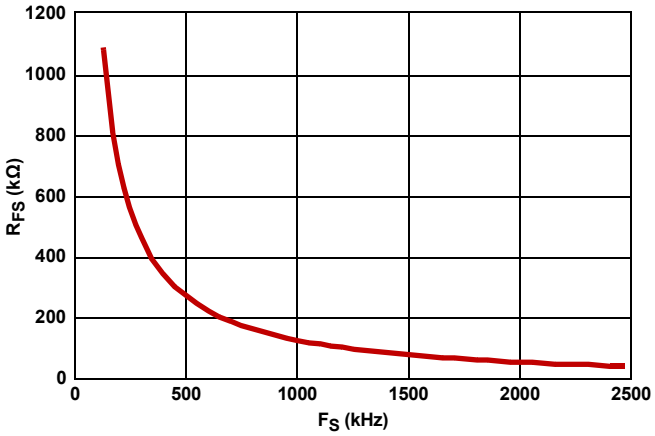


FIGURE 33. R_{FS} vs FREQUENCY

Oscillator and Synchronization

The oscillator has a default frequency of 500kHz with the FS pin connected to VCC, ground, or floating. The frequency can be programmed to any frequency between 200kHz and 2.2MHz with a resistor from the FS pin to GND.

$$R_{FS}[k\Omega] = \frac{145000 - 16 \cdot FS[kHz]}{FS[kHz]} \quad \text{(EQ. 13)}$$

The SYNC pin is bi-directional and it outputs the IC's default or programmed local clock signal when it's free running. The IC locks to an external clock injected to SYNC pin (external clock frequency recommended to be 10% higher than the free running frequency). The delay from the rising edge of the external clock signal to the PHASE rising edge is half of the free running switching period pulse 220ns, (0.5Tsw+220ns). The maximum external clock frequency is recommended to be 1.6 of the free running frequency.

When the part enters PFM pulse skipping mode, the synchronization function is shut off and also no clock signal output in SYNC pin.

With the SYNC pins simply connected together, multiple ISL78201s can be synchronized. The slave ICs automatically have 180° phase shift respect to the master IC.

PGOOD

The PGOOD pin is output of an open drain transistor (refer to at "Block Diagram" on page 4). An external resistor is required to be pulled up to VCC for proper PGOOD function. At startup, PGOOD will be turned HIGH (internal PGOOD open drain transistor is turned off) with 128 cycles delay after soft start is finished (soft start ramp reaches 1.02V) and FB voltage is within OV/UV window (90%REF<FB<110%REF).

At normal operation, PGOOD will be pulled low with 1 cycle (minimum) and 6 cycles (maximum) delay if any of the OV (110%) or UV (90%) comparator is tripped. The PGOOD will be released HIGH with 128 cycles delay after FB recovers to be within OV/UV window (90%REF<FB<110%REF). When EN is pulled low or VCC is below POR, PGOOD is pulled low with no delay.

In the case when the PGOOD pin is pulled up by external bias supply instead of VCC of itself, when the part is disabled, the internal PGOOD open drain transistor is off, the external bias supply can charge PGOOD pin HIGH. This should be known as false PGOOD reporting. At start-up when VCC rise from 0, PGOOD will be pulled low when VCC reaches 1V. After EN pulled low and VCC falling, PGOOD internal open drain transistor will open with high impedance when VCC falls below 1V. The time between EN pulled low and PGOOD OPEN depends on the VCC falling time to 1V.

Fault Protection

Overcurrent Protection

The overcurrent function protects against any overload condition and output shorts at worst case, by monitoring the current flowing through the upper MOSFET.

There are 2 current limiting thresholds. The first one, I_{OC1}, is to limit the high-side MOSFET peak current cycle-by-cycle. The current limit threshold is set to default at 3.6A with the ILIMIT pin connected to GND or VCC, or left open. The current limit threshold can also be programmed by a resistor, R_{LIM}, at the ILIMIT pin to ground. Use Equation 14 to calculate the resistor.

$$R_{LIM} = \frac{300000}{I_{OC}[A] + 0.018} \quad \text{(EQ. 14)}$$

Note that with the lower R_{LIM}, I_{OC1} is higher. The usable resistor value range to program OC1 peak current threshold is 40kΩ to 330kΩ. R_{LIM} value out of this range is not recommended.

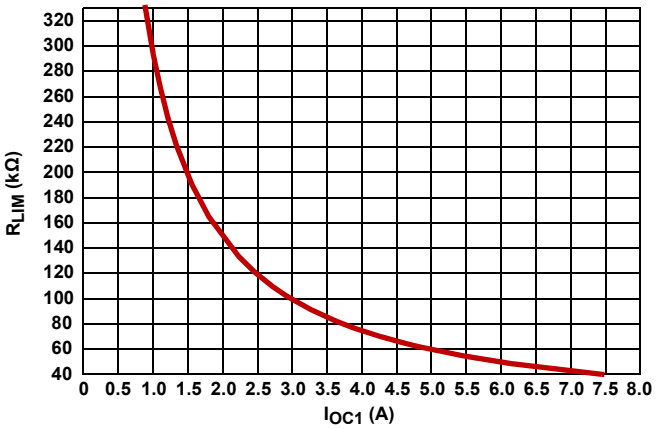


FIGURE 34. R_{LIM} vs I_{OC1}

The second current protection threshold, I_{OC2}, is 15% higher than I_{OC1} mentioned above. At the instant the high-side MOSFET current reaches I_{OC2}, the PWM shuts off after a 2 cycle delay and the IC enters hiccup mode. In hiccup mode, the PWM is disabled for a dummy soft-start duration equal to 5 regular soft-start periods. After this dummy soft-start cycle, the true soft-start cycle is attempted again. The I_{OC2} offers a robust and reliable protection against worst case conditions.

The frequency fold back is implemented for the ISL78201. When overcurrent limiting, the switching frequency is reduced to proportional to the output voltage in order to keep the inductor current under the limit threshold during overload condition. The low limit of frequency under frequency foldback is 40kHz.

Overvoltage Protection

If the voltage detected on the FB pin is over 110% or 120% of reference, the high-side and low-side driver shuts down immediately and keep off until FB voltage drops to 0.8V. When the FB voltage drops to 0.8V, the drivers are released ON. 110% OVP is off at soft-start and becomes active after soft-start is done. 120% OVP is active before and after soft-start.

Thermal Protection

The ISL78201 PWM will be disabled if the junction temperature reaches +160°C. There is +20°C hysteresis for OTP. The part will restart after the junction temperature drops below +140°C.

Component Selections

The ISL78200 iSim model is available on the web and can be used to simulate the operating behaviors to assist the design.

Output Capacitors - Buck

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are 2 critical factors when considering output capacitance choice. The current mode control loop allows the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * f_{SW} * C_{OUT}} \quad \text{(EQ. 15)}$$

Where ΔI is the inductor's peak to peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 16)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. The Equation 17 determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (V_{OUTMAX}/V_{OUT})^2 - 1)} \quad \text{(EQ. 17)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load.

Input Capacitors - Buck

Depending upon the system input power rail conditions, the aluminum electrolytic type capacitor is normally needed to provide the stable input voltage and restrict the switching frequency pulse current in small areas over the input traces for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at the VIN pin of the IC and multiple capacitors including 1µF and 0.1µF are recommended. Place these capacitors as closely as possible to the IC.

Output Inductor - Buck

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% to 40% of total load current. The inductor value can then be calculated using Equation 18:

$$L = \frac{V_{IN} - V_{OUT}}{Fs \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 18)}$$

Increasing the value of inductance reduces the ripple current and thus ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be such that it will not saturate in overcurrent conditions.

Low-Side Power MOSFET

In synchronous buck application, a power N MOSFET is needed as the synchronous low-side MOSFET and a good one should have low Qgd, low $r_{DS(ON)}$ and small Rg (Rg_typ < 1.5Ω recommended). Vgth_min is recommended to be or higher than 1.2V. A good example is SQS462EN.

A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB according to Equation 19.

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_{UP}}{R_{LOW}}\right) \quad \text{(EQ. 19)}$$

In applications requiring the least input quiescent current, large resistors should be used for the divider to keep its leakage current low. Generally, a resistor value of 10k to 300k can be used for the upper resistor.

Boost Inductor

Besides the need to sustain the current ripple to be within a certain range (30% to 50%), the boost inductor current at its soft-start is a more important perspective to be considered in selection of the boost inductor. Each time the boost starts up, there is a fixed 500µs soft-start time when the duty cycle increase linearly from t_{MINON} to ~50%. Before and after boost start-up, the boost output voltage will jump from V_{IN}_boost to voltage (V_{IN}_boost + V_{OUT}_buck). The design target in boost soft-start is to ensure the boost input current is sustained to a minimum but capable of charging the boost output voltage to have a voltage step equaling to V_{OUT}_buck. A big inductor will block the inductor current increase and not high enough to be able to charge the output capacitor to the final steady state value (V_{IN}_boost+V_{OUT}_buck) within 500µs. A 6.8µH inductor is a good starting point for its selection in design. The boost inductor current at start-up must be checked by an oscilloscope to ensure it is under the acceptable range. It is suggested to run the iSim model simulation to select the proper inductor value.

Boost Output Capacitor

Based on the same theory in boost start-up described above in boost inductor selection, a large capacitor at boost output will cause high inrush current at boost PWM start-up. 22µF is a good choice for applications with buck output voltage less than 10V. Also, some minimum amount of capacitance has to be used in boost output to keep the system stable. It is suggested to run the iSim model simulation to select the proper inductor value.

Loop Compensation Design-Buck

The ISL78201 uses constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes single order system. It is much easier to design the compensator to stabilize the loop compared with voltage mode control. Peak current mode control has inherent input voltage feed-forward function to achieve good line regulation. Figure 35 shows the small signal model of a buck regulator.

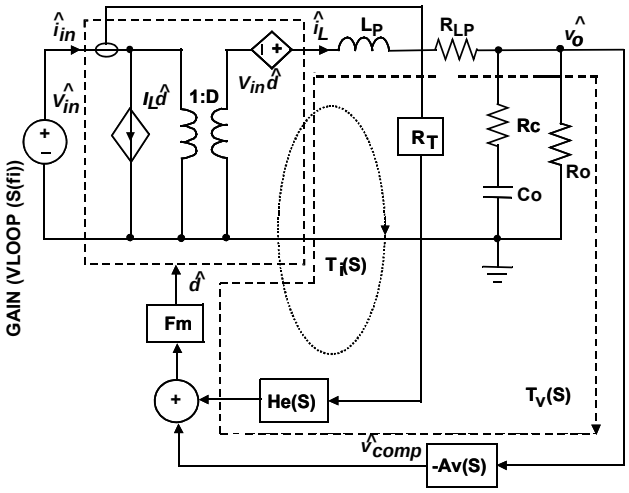


FIGURE 35. SMALL SIGNAL MODEL OF BUCK REGULATOR

PWM Comparator Gain F_m

The PWM comparator gain F_m for peak current mode control is given by Equation 20:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{(S_e + S_n)T_s} \quad \text{(EQ. 20)}$$

Where S_e is the slew rate of the slope compensation and S_n is given by Equation 21

$$S_n = R_t\frac{V_{in} - V_o}{L_P} \quad \text{(EQ. 21)}$$

Where R_t is the gain of the current amplifier.

Current Sampling Transfer Function $H_e(S)$

In current loop, the current signal is sampled every switching cycle. It has the following transfer function in Equation 22:

$$H_e(S) = \frac{S^2}{\omega_n^2} + \frac{S}{\omega_n Q_n} + 1 \quad \text{(EQ. 22)}$$

Where Q_n and ω_n are given by $Q_n = -\frac{2}{\pi}, \omega_n = \pi f_s$

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 23)}$$

Where

$$\omega_{esr} = \frac{1}{R_c C_o}, Q_p \approx R_o\sqrt{\frac{C_o}{L_P}}, \omega_o = \frac{1}{\sqrt{L_P C_o}}$$

Transfer function $F_2(S)$ from control to inductor current is given by Equation 24:

where $\omega_z = \frac{1}{R_o C_o}$.

$$F_2(S) = \frac{\hat{i}_o}{\hat{d}} = \frac{V_{in}}{R_o + R_{LP}}\frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 24)}$$

Current loop gain $T_i(S)$ is expressed as Equation 25:

$$T_i(S) = R_t F_m F_2(S) H_e(S) \quad \text{(EQ. 25)}$$

The voltage loop gain with open current loop is Equation 26:

$$T_v(S) = KF_m F_1(S) A_v(S) \quad \text{(EQ. 26)}$$

The Voltage loop gain with current loop closed is given by Equation 27:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)} \quad \text{(EQ. 27)}$$

If $T_i(S) >> 1$, then Equation 27 can be simplified as Equation 28:

$$L_v(S) = \frac{R_o + R_{LP}}{R_t}\frac{1 + \frac{S}{\omega_{esr}}}{1 + \frac{S}{\omega_p}}\frac{A_v(S)}{H_e(S)}, \omega_p \approx \frac{1}{R_o C_o} \quad \text{(EQ. 28)}$$

Equation 28 shows that the system is a single order system. Therefore, a simple type II compensator can be easily used to stabilize the system. While type III compensator is needed to expand the bandwidth for current mode control in some cases.

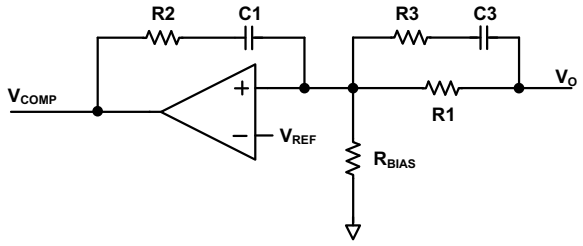


FIGURE 36. TYPE III COMPENSATOR

A compensator with 2 zeros and 1 pole is recommended for this part as shown in Figure 36. Its transfer function is expressed as Equation 29:

$$A_v(S) = \frac{\hat{v}_{comp}}{\hat{v}_O} = \frac{1}{SR_1C_1}\frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{\left(1 + \frac{S}{\omega_{cp}}\right)} \quad \text{(EQ. 29)}$$

where,

$$\omega_{cz1} = \frac{1}{R_2C_1}, \quad \omega_{cz2} = \frac{1}{(R_1 + R_3)C_3}, \omega_{cp} = \frac{1}{R_3C_3}$$

Compensator design goal:

Loop bandwidth f_c: $\left(\frac{1}{4}\text{to}\frac{1}{10}\right)f_s$

Gain margin: >10dB

Phase margin: 45°

The compensator design procedure is as follows:

1. Position ω_{CZ2} and ω_{CP} to derive R3 and C3.

Put the compensator zero ω_{CZ2} at (1 to 3)/(R_oC_o)

$$\omega_{cz2} = \frac{3}{R_oC_o} \quad \text{(EQ. 30)}$$

Put the compensator pole ω_{CP} at ESR zero or 0.35 to 0.5 times of switching frequency, whichever is lower. In all-ceramic-cap design, the ESR zero is normally higher than half of the switching frequency. R3 and C3 can be derived as following:

Case A: ESR zero $\frac{1}{2\pi R_cC_o}$ less than (0.35 to 0.5)f_s

$$C_3 = \frac{R_oC_o - 3R_cC_o}{3R_1} \quad \text{(EQ. 31)}$$

$$R_3 = \frac{3R_cR_1}{R_o - 3R_c} \quad \text{(EQ. 32)}$$

Case B: ESR zero $\frac{1}{2\pi R_cC_o}$ larger than (0.35 to 0.5)f_s

$$C_3 = \frac{0.33R_oC_of_s - 0.46}{f_sR_1} \quad \text{(EQ. 33)}$$

$$R_3 = \frac{R_1}{0.73R_oC_of_s - 1} \quad \text{(EQ. 34)}$$

Case C: Derive at R2 and C1.

The loop gain $L_V(S)$ at cross over frequency of f_c has unity gain. Therefore, C1 is determined by Equation 35.

$$C_1 = \frac{(R_1 + R_3)C3}{2\pi f_cR_tR_1C_o} \quad \text{(EQ. 35)}$$

The compensator zero ω_{CZ1} can boost the phase margin and bandwidth. To put ω_{CZ1} at 2 times of cross cover frequency f_c is a good start point. It can be adjusted according to specific design. R1 can be derived from Equation 36.

$$R_2 = \frac{1}{4\pi f_cC_1} \quad \text{(EQ. 36)}$$

Example: V_{IN} = 12V, V_o = 5V, I_o = 2A, f_s = 500kHz, C_o = 60µF/3mΩ, L = 10µH, R_t = 0.20V/A, f_c = 50kHz, R_1 = 105k, R_{BIAS} = 20kΩ.

Select the crossover frequency to be 35kHz. Since the output capacitors are all ceramics, use Equations 33 and 34 to derive R3 to be 20k and C3 to be 470pF.

Then use Equations 35 and 36 to calculate C_1 to be 180pF and R_2 to be 12.7k. Select 150pF for C_1 and 15k for R_2.

There is approximately 30pF parasitic capacitance between COMP to FB pins that contributes to a high frequency pole. Any extra external capacitor is not recommended between COMP and FB.

Figure 37 shows the simulated bode plot of the loop. It is shown that it has 26kHz loop bandwidth with 70° phase margin and -28dB gain margin.

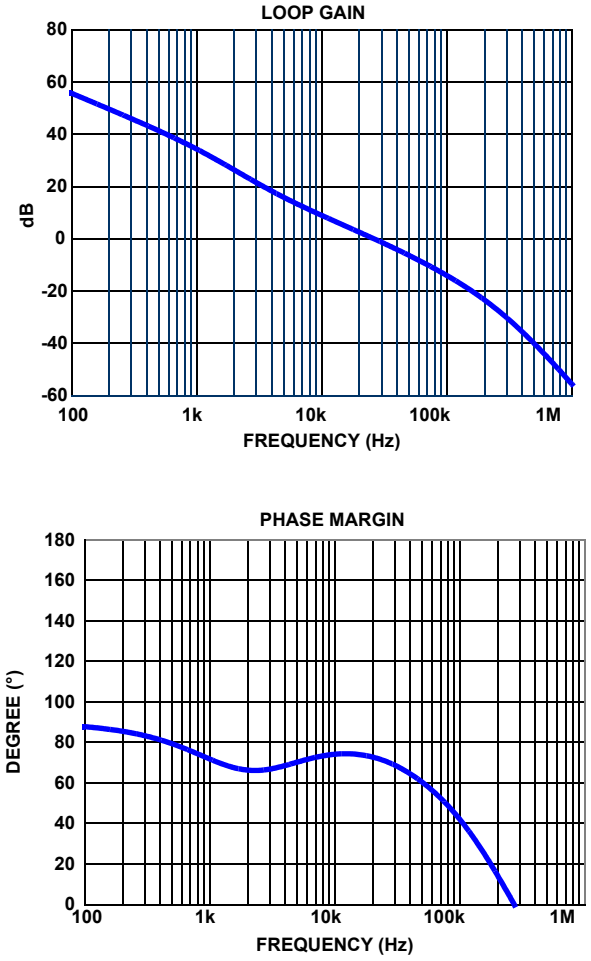


FIGURE 37. SIMULATED LOOP BODE PLOT

Note in applications where the PFM mode is desired especially when type III compensation network is used, the value of the capacitor between the COMP pin and the FB pin (not the capacitor in series with the resistor between COMP and FB) should be minimal to reduce the noise coupling for proper PFM operation. No external capacitor between COMP and FB is recommended at PFM applications.

In PFM mode operations, a RC filter from FB to ground (R in series with C, connecting from FB to ground) may help to reduce the noise effects injected to FB pin. The recommended values for the filter is 499Ω to 1k for the R and 470pF for the C.

Loop Compensation Design for 2-Stage Boost Buck and Single-Stage Buck Boost

For 2-stage boost buck and single-stage non-inverting buck boost configurations, it's highly recommended to use the iSim model (The ISL78200 iSim model can be used to simulate ISL78201 and it's available through internet) to evaluate the loop bandwidth and phase margin.

Layout Suggestions

1. Put the input ceramic capacitors as close to the IC VIN pin and power ground connecting to the power MOSFET or diode. Keep this loop (input ceramic capacitor, IC V_{IN} pin and MOSFET/diode) as tiny as possible to achieve the least voltage spikes induced by the trace parasitic inductance.
2. Put the input aluminum capacitors close to IC VIN pin.
3. Keep the phase node copper area small but large enough to handle the load current.
4. Put the output ceramic and aluminum capacitors also close to the power stage components.
5. Put vias (20 recommended) in the bottom pad of the IC. The bottom pad should be placed in the ground copper plane with an area as large as possible in multiple layers to effectively reduce the thermal impedance.
6. Place the 4.7µF ceramic decoupling capacitor at the VCC pin and as close as possible to the IC. Put multiple vias (≥3) close to the ground pad of this capacitor.
7. Keep the bootstrap capacitor close to the IC.
8. Keep the LGATE drive trace as short as possible and try to avoid using a via in the LGATE drive path to achieve the lowest impedance.
9. Place the positive voltage sense trace close to the load for tighter regulation.
10. Place all the peripheral control components close to the IC.

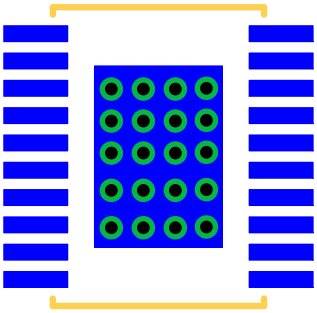


FIGURE 38. PCB VIA PATTERN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 31, 2015	FN8615.1	On page 6, updated Charged Device Model test method from “JESD22-C101E” to “AEC-Q100-11”.
February 18, 2014	FN8615.0	Initial Release

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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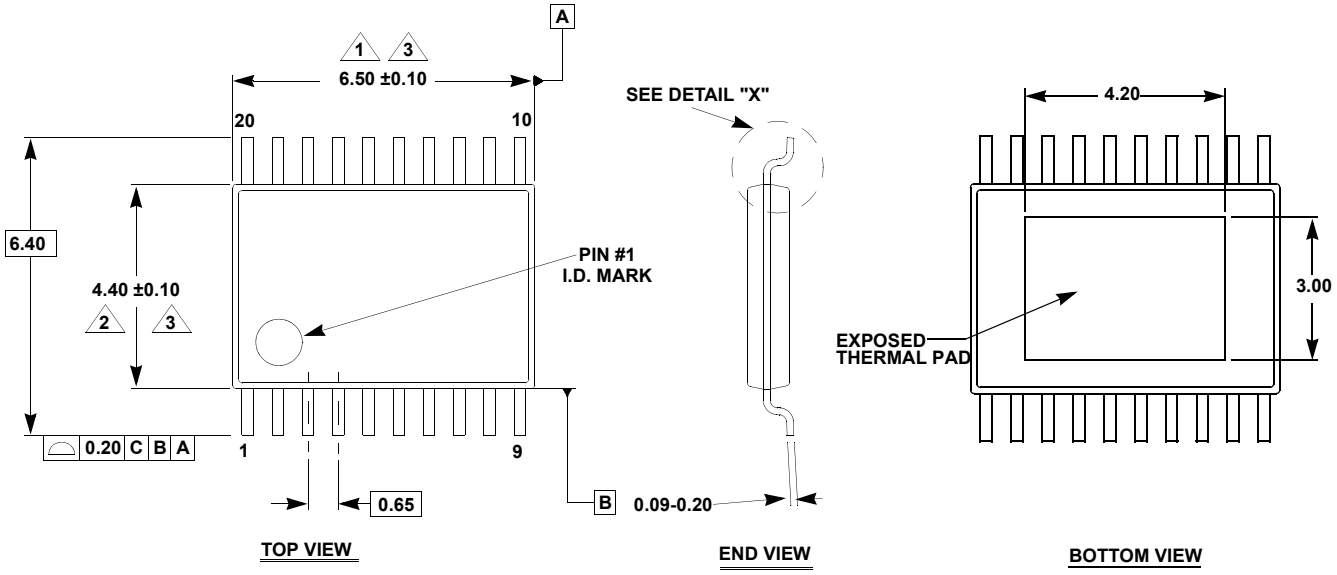
Package Outline Drawing

M20.173A

20 LEAD HEAT-SINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)

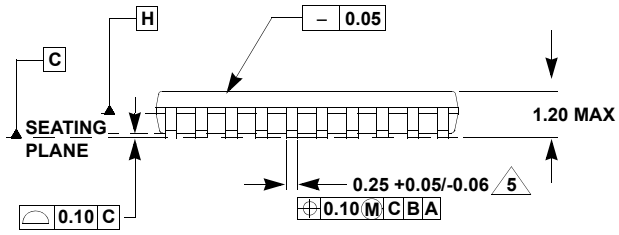
Rev 0, 8/13



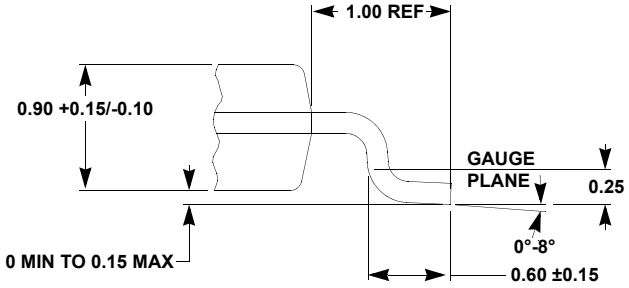
TOP VIEW

END VIEW

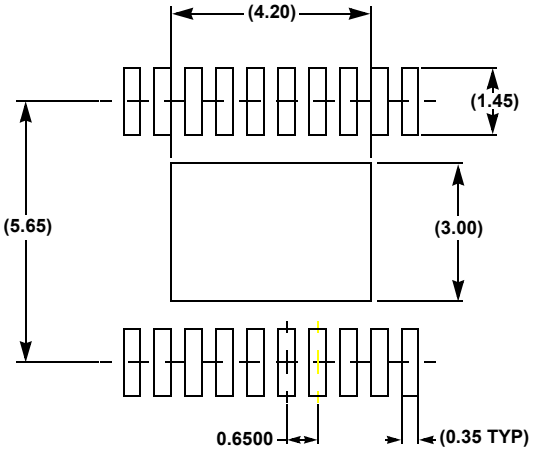
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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