High Performance 2A and 3A Linear Regulators

ISL80102, ISL80103

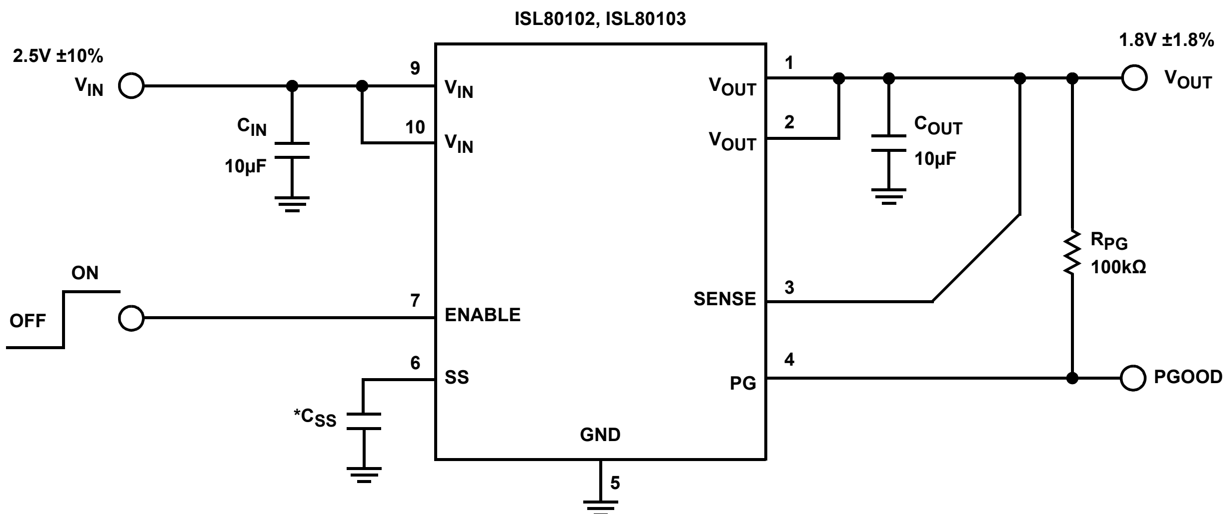
The ISL80102 and ISL80103 are low voltage, high-current, single output LDOs specified for 2A and 3A output current, respectively. These LDOs operate from the input voltages of 2.2V to 6V and are capable of providing the output voltages of 0.8V to 5V on the adjustable V_{OUT} versions. Fixed output voltage options are available in 1.8V, 2.5V, 3.3V and 5V. Other custom voltage options available upon request.

For applications that demand in-rush current less than the current limit, an external capacitor on the soft-start pin provides adjustment. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode. A sub-micron BiCMOS process is utilized for this product family to deliver the best in class analog performance and overall value.

These CMOS (LDOs) will consume significantly lower quiescent current as a function of load over bipolar LDOs, which translates into higher efficiency and the ability to consider packages with smaller footprints. The quiescent current has been modestly compromised to enable a leading class fast load transient response, and hence a lower total AC regulation band for an LDO in this category.

Features

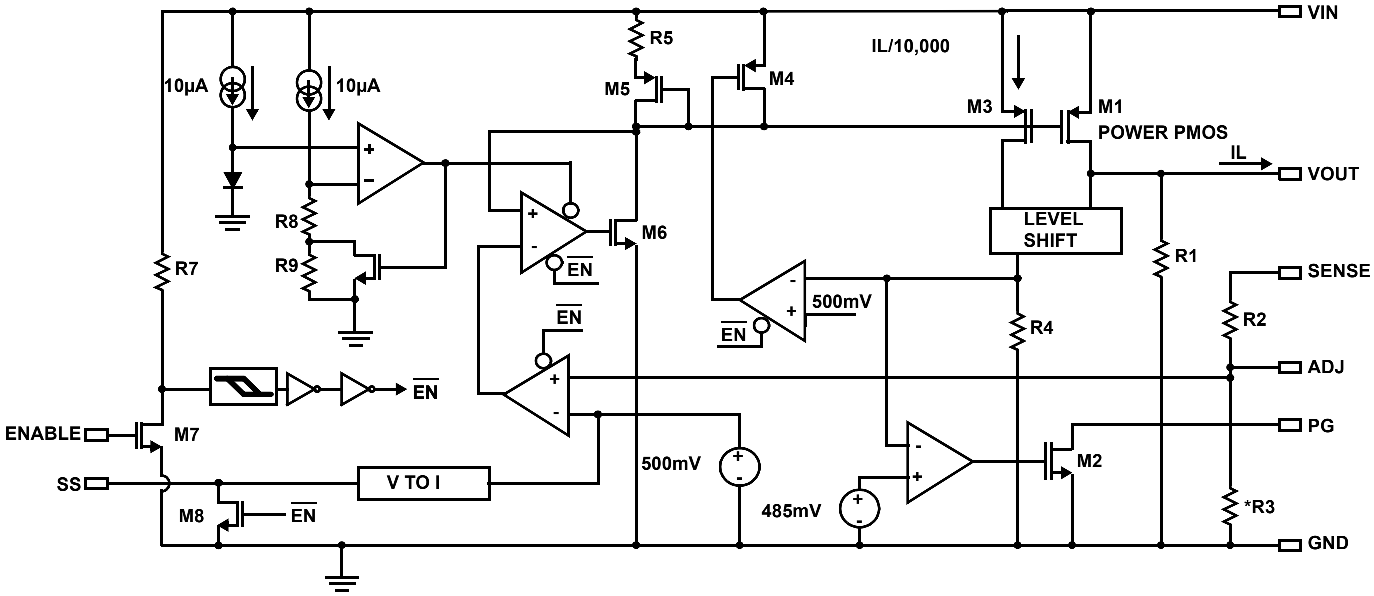
- Stable with all capacitor types (Note 10)
- 2A and 3A output current ratings
- 2.2V to 6V input voltage range
- ±1.8% V_{OUT} accuracy guaranteed over line, load and T_J = -40°C to +125°C
- Very low 120mV dropout voltage at 3A (ISL80103)
- Fixed and adjustable V_{OUT} versions
- Very fast transient response
- Excellent 62dB PSRR
- 100µV_{RMS} output noise
- Power-good output
- Adjustable in-rush current limiting
- Short circuit and over-temperature protection
- Available in a 10 Ld DFN
- Servers
- Telecommunications and networking
- Medical equipment
- Instrumentation systems
- Routers and switchers



*CSS is optional, (see Note 11) on page 5.

FIGURE 1. TYPICAL APPLICATION

Block Diagram



*R3 is open for ADJ versions.

Ordering Information

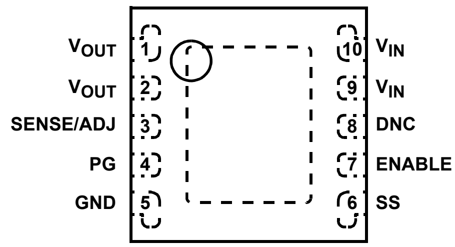
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} VOLTAGE	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL80102IRAJZ	DZJA	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR18Z	DZNA	1.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR25Z	DZPA	2.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IRAJZ	DZAA	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR18Z	DZEA	1.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR25Z	DZFA	2.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102EVAL2Z	Evaluation Board				
ISL80103EVAL2Z	Evaluation Board				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL80102, ISL80103. For more information on MSL please see tech brief TB363.

Pin Configuration

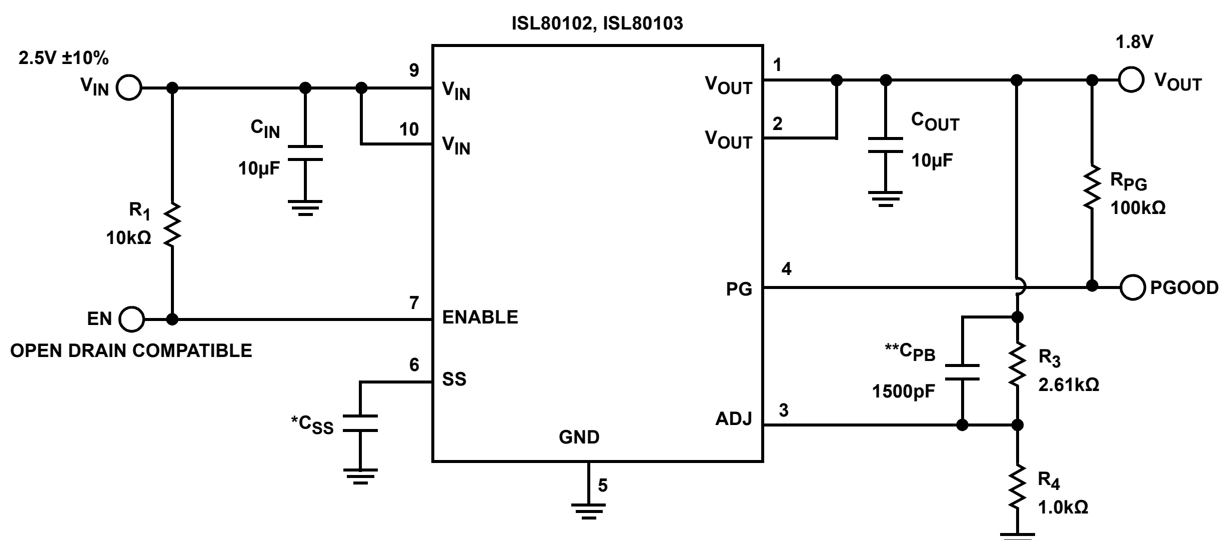
ISL80102, ISL80103
(10 LD 3x3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	VOUT	Output voltage pin.
3	SENSE/ADJ	Remote voltage sense for internally fixed VOUT options. ADJ pin for externally set VOUT.
4	PG	VOUT in regulation signal. Logic low defines when VOUT is not in regulation. Must be grounded if not used.
5	GND	GND pin.
6	SS	External cap adjusts in-rush current.
7	ENABLE	VIN independent chip enable. TTL and CMOS compatible.
8	DNC	Do not connect this pin to ground or supply. Leave floating.
9, 10	VIN	Input supply pin.
	EPAD	EPAD must be connected to copper plane with as many vias as possible for proper electrical and optimal thermal performance.

Typical Application



*CSS is optional, (see Note 11) on page 5.

**C_{PB} is optional. See “Functional Description” on page 12 for more information.

FIGURE 2. TYPICAL APPLICATION DIAGRAM

Absolute Maximum Ratings (Note 6)

V_{IN} Relative to GND . . . . . -0.3V to +6.5V
V_{OUT} Relative to GND . . . . . -0.3V to +6.5V
PG, ENABLE, SENSE/ADJ, SS, Relative to GND. . . . . -0.3V to +6.5V

Recommended Operating Conditions (Note 8)

Junction Temperature Range (T_J) . . . . . -40°C to +125°C
VIN Relative to GND . . . . . 2.2V to 6V
V_{OUT} Range . . . . . 800mV to 5V
PG, ENABLE, SENSE/ADJ, SS Relative to GND . . . . . 0V to 6V
PG Sink Current 10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 4, 5).	45	4

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. ABS max voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
7. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10µF$, $T_J = +25°C$, $I_{LOAD} = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 12 and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} Options: 1.8V. V_{IN} =2.2V; I_{LOAD} = 0A		0.5		%
		V_{OUT} Options: 1.8V. 2.2V < V_{IN} < 3.6V; 0A < I_{LOAD} < 3A	**-1.8**		**1.8**	%
		V_{OUT} Options: 2.5V V_{IN} =V_{OUT} + 0.4V; I_{LOAD} = 0A		0.5		%
		V_{OUT} Options: 2.5V V_{OUT} + 0.4V < V_{IN} < 6V; 0A < I_{LOAD} < 3A	**-1.8**		**-1.8**	%
Feedback Pin (ADJ Version)	V_{FB}	2.2V < V_{IN} < 6V, 0A < I_{LOAD} < 3A	**491**	500	**509**	mV
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 0.4V < V_{IN} < 3.6V, V_{OUT} = 1.8V		0.1	**0.4**	%
		V_{OUT} + 0.4V < V_{IN} < 6V, V_{OUT} = 2.5V		0.1	**0.8**	%
DC Output Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	0A < I_{LOAD} < 3A, All voltage options	**-0.8**			%
		0A < I_{LOAD} < 2A, All voltage options	**-0.6**			%
Feedback Input Current		V_{ADJ} = 0.5V		0.01	**1**	µA
Ground Pin Current	I_Q	I_{LOAD} = 0A, 2.2V < V_{IN} < 6V		7.5	**9**	mA
		I_{LOAD} = 3A, 2.2V < V_{IN} < 6V		8.5	**12**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0.2V, V_{IN} = 5V		0.4		µA
		ENABLE Pin = 0.2V, V_{IN} = 6V		3.3	**16**	µA
Dropout Voltage (Note 9)	V_{DO}	I_{LOAD} = 3A, V_{OUT} = 2.5V, 10 LD 3x3 DFN		120	**185**	mV
		I_{LOAD} = 2A, V_{OUT} = 2.5V, 10 LD 3x3 DFN		81	**125**	mV
Output Short Circuit Current (3A Version)	ISC	V_{OUT} = 0V, V_{OUT} + 0.4V < V_{IN} < 6V		5.0		A
Output Short Circuit Current (2A Version)		V_{OUT} = 0V, V_{OUT} + 0.4V < V_{IN} < 6V		2.8		A

Electrical Specifications Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10µF$, $T_J = +25°C$, $I_{LOAD} = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 12 and Tech Brief TB379.
Boldface limits apply over the operating temperature range, -40°C to +125°C. Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Thermal Shutdown Temperature	TSD	V_{OUT} + 0.4V < V_{IN} < 6V		160		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	V_{OUT} + 0.4V < V_{IN} < 6V		15		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, I_{LOAD} = 1A; V_{IN} = 2.2V		55		dB
		f = 120Hz, I_{LOAD} = 1A; V_{IN} = 2.2V		62		dB
Output Noise Voltage		I_{LOAD} = 10mA, BW = 300Hz < f < 300kHz		100		$µV_{RMS}$
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold	$V_{EN(HIGH)}$	2.2V < V_{IN} < 6V	**0.616**	0.8	**0.95**	V
Turn-off Threshold	$V_{EN(LOW)}$	2.2V < V_{IN} < 6V	**0.463**	0.6		V
Hysteresis	$V_{EN(HYS)}$	2.2V < V_{IN} < 6V		135		mV
Enable Pin Turn-on Delay	t_{EN}	C_{OUT} = 10µF, I_{LOAD} = 1A		150		µs
Enable Pin Leakage Current		V_{IN} = 6V, EN = 3V			**1**	µA
SOFT-START CHARACTERISTICS						
Reset Pull-Down resistance	R_{PD}			323		Ω
Soft-Start Charge Current	I_{CHG}		**-7**	-4.5	**-2**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	84	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		I_{SINK} = 500µA		47	**100**	mV
PG Flag Leakage Current		V_{IN} = 6V, PG = 6V		0.05	**1**	µA

NOTES:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.
10. Minimum cap of 10µF X5R/X7R on V_{IN} and V_{OUT} required for stability.
11. If the current limit for in-rush current is acceptable in application, do not use this feature. Used only when large bulk capacitance required on V_{OUT} for application.

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

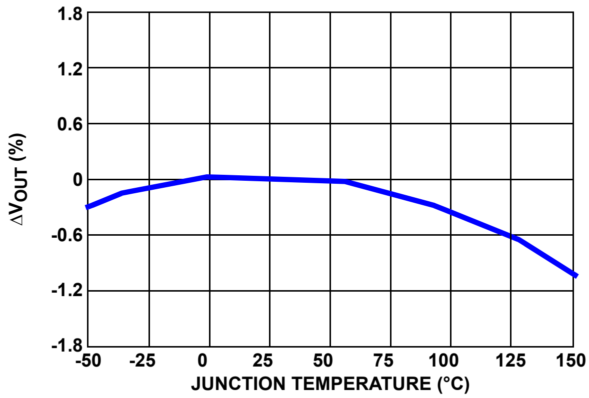


FIGURE 3. ΔV_{OUT} vs TEMPERATURE

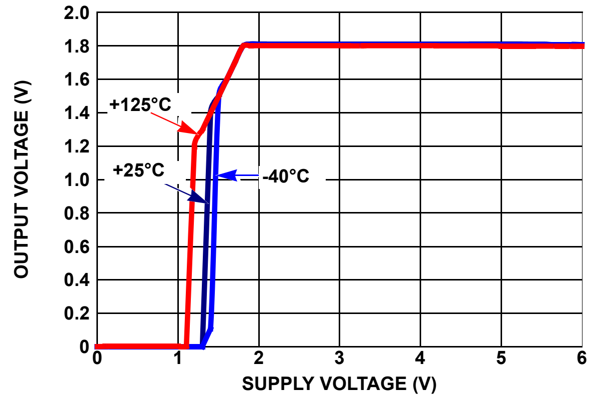


FIGURE 4. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

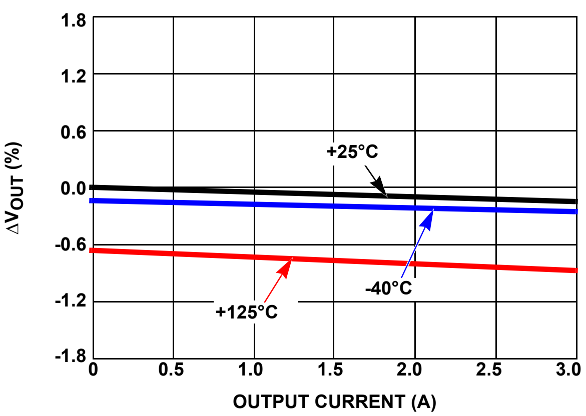


FIGURE 5. ΔV_{OUT} vs OUTPUT CURRENT

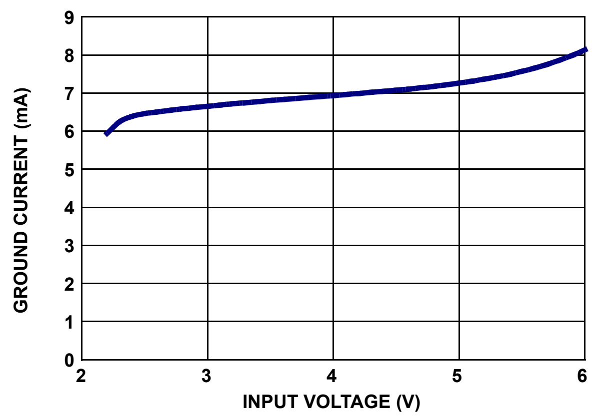


FIGURE 6. GROUND CURRENT vs SUPPLY VOLTAGE

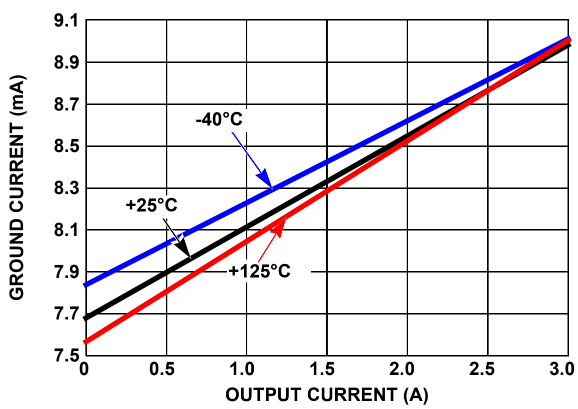


FIGURE 7. GROUND CURRENT vs OUTPUT CURRENT

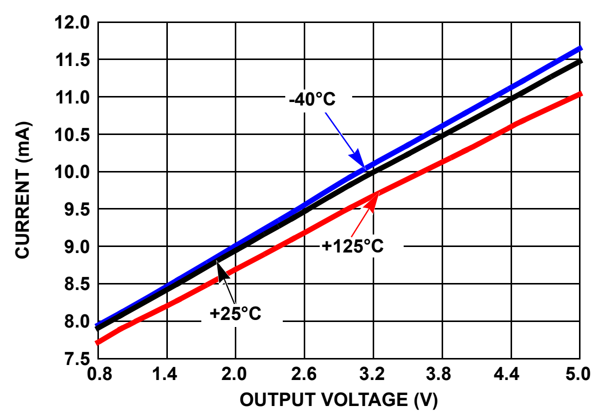


FIGURE 8. GROUND CURRENT vs OUTPUT VOLTAGE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

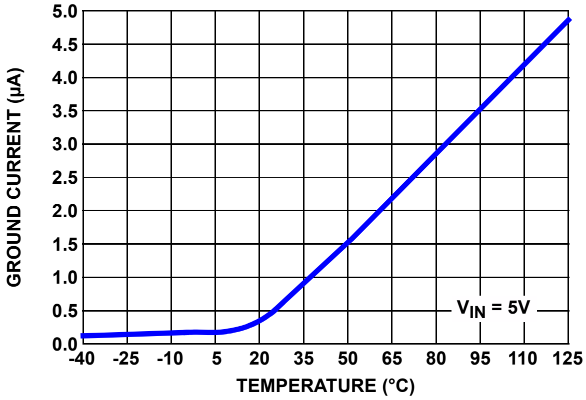


FIGURE 9. SHUTDOWN CURRENT vs TEMPERATURE

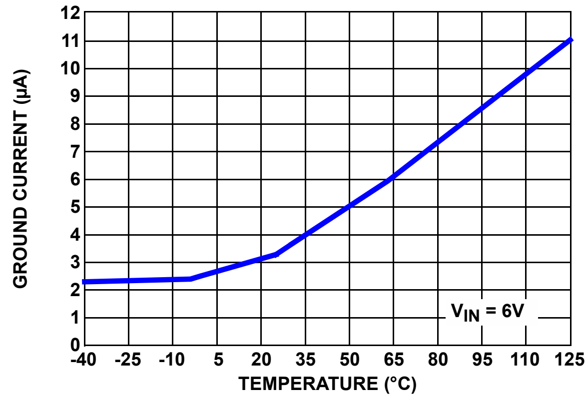


FIGURE 10. SHUTDOWN CURRENT vs TEMPERATURE

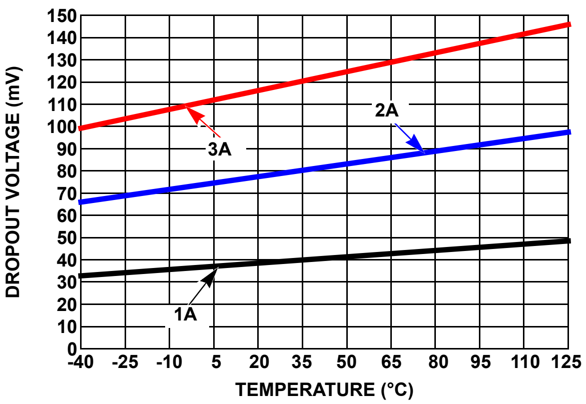


FIGURE 11. DROPOUT VOLTAGE vs TEMPERATURE

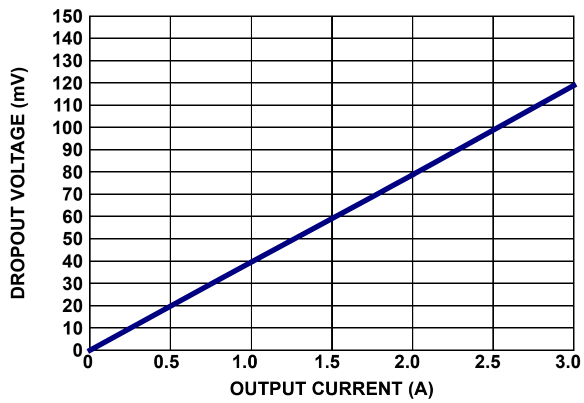


FIGURE 12. DROPOUT VOLTAGE vs OUTPUT CURRENT

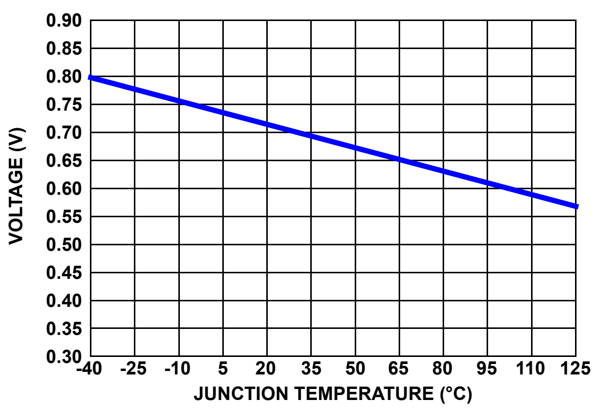


FIGURE 13. ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

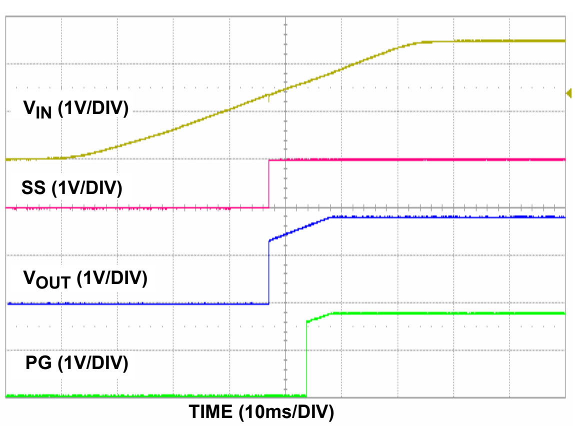


FIGURE 14. POWER-UP (V_{IN} = 2.2V)

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

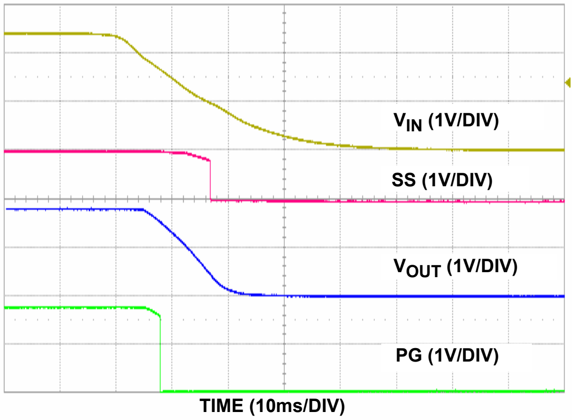


FIGURE 15. POWER-DOWN (V_{IN} = 2.2V)

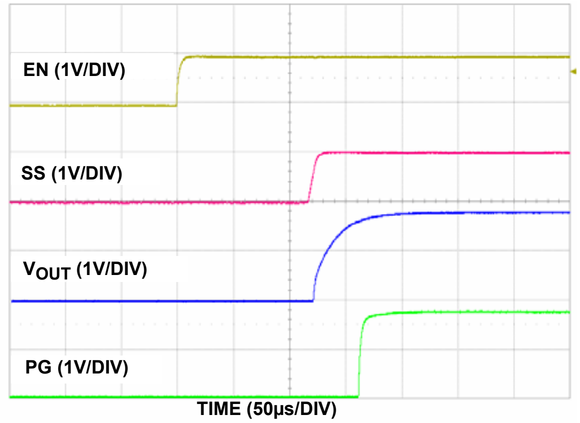


FIGURE 16. ENABLE START-UP

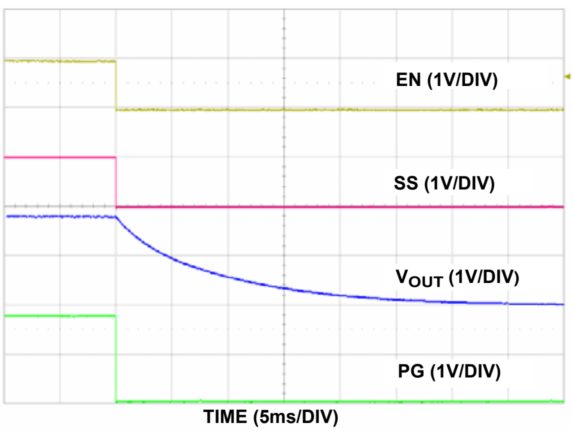


FIGURE 17. ENABLE SHUTDOWN

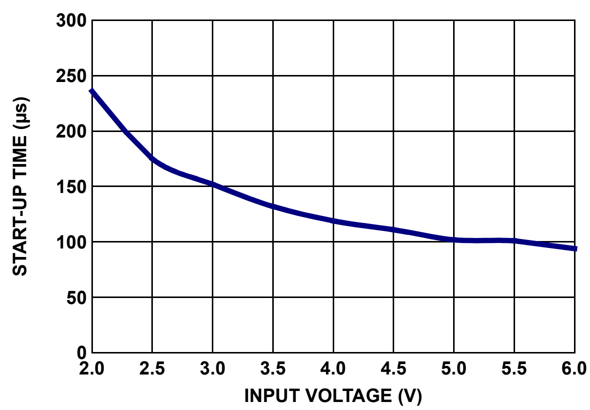


FIGURE 18. START-UP TIME vs SUPPLY VOLTAGE

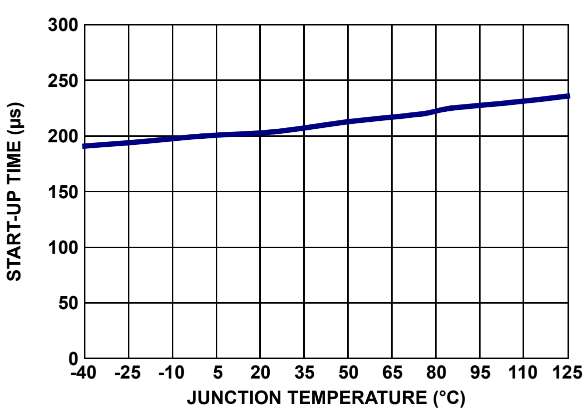


FIGURE 19. START-UP TIME vs TEMPERATURE

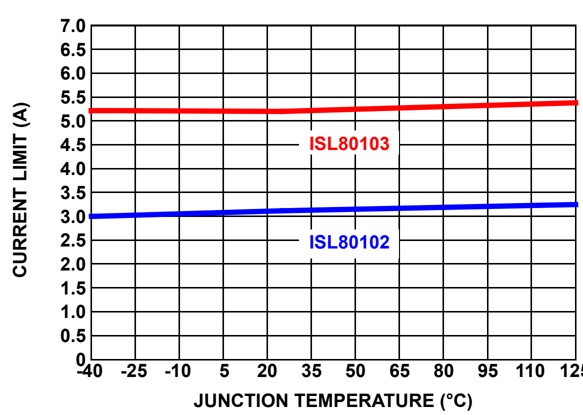


FIGURE 20. CURRENT LIMIT vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

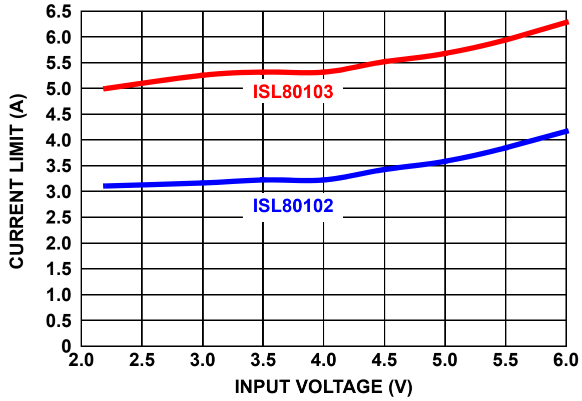


FIGURE 21. CURRENT LIMIT vs SUPPLY VOLTAGE

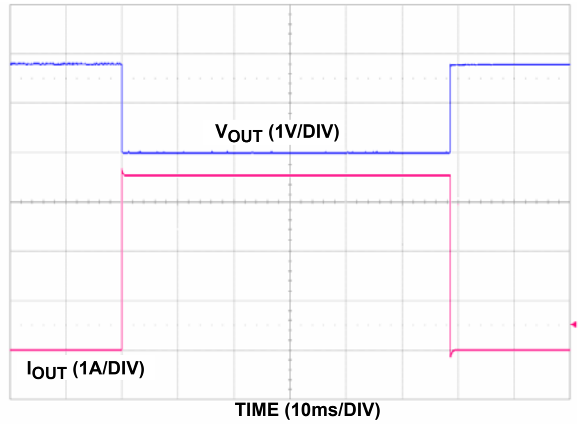


FIGURE 22. CURRENT LIMIT RESPONSE (ISL80102)

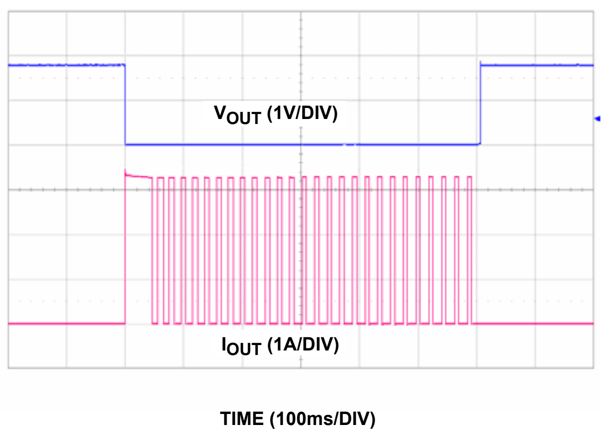


FIGURE 23. THERMAL CYCLING (ISL80102)

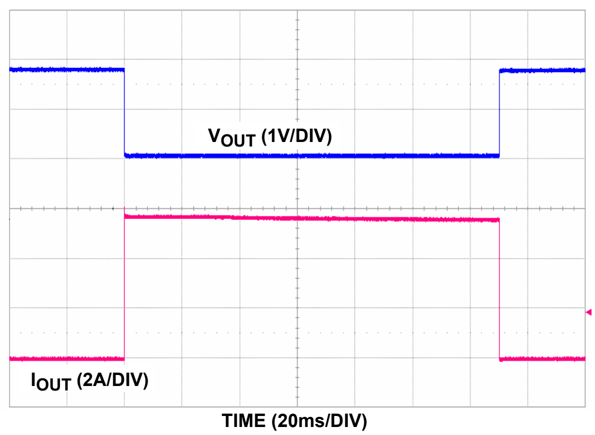


FIGURE 24. CURRENT LIMIT RESPONSE (ISL80103)

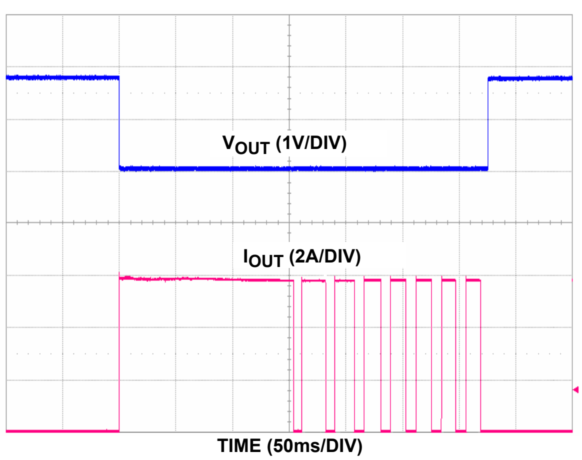


FIGURE 25. THERMAL CYCLING (ISL80103)

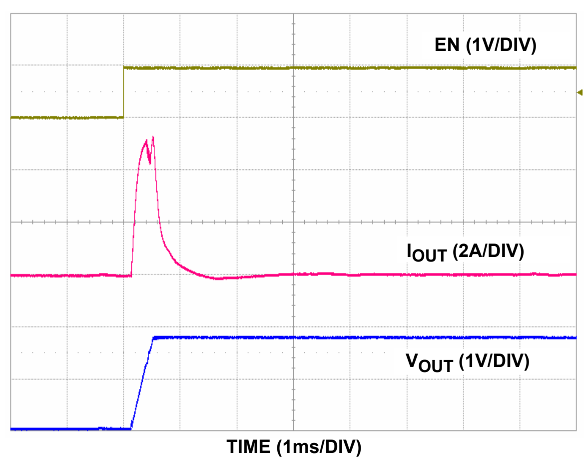


FIGURE 26. IN-RUSH CURRENT WITH NO SOFT-START CAPACITOR, C_{OUT} = 1000µF

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

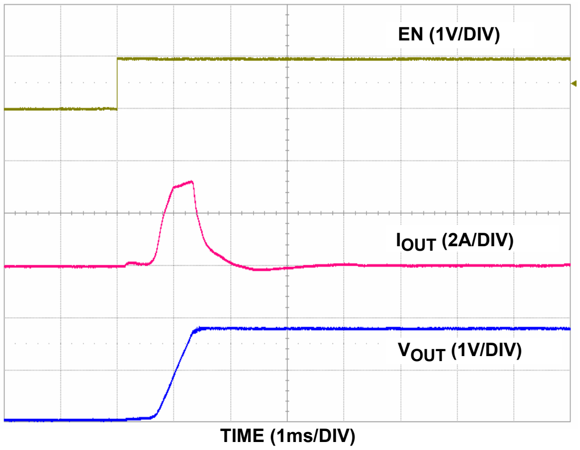


FIGURE 27. IN-RUSH WITH 22nF SOFT-START CAPACITOR, C_{OUT} = 1000µF

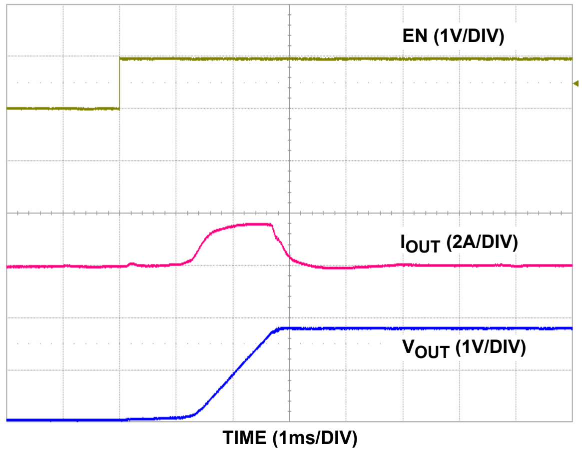


FIGURE 28. IN-RUSH WITH 47nF SOFT-START CAPACITOR, C_{OUT} = 1000µF

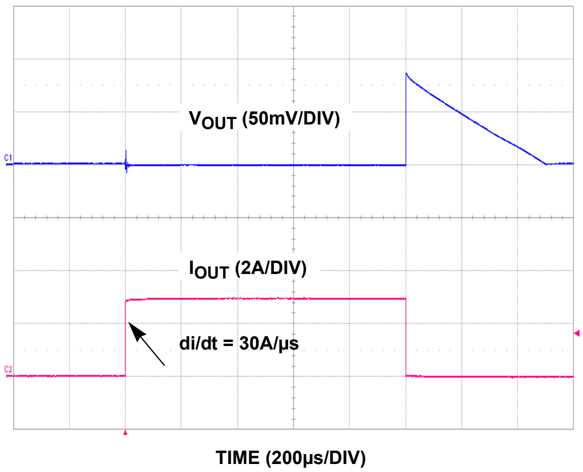


FIGURE 29. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC

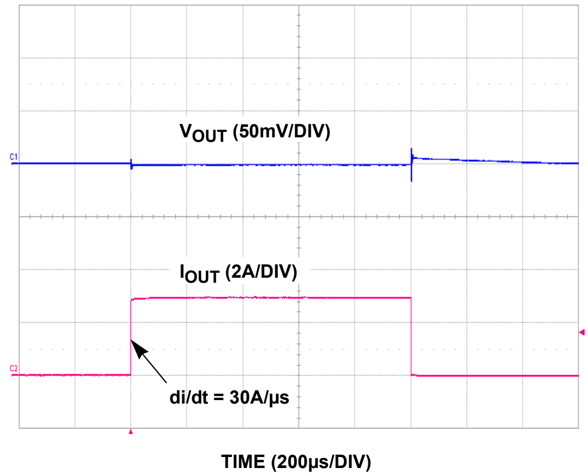


FIGURE 30. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC + 100µF OSCON

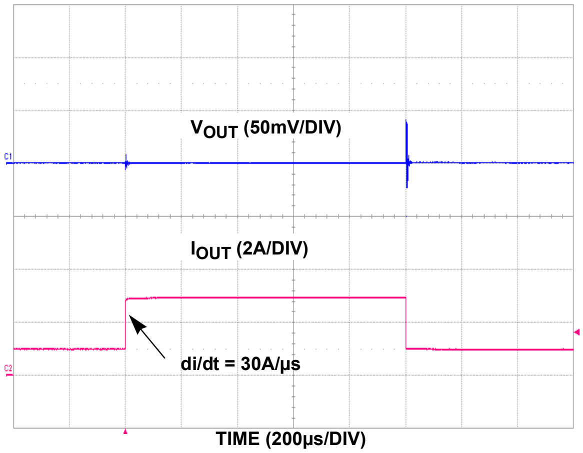


FIGURE 31. LOAD TRANSIENT 1A TO 3A, C_{OUT} = 10µF CERAMIC

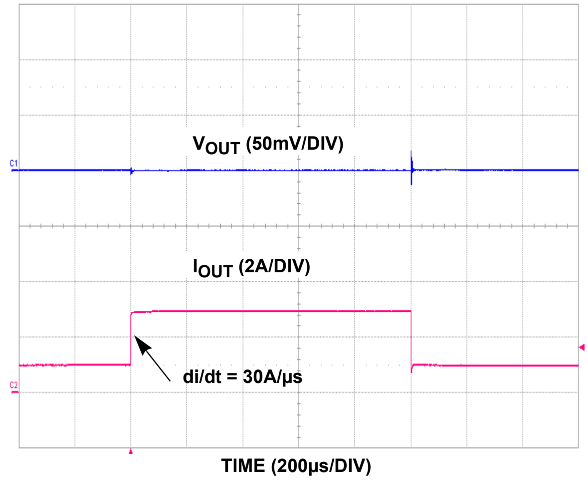


FIGURE 32. LOAD TRANSIENT 1A TO 3A, C_{OUT} = 10µF CERAMIC + 100µF OSCON

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

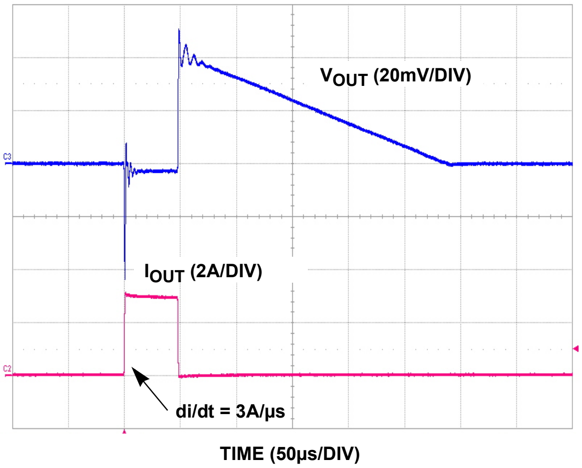


FIGURE 33. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, NO C_{PB} (ADJ VERSION)

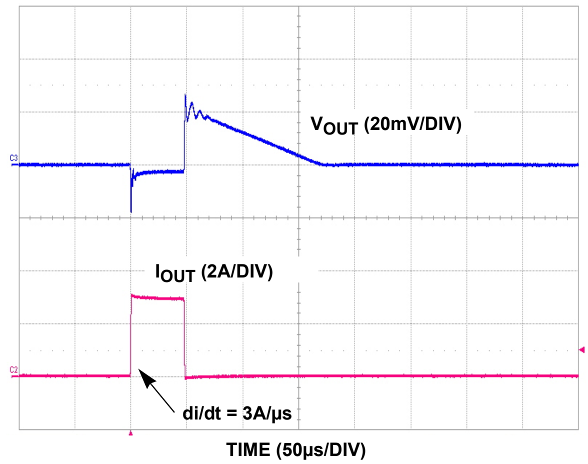


FIGURE 34. LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, C_{PB} = 1500pF (ADJ VERSION)

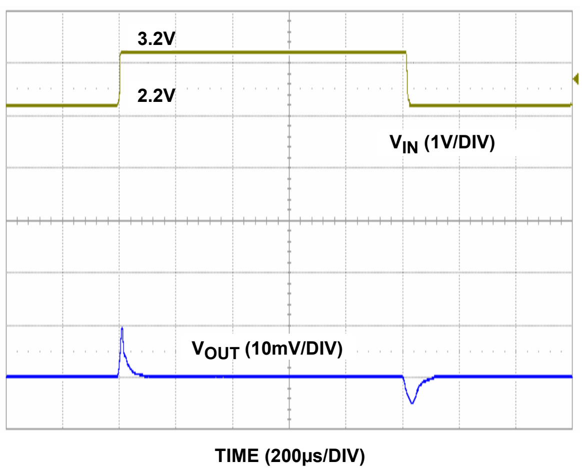


FIGURE 35. LINE TRANSIENT

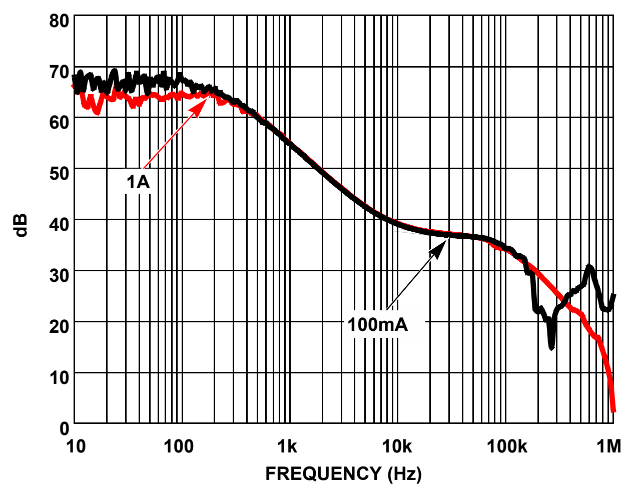


FIGURE 36. PSRR vs LOAD

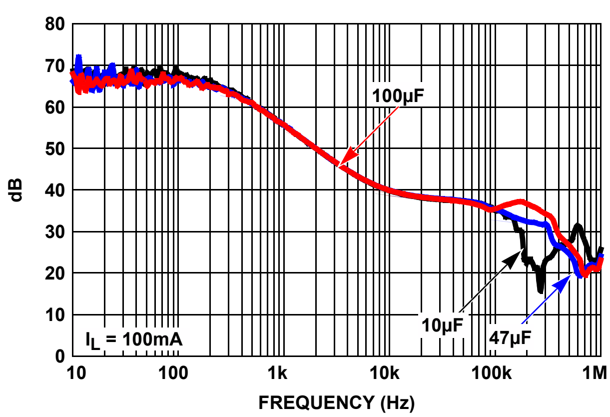


FIGURE 37. PSRR vs C_{OUT}

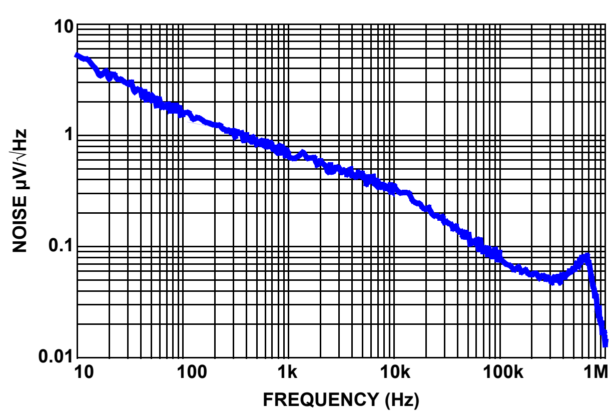


FIGURE 38. SPECTRAL NOISE DENSITY vs FREQUENCY

Functional Description

Input Voltage Requirements

Despite other output voltages offered, this family of LDOs is optimized for a true 2.5V to 1.8V conversion where the input supply can have a tolerance of as much as ±10% for conditions noted in the "Electrical Specifications" table on page 4. Minimum guaranteed input voltage is 2.2V, however, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The dropout spec of this family of LDOs has been generously specified in order to allow applications to design for a level of efficiency that can accommodate the smaller outline package.

Enable Operation

The Enable turn-on threshold is typically 770mV with a hysteresis of 135mV. An internal pull-up or pull-down resistor is available upon request. As a result, this pin must not be left floating. This pin must be tied to V_{IN} if it is not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the Enable pin. The Enable pin may be connected directly to V_{IN} for applications that are always on.

Power-Good Operation

Applications not using this feature must connect this pin to ground. The PGOOD flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PGOOD pin requires an external pull-up resistor, which is typically connected to the VOUT pin. The PGOOD pin should not be pulled up to a voltage source greater than V_{IN}. The PGOOD fault can be caused by the output voltage going below 84% of the nominal output voltage, or the current limit fault, or low input voltage. The PGOOD does not function during thermal shutdown. While the PGOOD functions in shutdown.

Soft-Start Operation (Optional)

If the current limit for in-rush current is acceptable in the application, do not use this feature. The soft-start circuit controls the rate at which the output voltage comes up to regulation at power-up or LDO enable. A constant current charges an external soft-start capacitor. The external capacitor always gets discharged to ground pin potential at the beginning of start-up or enabling. The discharge rate is the RC time constant of R_{PD} and C_{SS}. See Figures 26 through 29 in the "Typical Operating Performance Curves" beginning on page 6. R_{PD} is the ON-resistance of the pull down MOSFET, M8. R_{PD} is 300Ω typically.

The soft-start feature effectively reduces the in-rush current at power-up or LDO enable until V_{OUT} reaches regulation. The in-rush current can be an issue for applications that require large, external bulk capacitances on V_{OUT} where high levels of charging current can be seen for a significant period of time. The in-rush currents can cause V_{IN} to drop below minimum which could cause V_{OUT} to shutdown. Figure 39 shows the relationship between in-rush current and C_{SS} with a C_{OUT} of 1000µF.

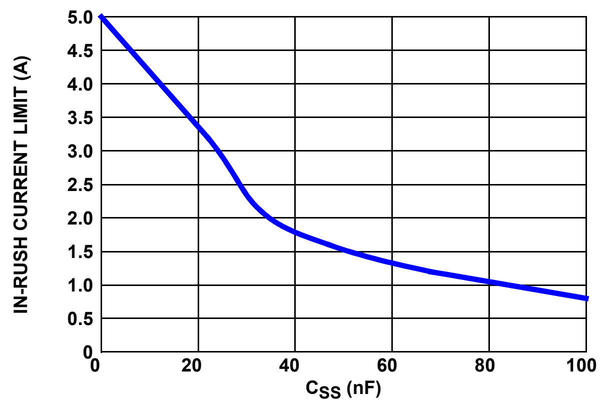


FIGURE 39. IN-RUSH CURRENT vs SOFT-START CAPACITANCE

Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 5V. An external resistor divider, R_3 and R_4, is used to set the output voltage as shown in Equation 1. The recommended value for R_4 is 500Ω to 1kΩ. R_3 is then chosen according to Equation 2:

$$V_{OUT} = 0.5V \times \left(\frac{R_3}{R_4} + 1\right) \quad \text{(EQ. 1)}$$

$$R_3 = R_4 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 2)}$$

External Capacitor Requirements

External capacitors are required for proper operation. To ensure optimal performance careful attention must be paid to the layout guidelines and selection of capacitor type and value.

OUTPUT CAPACITOR

The ISL80102, ISL80103 applies state-of-the-art internal compensation to keep selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a 10µF X5R/X7R is used for local bypass on V_{OUT}. This minimum capacitor must be connected to V_{OUT} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

Lower cost Y5V and Z5U type ceramic capacitors are acceptable if the size of the capacitor is larger to compensate for the significantly lower tolerance over X5R/X7R types. Additional capacitors of any value in Ceramic, POSCAP or Alum/Tantalum Electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

The minimum input capacitor required for proper operation is 10µF having a ceramic dielectric. This minimum capacitor must be connected to V_{IN} and ground pins of the LDO with PCB traces no longer than 0.5cm.

Phase Boost Capacitor (Optional)

The ISL80102 and ISL80103 are designed to be stable with 10µF or larger ceramic capacitor.

Applications using the ADJ versions, may see improved performance with the addition of a small ceramic capacitor C_{PB} as shown in Figure 2 on page 3. The conditions where C_{PB} may be beneficial are: (1) $V_{OUT} > 1.5V$, (2) C_{OUT} = 10µF, and (3) tight AC voltage regulation band.

C_{PB} introduces phase lead with the product of R_3 and C_{PB} that results in increasing the bandwidth of the LDO. Typical R3 x C_{PB} should be 4µs.

C_{PB} not recommended for $V_{OUT} < 1.5V$.

Current Limit Protection

The ISL80102, ISL80103 family of LDOs incorporates protection against overcurrent due to short, overload condition applied to the output and the in-rush current that occurs at start-up. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the "Electrical Specifications" table on page 4. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition, the LDO might begin to cycle on and off due to the die temperature exceeding the thermal fault condition. The TO220/TO263 package will tolerate higher levels of power dissipation on the die which may never thermal cycle if the heatsink of this larger package can keep the die temperature below the specified typical thermal shutdown temperature.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions (Note 8)" on page 4. The power dissipation can be calculated by using Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 3)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ will determine the maximum allowable power dissipation as shown in Equation 4:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 4)}$$

Where θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, please make sure that power dissipation calculated in Equation 3, P_D be less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heatsink. The EPAD of this package must be soldered to the copper plane (GND plane) for heat sinking. Figure 40 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

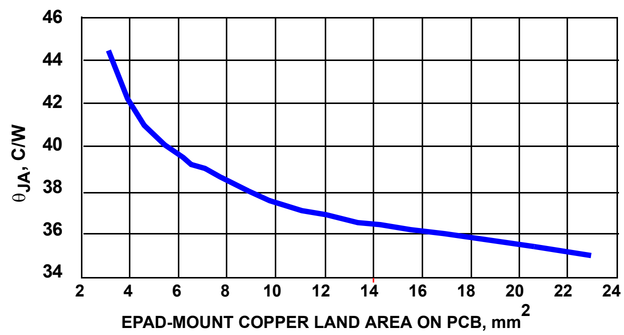


FIGURE 40. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

In the event the die temperature exceeds typically +160°C, then the output of the LDO will shut down until the die temperature can cool down to typically +145°C. The level of power combined with the thermal impedance of the package (+48°C/W for DFN) will determine if the junction temperature exceeds the thermal shutdown temperature.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
May 23, 2013	FN6660.6	Pin Descriptions on page page 3, updated EPAD section From: EPAD at ground potential. Soldering it directly to GND plane is optional. To: EPAD must be connected to copper plane with as many vias as possible for proper electrical and optimal thermal performance. Removed obsolete part numbers: ISL80102IR33Z, ISL80102IR50Z, ISL80103IR33Z, ISL80103IR50Z from ordering information table on page 2. Added evaluation boards to ordering information table on page 2: ISL80103IR50Z and ISL80103EVAL2Z. Features on page 1: Removed 5 Ld TO220 and 5 Ld TO263. Input Voltage Requirements on page 12: Removed the sentence “those applications that cannot accommodate the profile of the TO220/TO263”.
June 14, 2012	FN6660.5	In “Thermal Information” on page 4, corrected θ_{JA} from 48 to 45.
February 14, 2012	FN6660.4	Increased “VEN(HIGH)” minimum limit from 0.4V to 0.616 and added the “VEN(LOW)” spec for clarity on page 5.
December 14, 2011	FN6660.3	Increased “Turn-on Threshold” minimum limit on page 5 from 0.3V to 0.4V. Updated “Package Outline Drawing” on page 16 as follows: Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly.
March 4, 2011	FN6660.2	Converted to new template On page 1 - first paragraph, changed "Fixed output voltage options are available in 1.5V, 1.8V, 2.5V, 3.3V and 5V" to "Fixed output voltage options are available in 1.8V, 2.5V, 3.3V and 5V" In “Ordering Information” table on page 2, removed ISL80102IR15Z and ISL80103IR15Z. In Note 3 on page 2, below the “Ordering Information” table , removed '1.5V', so it reads “The 3.3V and 5V fixed output voltages will be released in the future. Please contact Intersil Marketing for more details.”
March 4, 2010	FN6660.1	Corrected Features on page 1 as follows: -Changed bullet "• 185mV Dropout @ 3A, 125mV Dropout @ 2A" to "• Very Low 120mV Dropout at 3A" -Changed bullet "• 65dB Typical PSRR" to "• 62dB Typical PSRR" -Deleted 0.5% Initial VOUT Accuracy Modified Figure 1 and placed as “TYPICAL APPLICATION” on page 1. Moved Pinout to page 3 In “Block Diagram” on page 2, corrected resistor associated with M5 from R4 to R5 Updated “Block Diagram” on page 2 as follows” - Added M8 from SS to ground. Updated Figure 1 on page 1 as follows: -Corrected Pin 6 from SS to IRSET -Removed Note 11 callout "Minimum cap on VIN and VOUT required for stability." Added Note "*CSS is optional. See Note 12 on Page 5." and “** CPB is optional. See “Functional Description” on page 12 for more information.” Added "The 1.5V, 3.3V and 5V fixed output voltages will be released in the future." to Note 3 on page 2. In “Thermal Information” on page 4, updated Theta JA from 45 to 48. In “Soft-Start Operation (Optional)” on page 12: -Changed "The external capacitor always gets discharged to 0V at start-up of after coming out of a chip disable. "The external capacitor always gets discharged to ground pin potential at start-up or enabling." -Changed "The soft-start function effectively limits the amount of in-rush current below the programmed current limit during start-up or an enable sequence to avoid an overcurrent fault condition." to "The soft-start feature effectively reduces the in-rush current at power-up or LDO enable until VOUT reaches regulation." -Added "See Figures 25 through 27 in the “Typical Operating Performance Curves” beginning on page 6." -Added “RPD is the on resistance of the pull-down MOSFET, M8. RPD is 300Ω typically.”

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. (Continued)

DATE	REVISION	CHANGE
March 4, 2010	FN6660.1 (CONTINUED)	Added "Phase Boost Capacitor (Optional)" on page 13. In "Typical Operating Performance" on page 11, revised figure "PSRR vs VIN" which had 3 curves with "SPECTRAL NOISE DENSITY vs FREQUENCY" which has one curve. Added "Figure 33. "LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, NO CPB (ADJ VERSION)" and "Figure 34. "LOAD TRANSIENT 0A TO 3A, C_{OUT} = 10µF CERAMIC, CPB = 1500pF (ADJ VERSION)"
September 30, 2009	FN6660.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

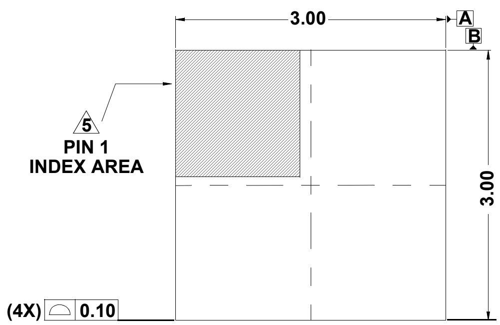
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

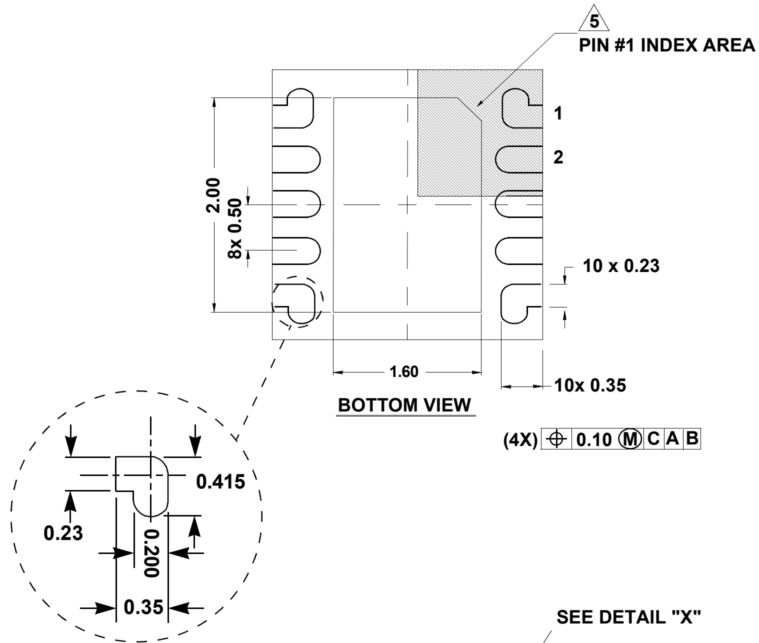
L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

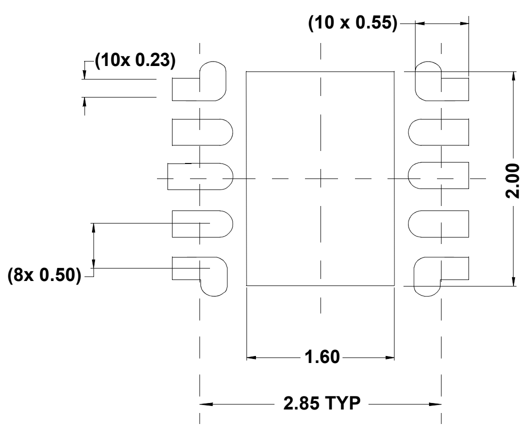
Rev 7, 10/11



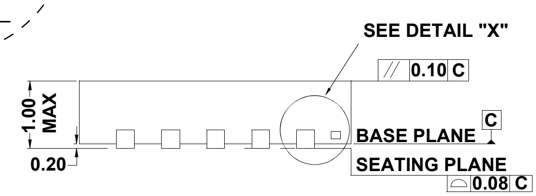
TOP VIEW



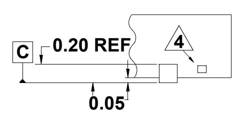
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.