SY89874U

2.5GHz, Any Differential, In-to-LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination

General Description

This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622MHz or higher) CML, LVPECL, LVDS or HSTL clock input signal and dividing down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. Available divider ratios are 2, 4, 8 and 16, or straight pass-through. In a typical 622MHz clock system this would provide availability of 311MHz, 155MHz, 77MHz, or 38MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /N).

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Precision Edge®

Features

- Integrated programmable clock divider and 1:2 fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - >2.5GHz f_{MAX}
  - <250ps t_r/t_f
  - <15ps within-device skew
- Low-jitter design:
  - <10ps$_{PP}$ total jitter
  - <1ps$_{RMS}$ cycle-to-cycle jitter
- Unique input termination and VT pin for DC-coupled and AC-coupled Inputs; CML, PECL, LVDS, and HSTL
- TTL/CMOS inputs for select and reset
- 100k EP-compatible LVPECL outputs
- Parallel programming capability
- Programmable divider ratios of 1, 2, 4, 8 and 16
- Low-voltage operation 2.5V or 3.3V
- Output disable function
- –40°C to 85°C temperature range
- Available in 16-pin (3mm x 3mm) QFN package

Applications

- SONET/SDH line cards
- Transponders
- High-end multiprocessor sensors

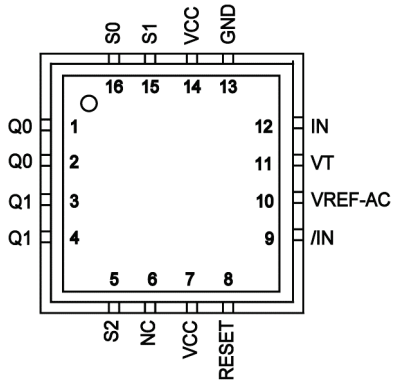
Ordering Information

Part Number[1]	Package Type	Operating Range	Package Marking	Lead Finish
SY89874UMG	QFN-16	Industrial	874U with Pb-free bar-line indicator	NiPdAu
SY89874UMGTR[2]	QFN-16	Industrial	874U with Pb-free bar-line indicator	NiPdAu

Note:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

Pin Configuration

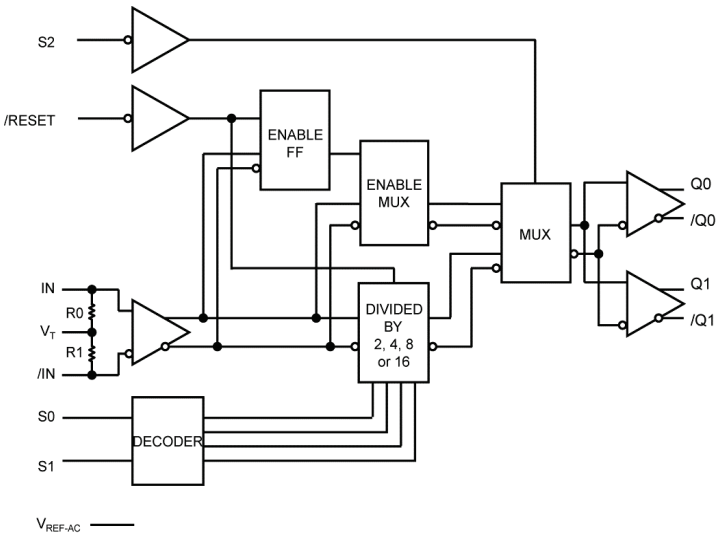


16-Pin QFN

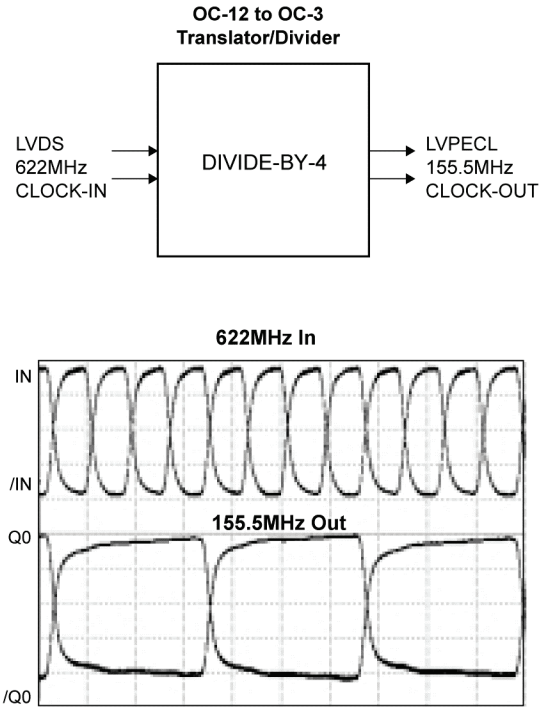
Pin Description

Pin Number	Pin Name	Pin Function
12, 9	IN, /IN	Differential input. Internal 50Ω termination resistors to VT input. Flexible input accepts any differential input. See the Input Interface Applications section.
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	Differential buffered LVPECL Outputs. Divided by 1, 2, 4, 8, or 16. See Truth Table. Unused PECL outputs may be left floating with no impact on jitter performance.
16, 15, 5	S0, S1, S2	Select pins. See Truth Table. LVTTL/CMOS logic levels. Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). Input threshold is V_{CC}/2.
6	NC	No connect.
8	/RESET /DISABLE	LVTTL/CMOS logic levels. Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected. Apply LOW to reset the divider (divided by 2, 4, 8, or 16 mode). Also acts as a synchronous disable/enable function. The reset and disable function occurs on the next HIGH-to-LOW clock input transition. Input threshold is V_{CC}/2.
10	VREF-AC	Reference voltage. Equal to V_{CC}-1.4V (approximately). Used for AC-coupled applications only. Decouple the VREF-AC pin with a 0.01µF capacitor. See the Input Interface Applications section.
11	VT	Termination center tap. For CML or LVDS inputs, leave this floating. Otherwise, see Figures 2a to 2f within the Input Interface Applications section.
7, 14	VCC	Positive power supply. Bypass with .01µF /0.01µF low-ESR capacitor.
13	GND	Ground.

Functional Block Diagram



Typical Performance



Truth Table

/RESET	S2	S1	S0	Outputs
1	0	X	X	Reference clock (pass through)
1	1	0	0	Reference clock ÷ 2
1	1	0	1	Reference clock ÷ 4
1	1	1	0	Reference clock ÷ 8
1	1	1	1	Reference clock ÷ 16
0	1	X	X	Q = Low, /Q = High clock disable

Absolute Maximum Ratings[3]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}+0.3V
ECL Output Current
  Continuous 50mA
  Surge 100mA
Input Current IN, /IN (I_{IN}) ..... ±50mA
V_T Current (I_{VT}) ..... ±100mA
V_{REF-AC} Sink/Source Current ($I_{VREF-AC}$)[5] ..... ±2mA
Lead Temperature (soldering, 20s) ..... 260°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[4]

Supply Voltage (V_{CC}) ..... +3.3V ±10% or +2.5V ±5%
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
  QFN (θ_{JA})
  Still-Air ..... 60°C/W
  500lfpm ..... 54°C/W
  QFN (Ψ_{JB})[6]
  Junction-to-Board ..... 32°C/W

DC Electrical Characteristics[7]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply		2.375		3.63	V
I_{CC}	Power supply current	No load, maximum V_{CC}		50	75	mA
R_{IN}	Differential input resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input high voltage (IN, /IN)	Note 8	0.1		V_{CC} + 0.3	V
V_{IL}	Input low voltage (IN, /IN)	Note 8	–0.3		V_{IH} – 0.1	V
V_{IN}	Input voltage swing	Notes 8, 9	0.1		V_{CC}	V
V_{DIFF_IN}	Differential input voltage swing	Notes 8, 9, 10	0.2			V
I_{IN}	Input current (IN, /IN)	Note 8			45	mA
V_{REF-AC}	Reference voltage	Note 11	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V

Notes:

3. Exceeding the absolute maximum ratings may damage the device.
4. The device is not guaranteed to function outside its operating ratings.
5. Due to the limited drive capability, use for input of the same package only.
6. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
7. Specification for packaged product only. The circuit is designed to meet the DC specifications shown in the DC Electrical Characteristics table after thermal equilibrium has been established.
8. Due to the internal termination (see Input Buffer Structure), the input current depends on the applied voltages at IN, /IN, and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit. Performance might be impacted if the differential inputs are driven single-ended.
9. See Timing Diagram for V_T definition. V_{IN} (maximum) is specified when V_T is floating.
10. See Typical Operating Characteristics section for V_{DIFF} definition.
11. Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to the VT pin.

LVPECL (100KEP) DC Electrical Characteristics[12, 13]

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = -40°C to +85°C, R_L = 50Ω to V_{CC} - 2V, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH voltage		V_{CC} – 1.145	V_{CC} – 1.020	V_{CC} – 0.895	V
V_{OL}	Output LOW voltage		V_{CC} – 1.945	V_{CC} – 1.820	V_{CC} – 1.695	V
V_{OUT}	Output voltage swing		550	800	1050	mV
V_{DIFF_OUT}	Differential output voltage swing		1.10	1.60	2.10	V

LVTTL/CMOS DC Electrical Characteristics[13, 14]

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH voltage		2.0			V
V_{IL}	Input LOW voltage				0.8	V
I_{IH}	Input HIGH current		-125		20	µA
I_{IL}	Input LOW current				-300	µA

AC Electrical Characteristics[13, 15]

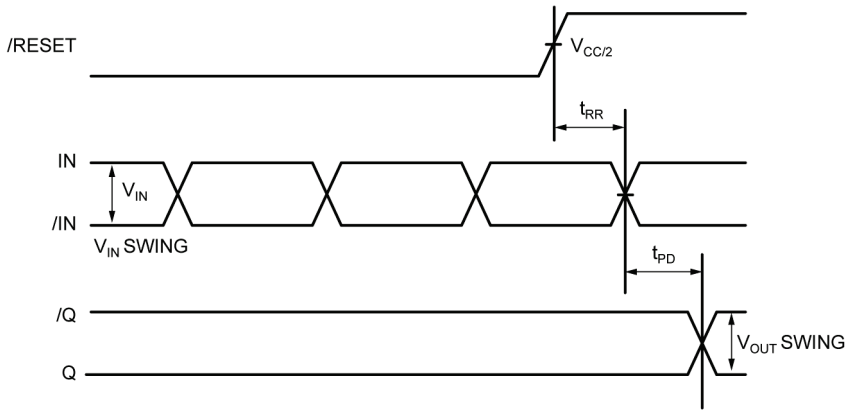
V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = -40°C to +85°C, R_L = 50Ω to V_{CC} - 2V, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maxiumum output toggle frequency	Output swing ≥400mV	2.5			GHz
	Maximum input frequency	Divide by 2, 4, 8, 16	3.2			GHz
t_{PD}	Differential propagation delay	Input swing <400mV	540	650	790	ps
	IN to Q	Input swing ≥400mV	480	600	730	ps
t_{SKEW}	Within-device skew (differential)	Note 16		7	15	ps
	Q0 – Q1					
	Part-to-part skew (differential)	Note 16			250	ps
t_{RR}	Reset recovery time	Note 17	600			ps
t_{JITTER}	Cycle-to-cycle jitter	Note 18			1	ps_{RMS}
	Total jitter	Note 19			10	ps_{PP}
t_r/t_f	Rise/fall time (20% to 80%)		70	150	250	ps

Notes:

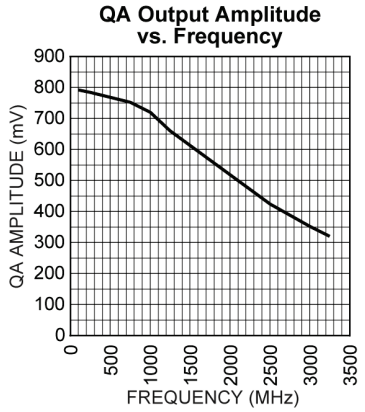
12. The circuit is designed to meet the DC specifications shown in the LVPECL (100KEP) Electrical Characteristics table after thermal equilibrium has been established.
13. Specification for packaged product only.
14. The circuit is designed to meet the DC specifications shown in the LVTTL/CMOS Electrical Characteristics table after thermal equilibrium has been established.
15. Measured with 400mV signal, 50% duty cycle, all outputs loaded with 50Ω to V_{CC} – 2V, unless otherwise stated.
16. Skew is measured between outputs under identical transitions.
17. See the Timing Diagram section.
18. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
19. Total jitter definition: With an ideal clock input, of frequency ≤f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

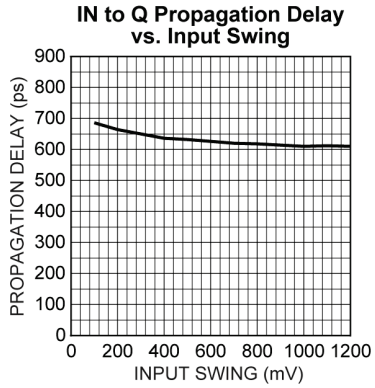
Timing Diagram

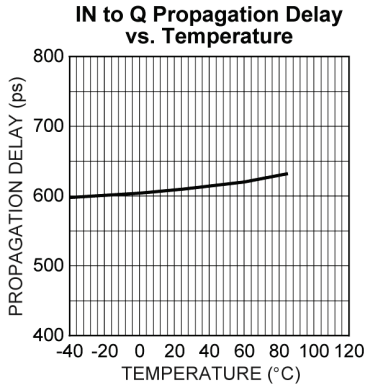


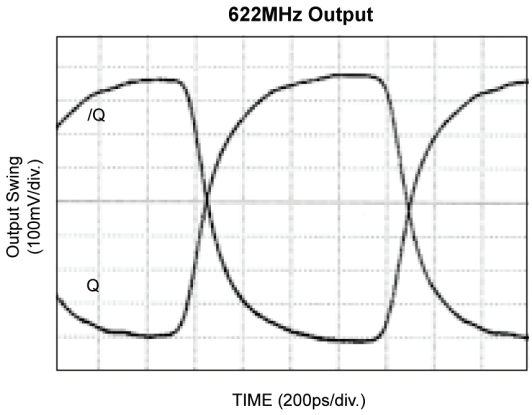
Typical Characteristics

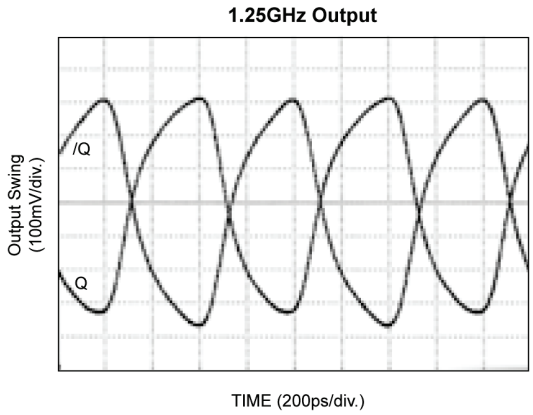
V_{CC} = 3.3V, V_{IN} = 400mV, T_A = +25°C, unless otherwise stated.

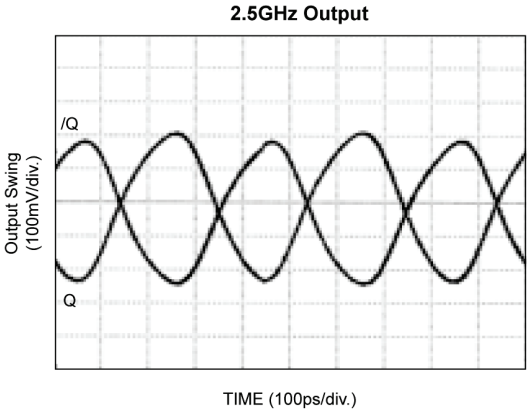






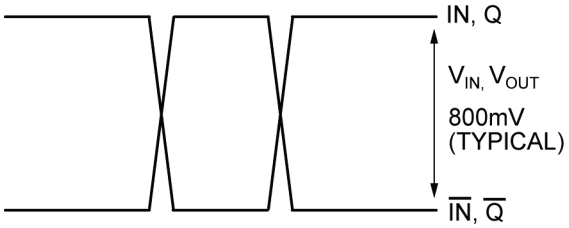




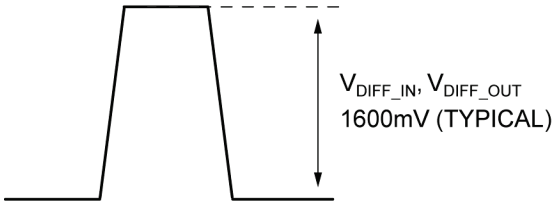


Definition of Single-Ended and Differential Swing

Single-ended swing is defined as the amplitude of the signal when driven differentially. Differential swing is defined as IN — /IN (or Q — /Q).

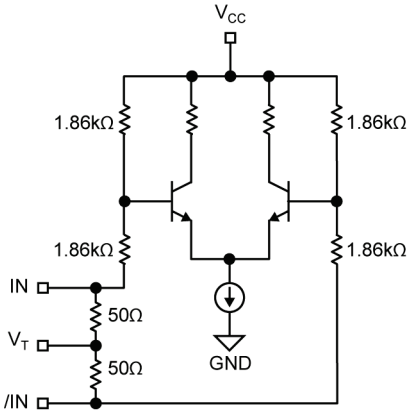


Single-ended swing

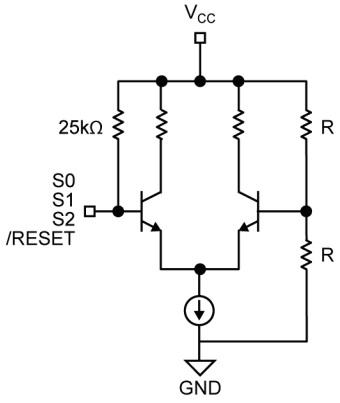


Differential swing

Input Buffer Structure

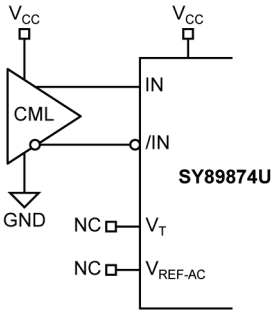


Single-ended swing

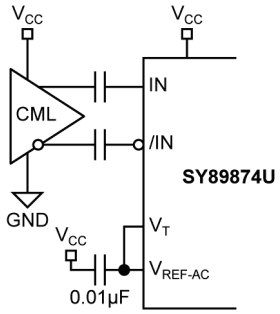


Differential swing

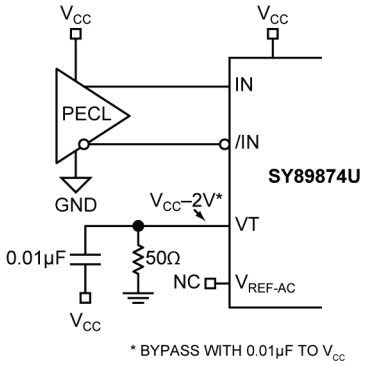
Input Interface Applications



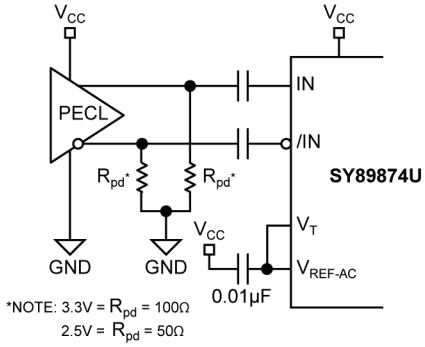
DC-coupled CML input interface



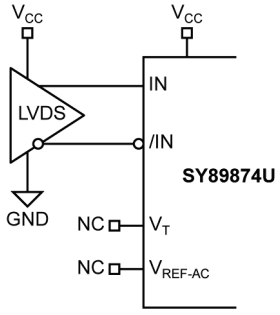
AC-coupled CML input interface



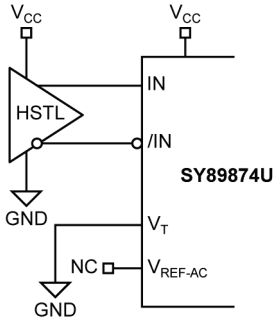
DC-coupled PECL input interface



AC-coupled PECL input interface



LVDS input interface

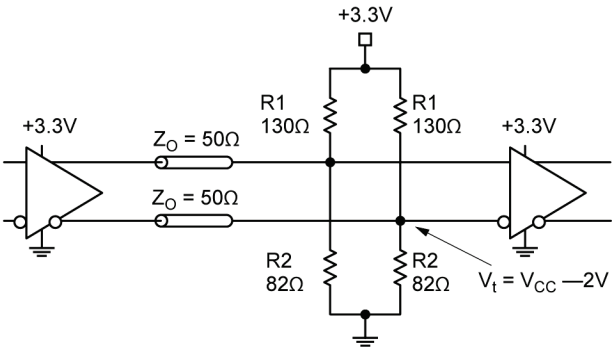


HSTL input interface

Related Product and Support Documentation

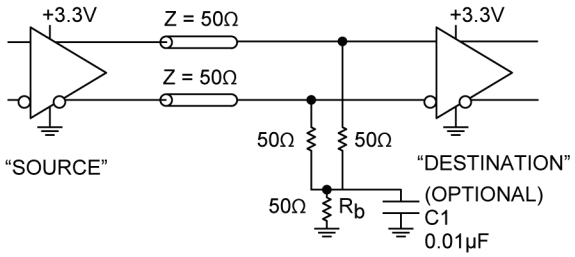
Part Number	Function	Website Link
SY89871U	2.5GHz Any Differential In-to-LVPECL Programmable Clock Divider/Fanout Buffer with Internal Termination	www.micrel.com/index.php/en/products/clock-timing/clock-data-distribution/clock-dividers/article/11-sy89871u.html
	QFN Application Note	www.amkor.com/products/notes_papers/mlf_appnote_0902.pdf
TCG Solutions	New Products and Applications	www.micrel.com/index.php/en/products/clock-timing.html

LVPECL Output Termination Recommendations



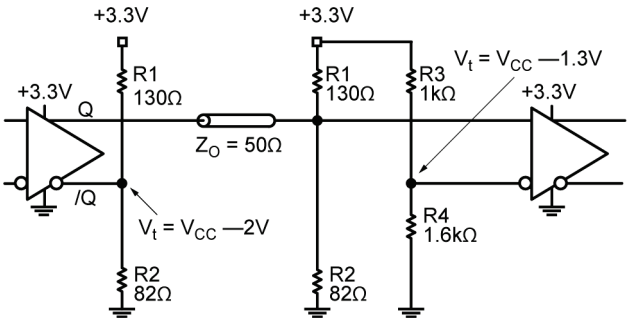
Parallel Termination Thevenin Equivalent

Note:
For +2.5V systems. R1 = 250Ω, R2 = 62.5Ω.



Three-Resistor "Y Termination"

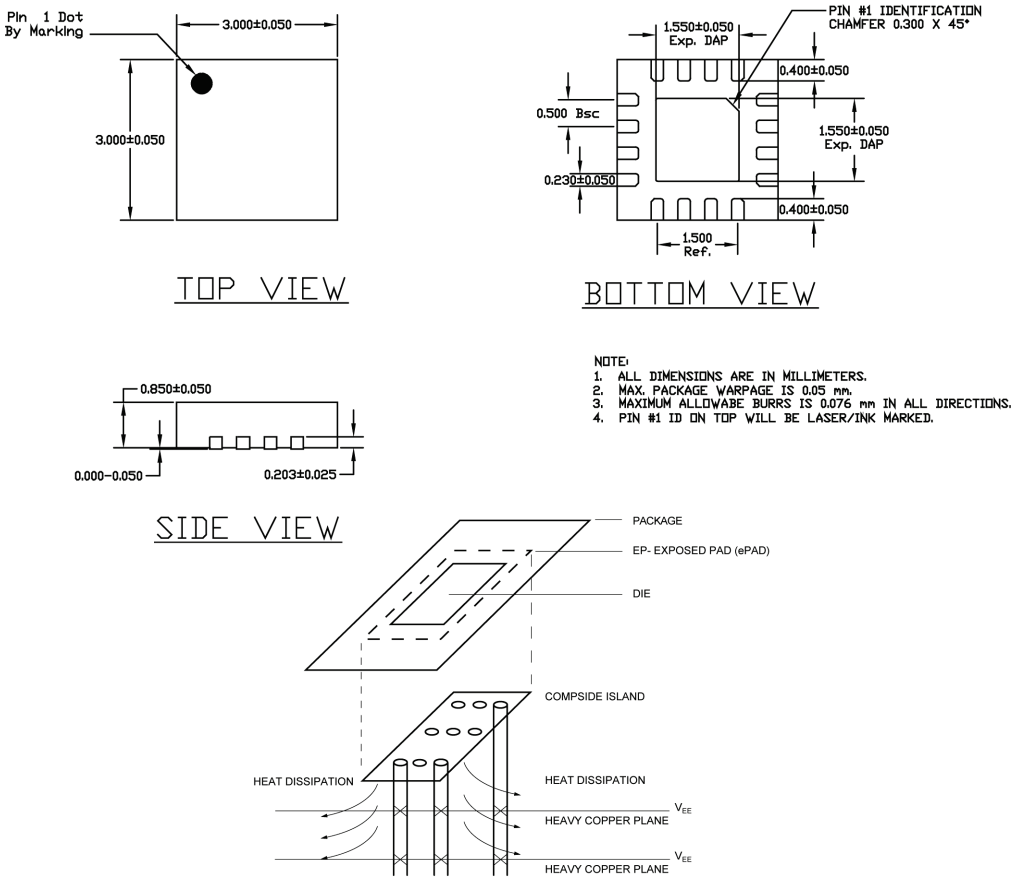
Notes:
Power-saving alternative to Thevenin termination.
Place termination resistors as close to destination inputs as possible.
R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +2.5V systems, R_b = 39Ω.
C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.



Terminating Unused I/O

Notes:
Unused output (/Q) must be terminated to balance the output.
For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.

Package Information[20, 21, 22]



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Note:

20. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.
21. Package meets Level 2 moisture sensitivity classification and is shipped in dry-pack.
22. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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