TPS22969 5.5-V, 6-A, 4.4-mΩ On-Resistance Load Switch

1 Features

- Integrated Single Channel Load Switch
- VBIAS Voltage Range: 2.5V to 5.5V
- VIN Voltage Range: 0.8V to 5.5V
- Ultra Low R_{ON} Resistance
  - R_{ON} = 4.4-mΩ at V_{IN} = 1.05-V (V_{BIAS} = 5V)
- 6A Maximum Continuous Switch Current
- Low Quiescent Current (20µA (typ) for V_{BIAS} = 5V)
- Low Shutdown Current (1µA (typ) for V_{BIAS} = 5V)
- Low Control Input Threshold Enables Use of 1.2-V or Higher GPIO
- Controlled and Fixed Slew Rate Across V_{BIAS} and V_{IN}
  - t_R = 599µs at V_{IN} = 1.05V (V_{BIAS} = 5V)
- Quick Output Discharge (QOD)
- SON 8-Terminal Package with Thermal Pad
- ESD Performance Tested per JESD 22
  - 2kV Human-Body Model (HBM)
  - 1kV Charged-Device Model (CDM)

2 Applications

- Ultrabook™/Notebooks
- Desktop PC
- Industrial PC
- Chromebook
- Servers
- Set-top Boxes
- Telecom Systems
- Tablet PC

3 Description

The TPS22969 is a small, ultra-low R_{ON}, single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8-V to 5.5-V and can support a maximum continuous current of 6-A.

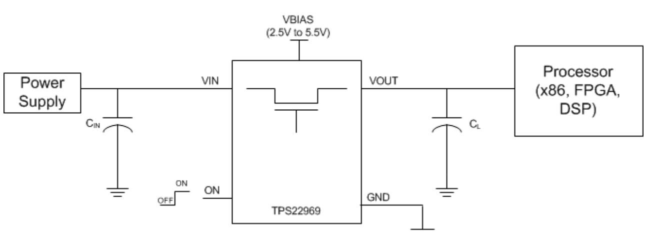
The combination of ultra-low R_{ON} and high current capability of the device makes it ideal for driving processor rails with very tight voltage dropout tolerances. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The switch can be independently controlled via the ON terminal, which is capable of interfacing directly with low-voltage control signals originating from microcontrollers or low voltage discrete logic. The device further reduces the total solution size by integrating a 224-Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off.

The TPS22969 is available in a small 3mm x 3mm SON-8 package (DNY). The DNY package integrates a thermal pad which allows for high power dissipation in high current and high temperature applications. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS22969DNY	WSON (8)	3mm × 3mm

4 Simplified Schematic



Typical Application: driving high current core rails for a processor

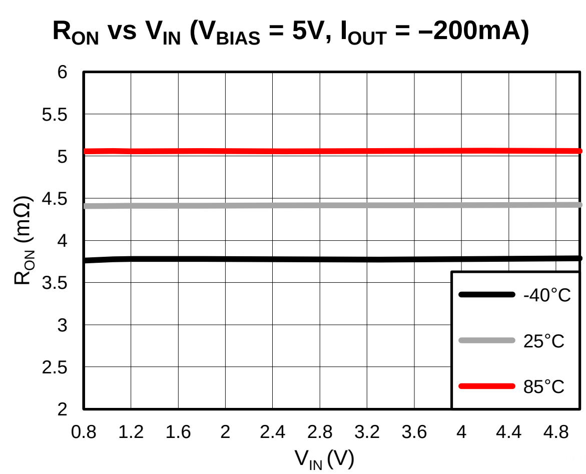


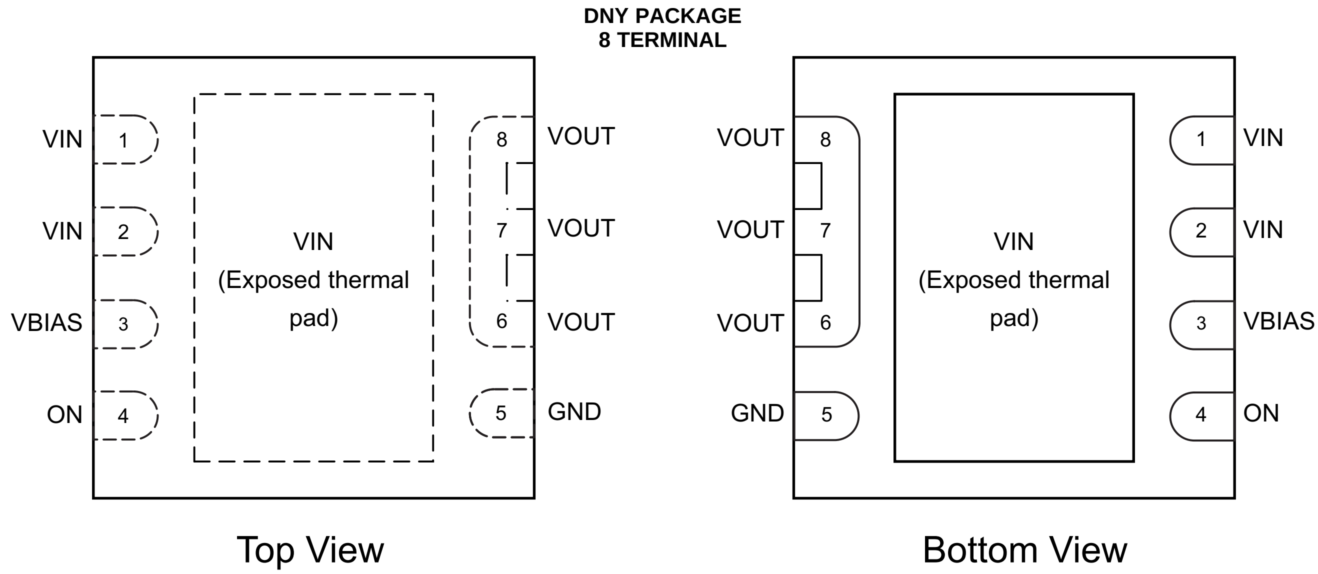
Table of Contents

5 Revision History

Changes from Original (February 2014) to Revision A — **Page**

- Initial release of full version. 1

6 Terminal Configuration and Functions



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	1, 2	I	Switch input. Place ceramic bypass capacitor(s) between this terminal and GND. See the Detailed Description section for more information.
VIN	Exposed thermal Pad	I	Switch input. Place ceramic bypass capacitor(s) between this terminal and GND. See the Detailed Description section for more information.
VBIAS	3	I	Bias voltage. Power supply to the device.
ON	4	I	Active high switch control input. Do not leave floating.
GND	5	–	Ground.
VOUT	6, 7, 8	O	Switch output. Place ceramic bypass capacitor(s) between this terminal and GND. See the Detailed Description section for more information.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	6	V
V_{BIAS}	Bias voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	6	V
V_{ON}	ON terminal voltage range	–0.3	6	V
I_{MAX}	Maximum Continuous Switch Current		6	A
I_{PLS}	Maximum Pulsed Switch Current, pulse < 300-µs, 2% duty cycle		8	A
T_A	Operating free-air temperature range	–40	85	°C
T_J	Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
V_{ESD} (1)	Human-Body Model (HBM) (2)		2	kV
	Charged-Device Model (CDM) (3)		1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
$V_{IH, ON}$	High-level voltage, ON	V_{BIAS} = 2.5V to 5.5V	1.2	5.5	V
$V_{IL, ON}$	Low-level voltage, ON	V_{BIAS} = 2.5V to 5.5V	0	0.5	V
C_{IN}	Input Capacitor		1 (1)		µF

(1) Refer to Detailed Description section.

7.4 Thermal Information

THERMAL METRIC (1)		TPS22969 DNY 8 TERMINALS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	44.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	17.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C (Full) and V_{BIAS} = 5.0V.** Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
CURRENTS AND THRESHOLDS								
$I_{Q,\ VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{BIAS}, V_{ON} = 5.0V		Full		20.4	26.0	µA
$I_{SD,\ VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0V, V_{OUT} = 0V		Full		1.1	1.5	µA
$I_{SD,\ VIN}$	V_{IN} shutdown current	V_{ON} = 0V, V_{OUT} = 0V	V_{IN} = 5.0V	Full			0.1	µA
			V_{IN} = 3.3V				0.1	
			V_{IN} = 1.8V				0.1	
			V_{IN} = 1.05V				0.1	
			V_{IN} = 0.8V				0.1	
I_{ON}	ON terminal leakage current	V_{ON} = 5.5V		Full			0.1	µA
$V_{HYS,\ ON}$	ON terminal hysteresis	V_{BIAS} = V_{IN}		25°C		113		mV
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance	I_{OUT} = –200mA, V_{BIAS} = 5.0V	V_{IN} = 5.0V	25°C		4.4	5.0	mΩ
				Full			5.6	
			V_{IN} = 3.3V	25°C		4.4	5.0	mΩ
				Full			5.6	
			V_{IN} = 2.5V	25°C		4.4	5.0	mΩ
				Full			5.6	
			V_{IN} = 1.8V	25°C		4.4	5.0	mΩ
				Full			5.6	
			V_{IN} = 1.05V	25°C		4.4	5.0	mΩ
				Full			5.6	
			V_{IN} = 0.8V	25°C		4.4	5.0	mΩ
				Full			5.6	
		I_{OUT} = –6A, V_{BIAS} = 5.0V	V_{IN} = 1.05V	Full		4.6	5.8 [1]	mΩ
R_{PD}	Output pulldown resistance	V_{IN} = 5.0V, V_{ON} = 0V, V_{OUT} = 1V		Full		224	233	Ω

(1) Parameter verified by design and characterization, but not tested in production.

7.6 Electrical Characteristics

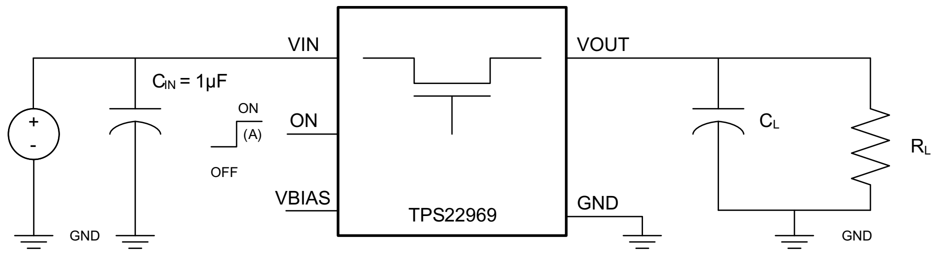
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C (Full) and V_{BIAS} = 2.5V**. Typical values are for T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
CURRENTS AND THRESHOLDS								
$I_{Q,\ VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{BIAS}, V_{ON} = 5.0V		Full		9.9	12.5	µA
$I_{SD,\ VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0V, V_{OUT} = 0V		Full		0.5	0.65	µA
$I_{SD,\ VIN}$	V_{IN} shutdown current	V_{ON} = 0V, V_{OUT} = 0V	V_{IN} = 2.5V	Full			0.1	µA
			V_{IN} = 1.8V				0.1	
			V_{IN} = 1.05V				0.1	
			V_{IN} = 0.8V				0.1	
I_{ON}	ON terminal input leakage current	V_{ON} = 5.5V		Full			0.1	µA
$V_{HYS,\ ON}$	ON terminal hysteresis	V_{BIAS} = V_{IN}		25°C		83		mV
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance	I_{OUT} = –200mA, V_{BIAS} = 2.5V	V_{IN} =2.5V	25°C		4.7	5.3	mΩ
				Full			6.0	
			V_{IN} =1.8V	25°C		4.6	5.2	mΩ
				Full			5.8	
			V_{IN} =1.05V	25°C		4.5	5.1	mΩ
				Full			5.7	
			V_{IN} = 0.8V	25°C		4.5	5.1	mΩ
				Full			5.7	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5V, V_{ON} = 0V, V_{OUT} = 1V		Full		224	233	Ω

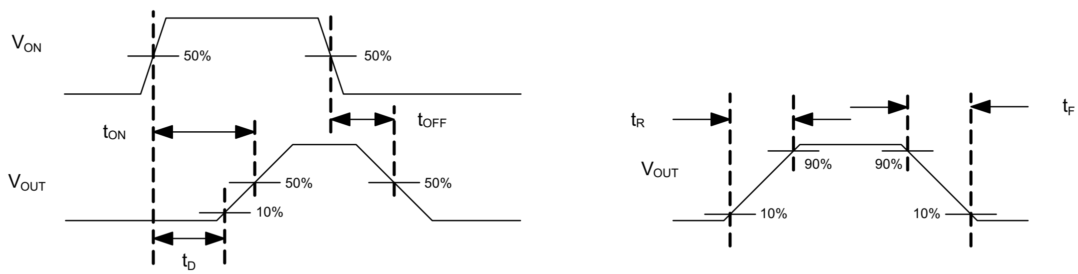
7.7 Switching Characteristics

Refer to the timing test circuit in Figure 1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON terminal is asserted high.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = 5V, V_{ON} = V_{BIAS} = 5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10Ω, C_L = 0.1µF		2397		µs
t_{OFF}	Turn-off time			4		
t_R	V_{OUT} rise time			2663		
t_F	V_{OUT} fall time			2		
t_D	Delay time			1009		
V_{IN} = 1.05V, V_{ON} = V_{BIAS} = 5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10Ω, C_L = 0.1µF		1064		µs
t_{OFF}	Turn-off time			4		
t_R	V_{OUT} rise time			599		
t_F	V_{OUT} fall time			2		
t_D	Delay time			727		
V_{IN} = 0.8V, V_{ON} = V_{BIAS} = 5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10Ω, C_L = 0.1µF		981		µs
t_{OFF}	Turn-off time			4		
t_R	V_{OUT} rise time			500		
t_F	V_{OUT} fall time			2		
t_D	Delay time			714		
V_{IN} = 2.5V, V_{ON} = 5V, V_{BIAS} = 2.5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10Ω, C_L = 0.1µF		1576		µs
t_{OFF}	Turn-off time			8		
t_R	V_{OUT} rise time			1372		
t_F	V_{OUT} fall time			2		
t_D	Delay time			865		
V_{IN} = 1.05V, V_{ON} = 5V, V_{BIAS} = 2.5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10Ω, C_L = 0.1µF		1080		µs
t_{OFF}	Turn-off time			8		
t_R	V_{OUT} rise time			604		
t_F	V_{OUT} fall time			2		
t_D	Delay time			738		
V_{IN} = 0.8V, V_{ON} = 5V, V_{BIAS} = 2.5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10Ω, C_L = 0.1µF		994		µs
t_{OFF}	Turn-off time			8		
t_R	V_{OUT} rise time			502		
t_F	V_{OUT} fall time			2		
t_D	Delay time			723		



Timing Test Circuit

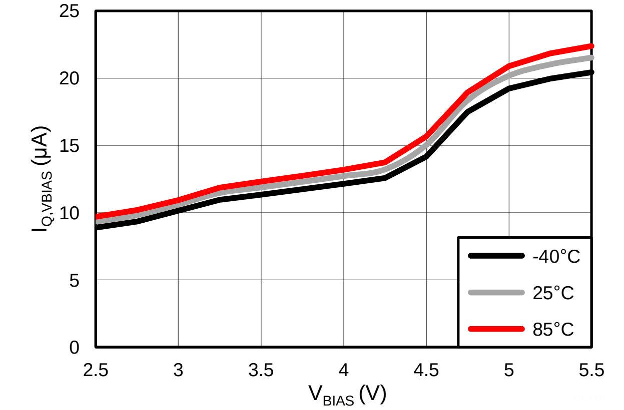


Timing Waveforms

(A) Rise and fall times of the control signal is 100ns.

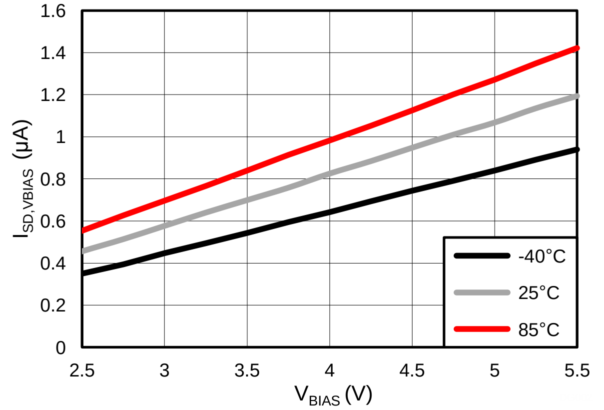
Figure 1. Switching Characteristics Measurement Setup and Definitions

7.8 Typical Characteristics



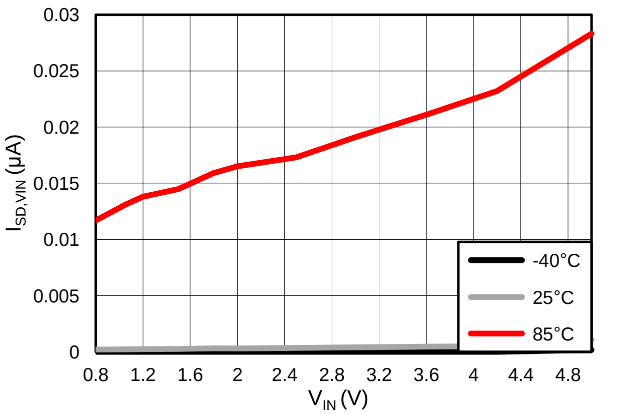
$V_{IN} = V_{BIAS}$ $V_{ON} = 5V$ $I_{OUT} = 0A$

Figure 2. $I_{Q,VBIAS}$ vs V_{BIAS}



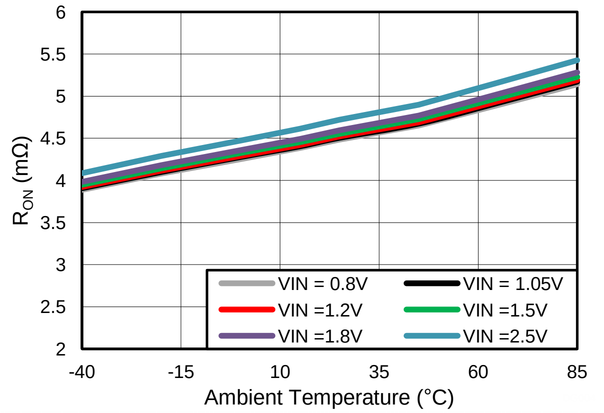
$V_{IN} = V_{BIAS}$ $V_{ON} = 0V$ $V_{OUT} = 0V$

Figure 3. $I_{SD,VBIAS}$ vs V_{BIAS}



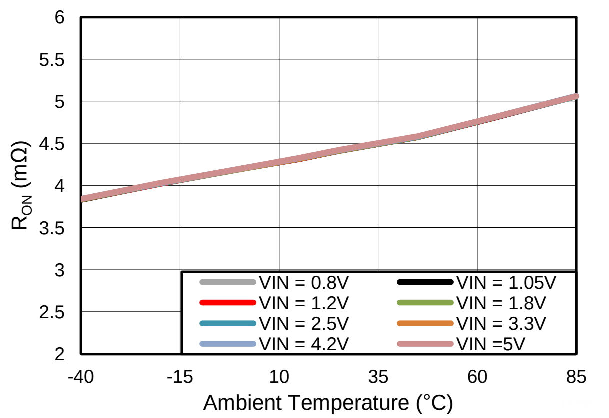
$V_{BIAS} = 5V$ $V_{ON} = 0V$ $V_{OUT} = 0V$

Figure 4. $I_{SD,VIN}$ vs V_{IN}



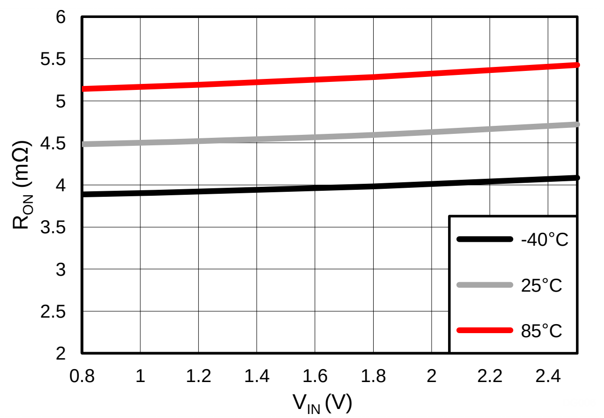
$V_{BIAS} = 2.5V$ $V_{ON} = 5V$ $I_{OUT} = –200mA$

Figure 5. R_{ON} vs Ambient Temperature



$V_{BIAS} = 5V$ $V_{ON} = 5V$ $I_{OUT} = –200mA$

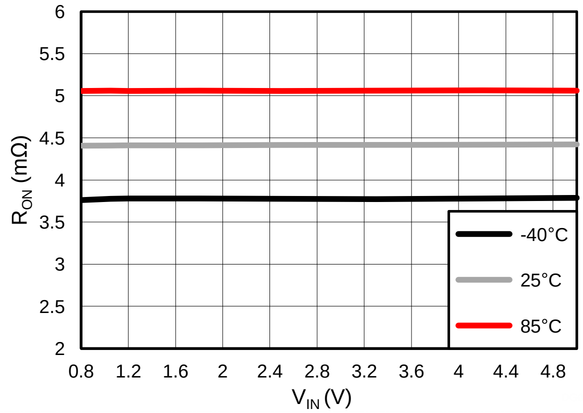
Figure 6. R_{ON} vs Ambient Temperature



$V_{BIAS} = 2.5V$ $V_{ON} = 5V$ $I_{OUT} = –200mA$

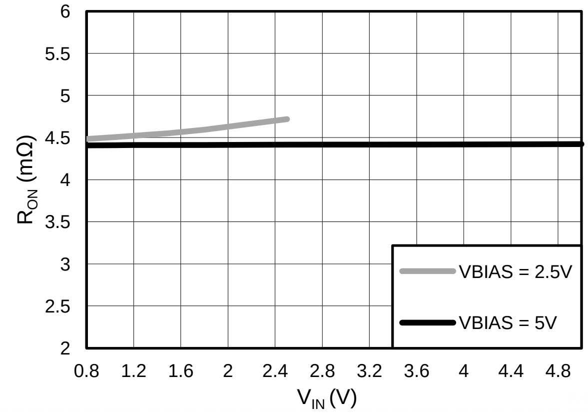
Figure 7. R_{ON} vs V_{IN}

Typical Characteristics (continued)



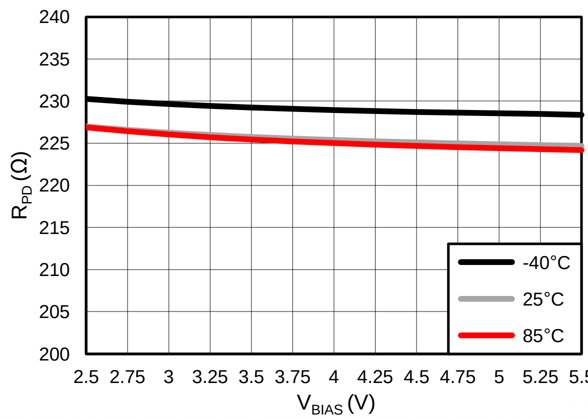
V_{BIAS} = 5V V_{ON} = 5V I_{OUT} = –200mA

Figure 8. R_{ON} vs V_{IN}



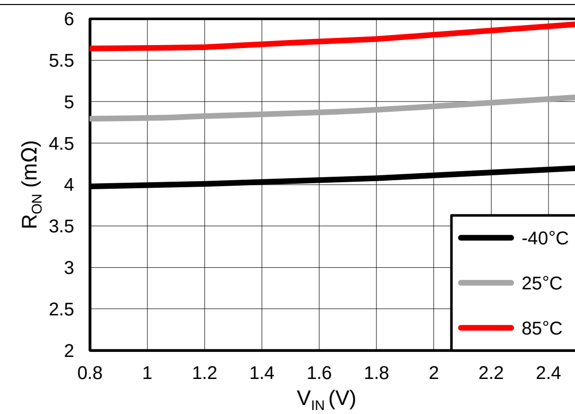
T_A = 25°C V_{ON} = 5V I_{OUT} = –200mA

Figure 9. R_{ON} vs V_{IN}



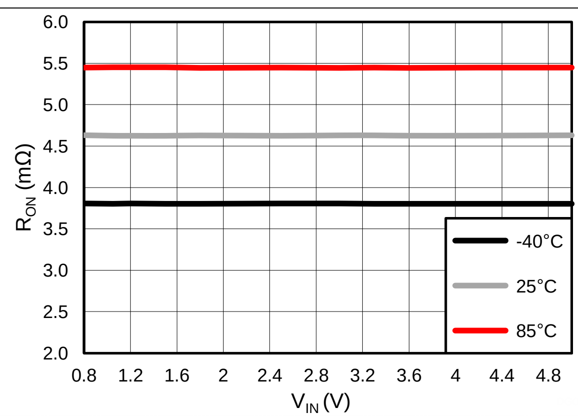
V_{ON} = 0V V_{IN} = 1.05V V_{OUT} = 1V

Figure 10. R_{PD} vs V_{BIAS}



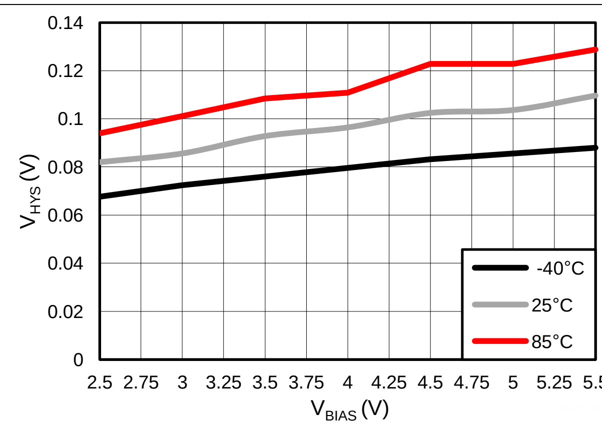
V_{BIAS} = 2.5V V_{ON} = 5V I_{OUT} = -6A

Figure 11. R_{ON} vs V_{IN} at 6A load



V_{BIAS} = 5V V_{ON} = 5V I_{OUT} = -6A

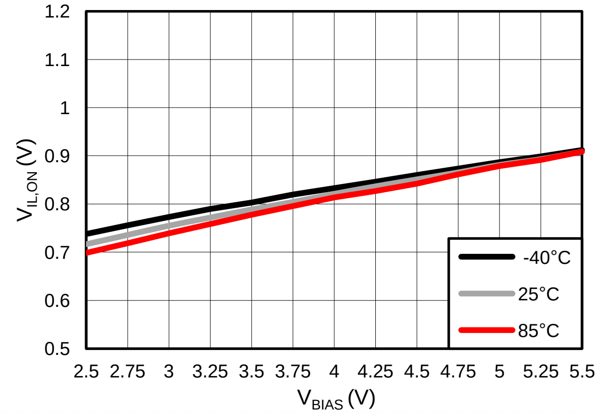
Figure 12. R_{ON} vs V_{IN} at 6A load



V_{IN} = V_{BIAS}

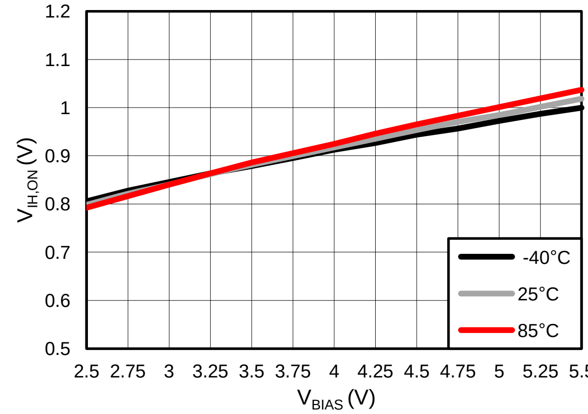
Figure 13. V_{HYS} vs V_{BIAS}

Typical Characteristics (continued)



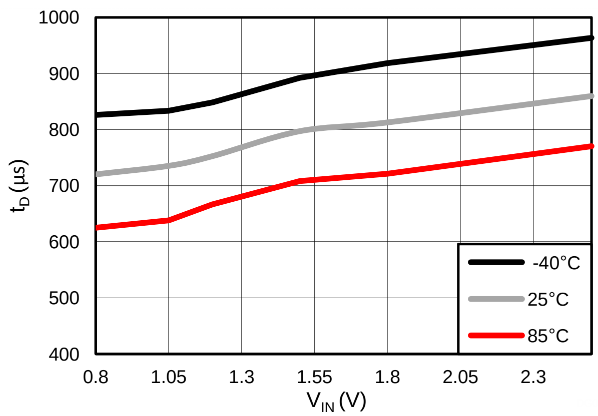
$V_{IN} = V_{BIAS}$ $I_{OUT} = 0A$

Figure 14. $V_{IL,ON}$ vs V_{BIAS}



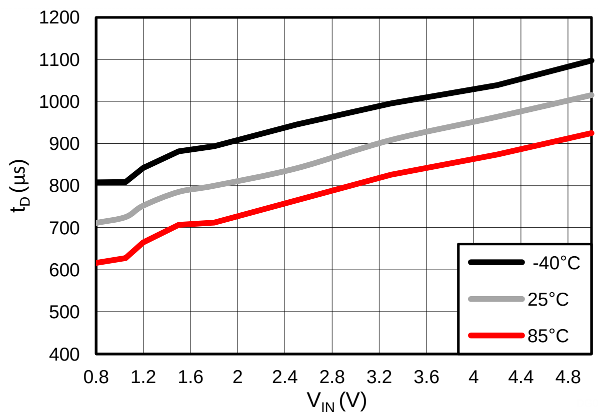
$V_{IN} = V_{BIAS}$ $I_{OUT} = 0A$

Figure 15. $V_{IH,ON}$ vs V_{BIAS}



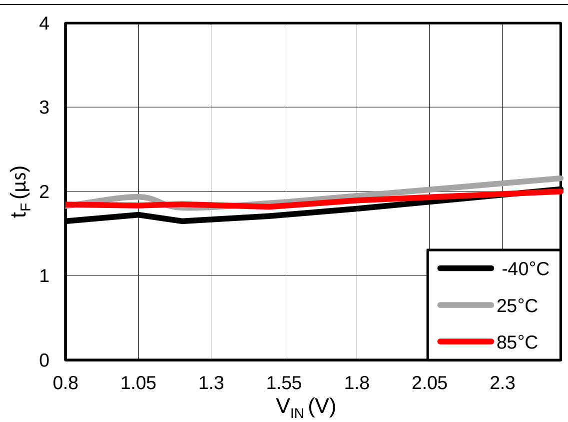
$V_{BIAS} = 2.5V$ $R_L = 10\Omega$ $C_L = 0.1\mu F$

Figure 16. t_D vs V_{IN}



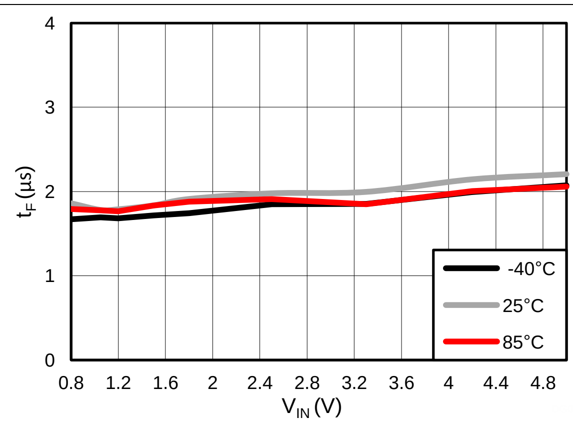
$V_{BIAS} = 5V$ $R_L = 10\Omega$ $C_L = 0.1\mu F$

Figure 17. t_D vs V_{IN}



$V_{BIAS} = 2.5V$ $R_L = 10\Omega$ $C_L = 0.1\mu F$

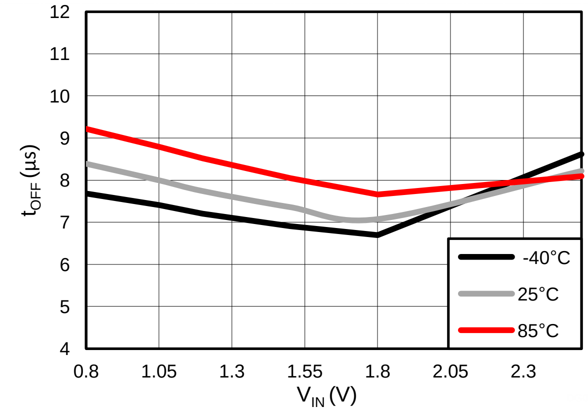
Figure 18. t_F vs V_{IN}



$V_{BIAS} = 5V$ $R_L = 10\Omega$ $C_L = 0.1\mu F$

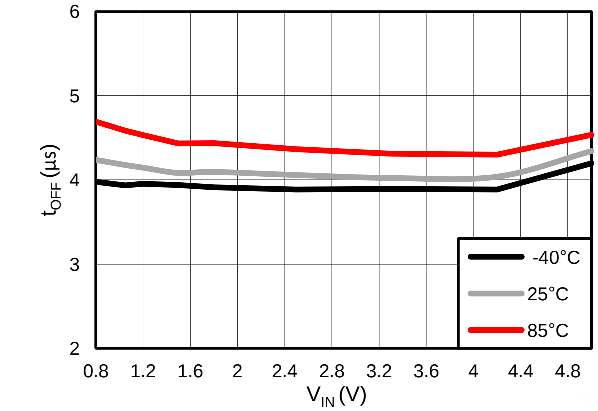
Figure 19. t_F vs V_{IN}

Typical Characteristics (continued)



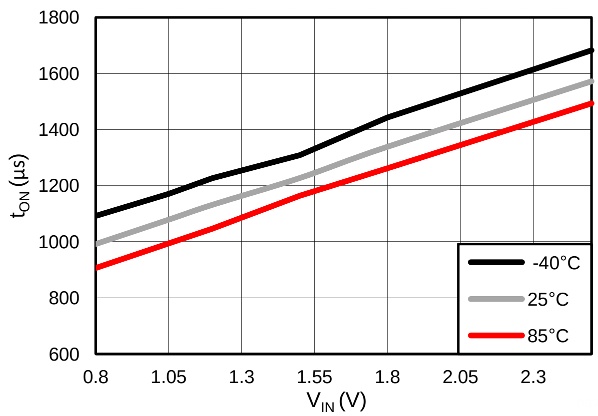
V_{BIAS} = 2.5V R_L = 10Ω C_L = 0.1µF

Figure 20. t_{OFF} vs V_{IN}



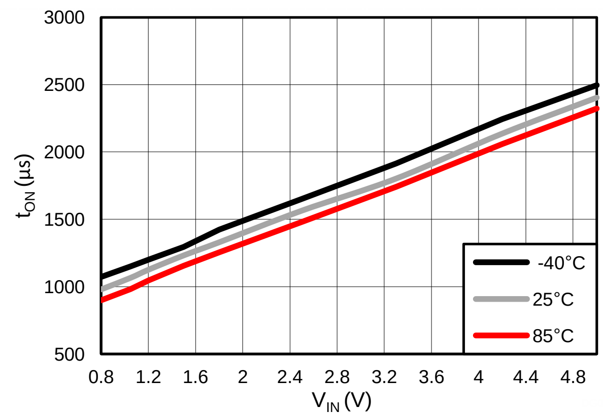
V_{BIAS} = 5V R_L = 10Ω C_L = 0.1µF

Figure 21. t_{OFF} vs V_{IN}



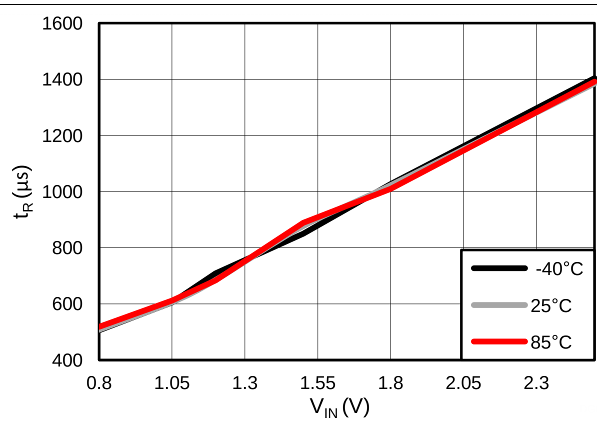
V_{BIAS} = 2.5V R_L = 10Ω C_L = 0.1µF

Figure 22. t_{ON} vs V_{IN}



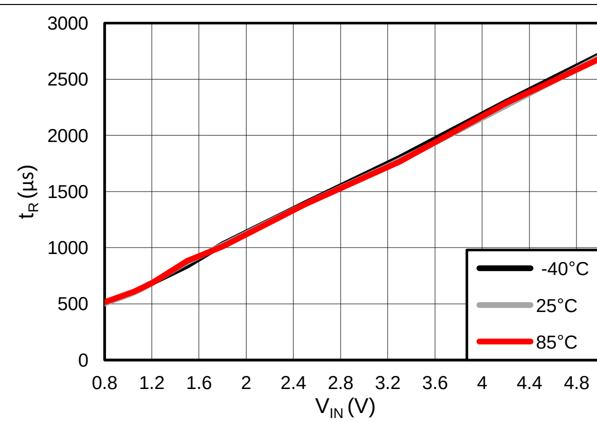
V_{BIAS} = 5V R_L = 10Ω C_L = 0.1µF

Figure 23. t_{ON} vs V_{IN}



V_{BIAS} = 2.5V R_L = 10Ω C_L = 0.1µF

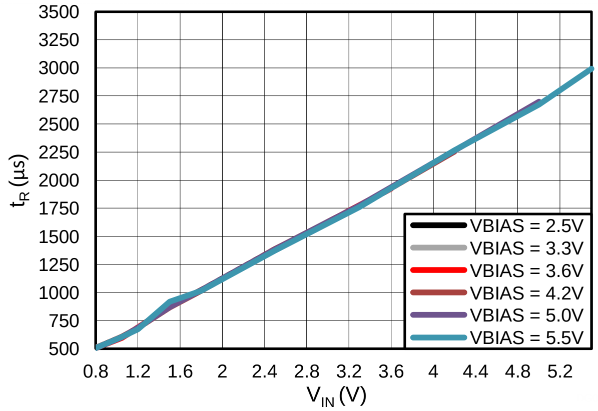
Figure 24. t_R vs V_{IN}



V_{BIAS} = 5V R_L = 10Ω C_L = 0.1µF

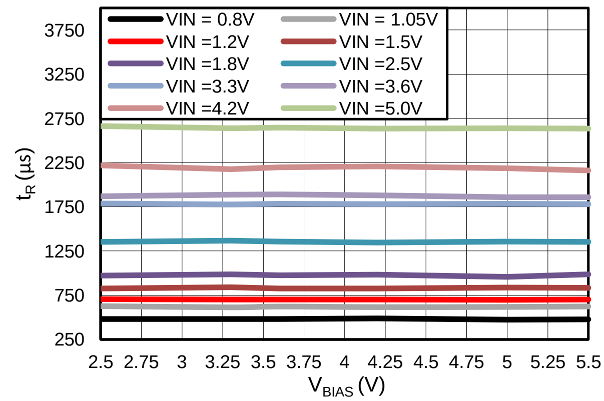
Figure 25. t_R vs V_{IN}

Typical Characteristics (continued)



T_A = 25°C R_L = 10Ω C_L = 0.1µF

Figure 26. t_R vs V_{IN} for Various V_{BIAS}



T_A = 25°C R_L = 10Ω C_L = 0.1µF

Figure 27. t_R vs V_{BIAS} for Various V_{IN}

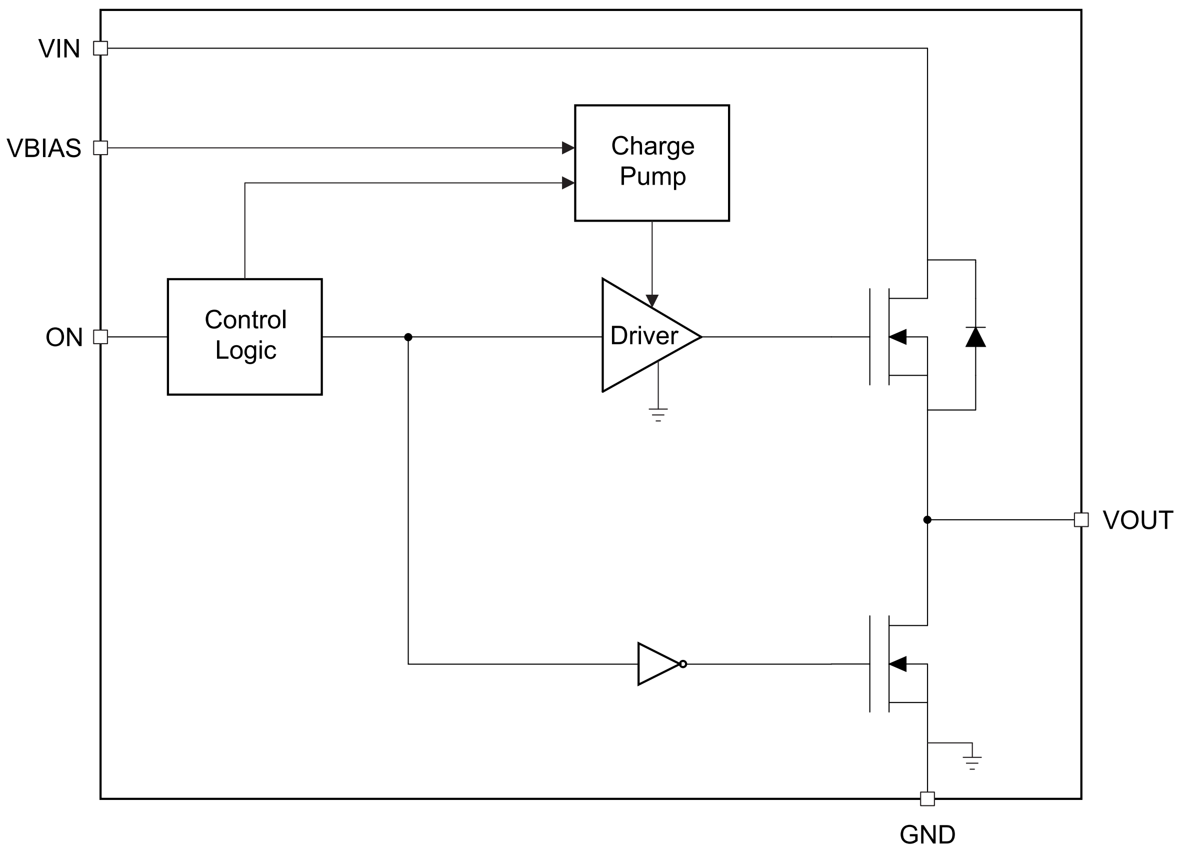
8 Detailed Description

8.1 Overview

The device is a 5.5V, 6A load switch in a 8-terminal SON package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unneccessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On/off Control

The ON terminal controls the state of the load switch, and asserting the terminal high (active high) enables the switch. The ON terminal is compatible with standard GPIO logic threshold and can be used with any microcontroller or discrete logic with 1.2-V or higher GPIO voltage. This terminal cannot be left floating and must be tied either high or low for proper functionality.

8.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the terminals, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor 10 times higher than the output capacitor to avoid excessive voltage drop; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device, but a ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

8.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the N-channel MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

8.3.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device may still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the Electrical Characteristics table. See Figure 28 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}. Performance of the device is not guaranteed for $V_{IN} > V_{BIAS}$.

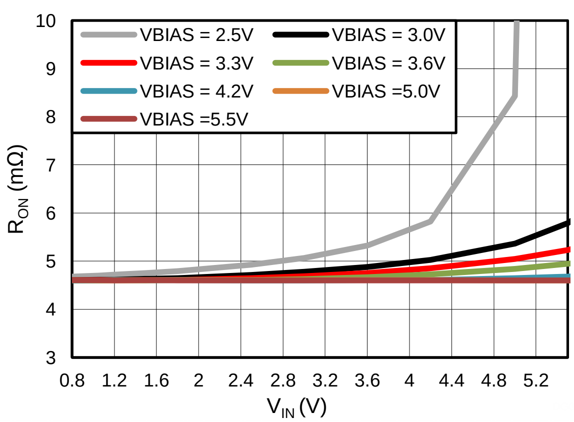


Figure 28. R_{ON} vs V_{IN} ($V_{IN} > V_{BIAS}$)

9 Applications and Implementation

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

9.2 Typical Application

This application demonstrates how the TPS22969 can be used to power downstream modules with large capacitances. The example below is powering a 100-µF capacitive output load.

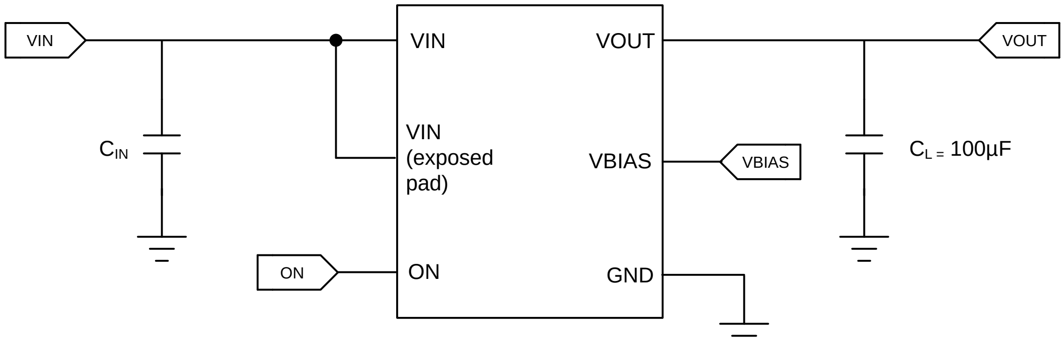


Figure 29. Typical Application Schematic for Powering a Downstream Module

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05V
V_{BIAS}	5.0V
Load current	6A

9.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- VIN voltage
- VBIAS voltage
- Load current

9.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (2)$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specficiations of the device are not violated.

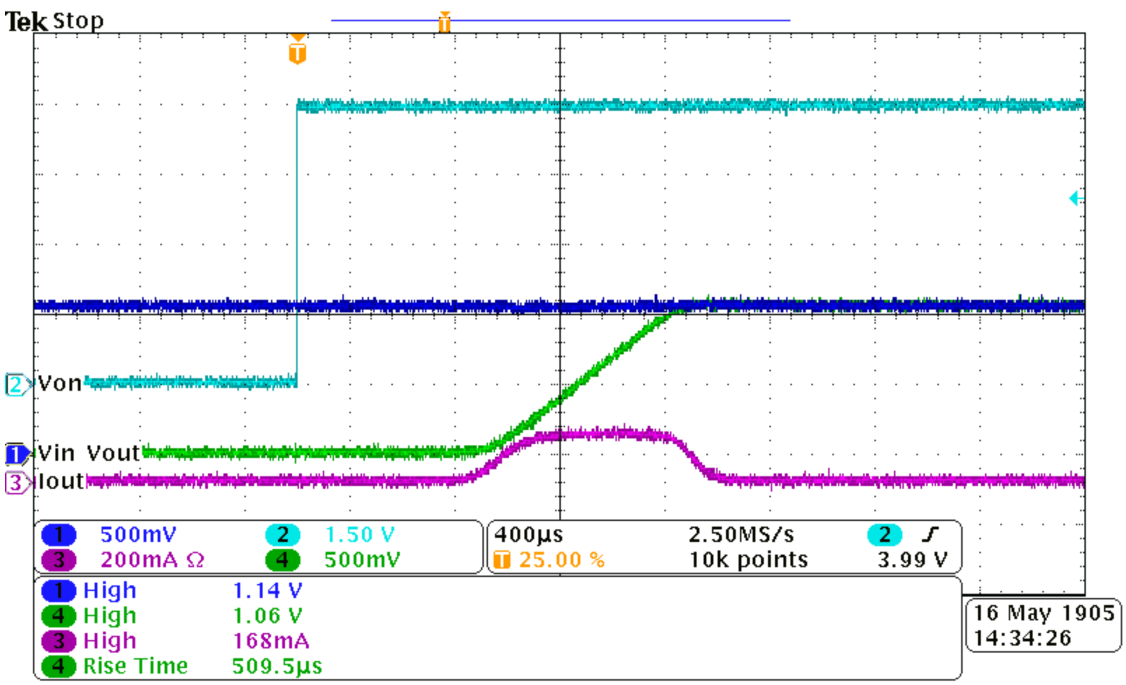


Figure 30. Inrush current (V_{BIAS} = 5V, V_{IN} = 1.05V, C_L = 100µF)

9.2.2.3 Thermal Considerations

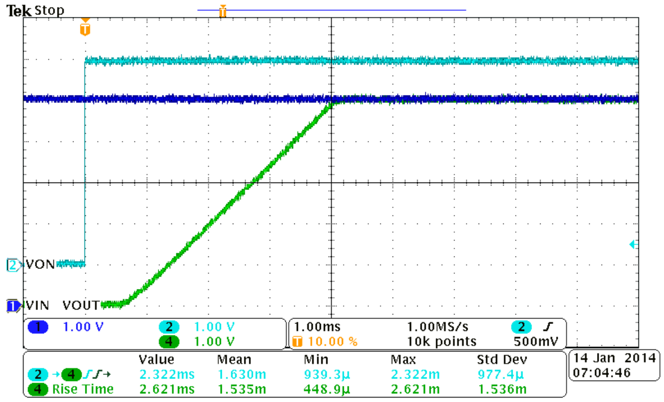
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 3.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (3)$$

where

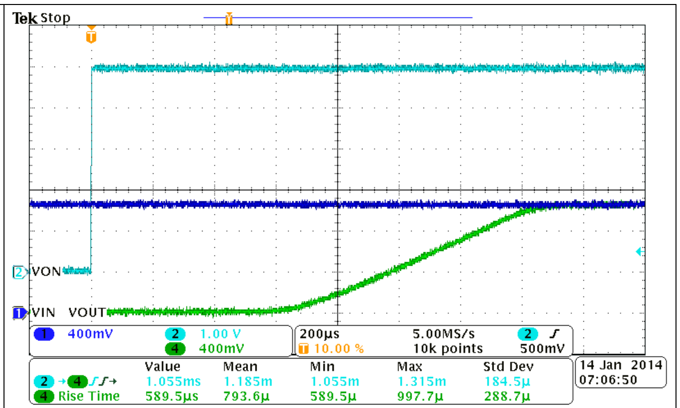
- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22969)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

9.2.3 Application Curves



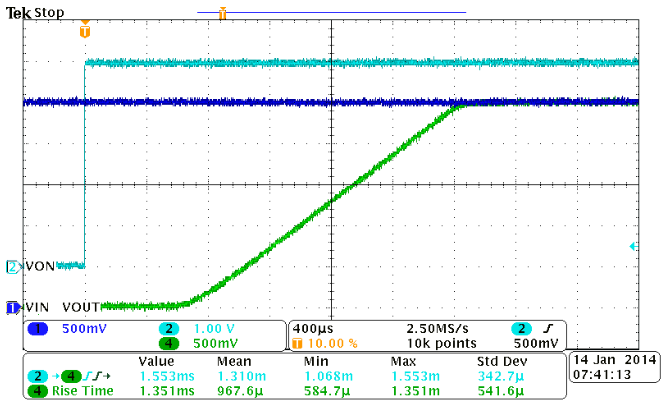
V_{BIAS} = 5V V_{IN} = 5V C_{IN} = 1µF C_L = 0.1µF

Figure 31. t_R at V_{BIAS} = 5V



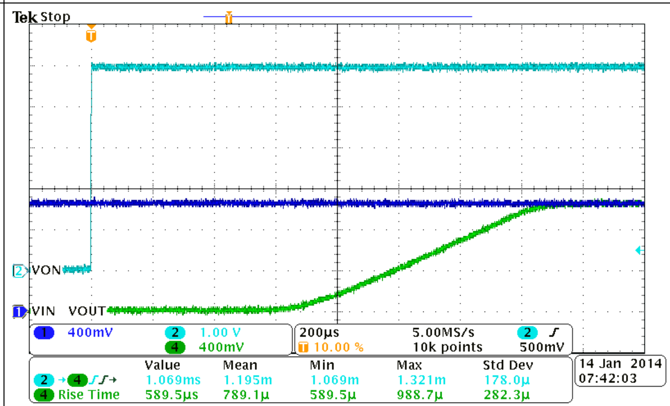
V_{BIAS} = 5V V_{IN} = 1.05V C_{IN} = 1µF C_L = 0.1µF

Figure 32. t_R at V_{BIAS} = 5V



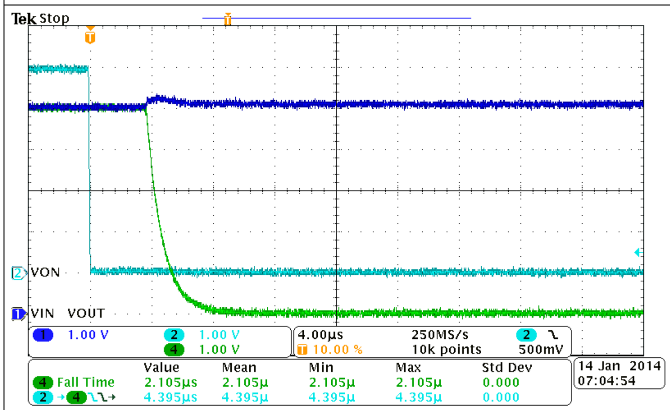
V_{BIAS} = 2.5V V_{IN} = 2.5V C_{IN} = 1µF C_L = 0.1µF

Figure 33. t_R at V_{BIAS} = 2.5V



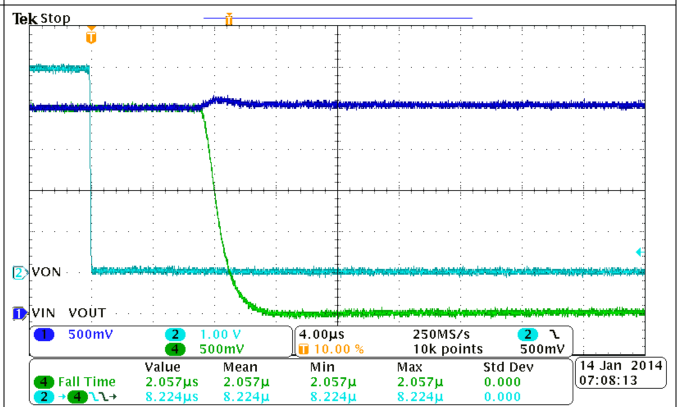
V_{BIAS} = 2.5V V_{IN} = 1.05V C_{IN} = 1µF C_L = 0.1µF

Figure 34. t_R at V_{BIAS} = 2.5V



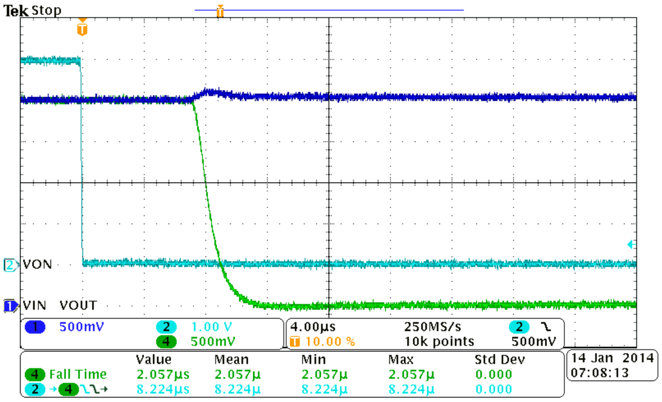
V_{BIAS} = 5V V_{IN} = 5V C_{IN} = 1µF C_L = 0.1µF

Figure 35. t_F at V_{BIAS} = 5V



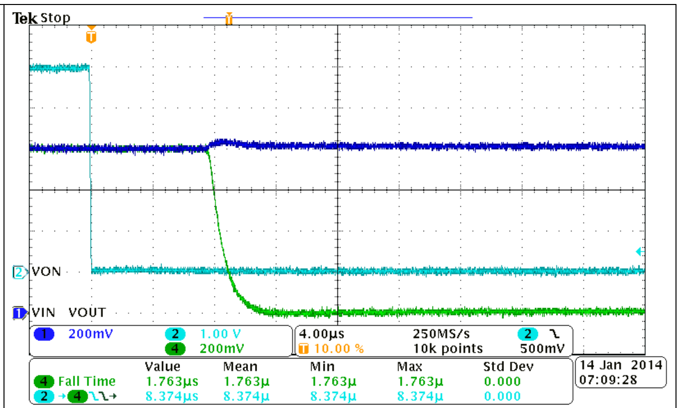
V_{BIAS} = 5V V_{IN} = 2.5V C_{IN} = 1µF C_L = 0.1µF

Figure 36. t_F at V_{BIAS} = 5V



V_{BIAS} = 2.5V V_{IN} = 2.5V C_{IN} = 1µF
C_L = 0.1µF

Figure 37. t_F at V_{BIAS} = 2.5V



V_{BIAS} = 2.5V V_{IN} = 0.8V C_{IN} = 1µF
C_L = 0.1µF

Figure 38. t_F at V_{BIAS} = 2.5V

10 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5-V to 5.5-V and V_{IN} range of 0.8-V to 5.5-V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10-µF may be sufficient.

11 Layout

11.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The VIN terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device terminals as possible.
- The VOUT terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device terminals as possible.
- The VBIAS terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-µF ceramic with X5R or X7R dielectric.

11.2 Layout Example

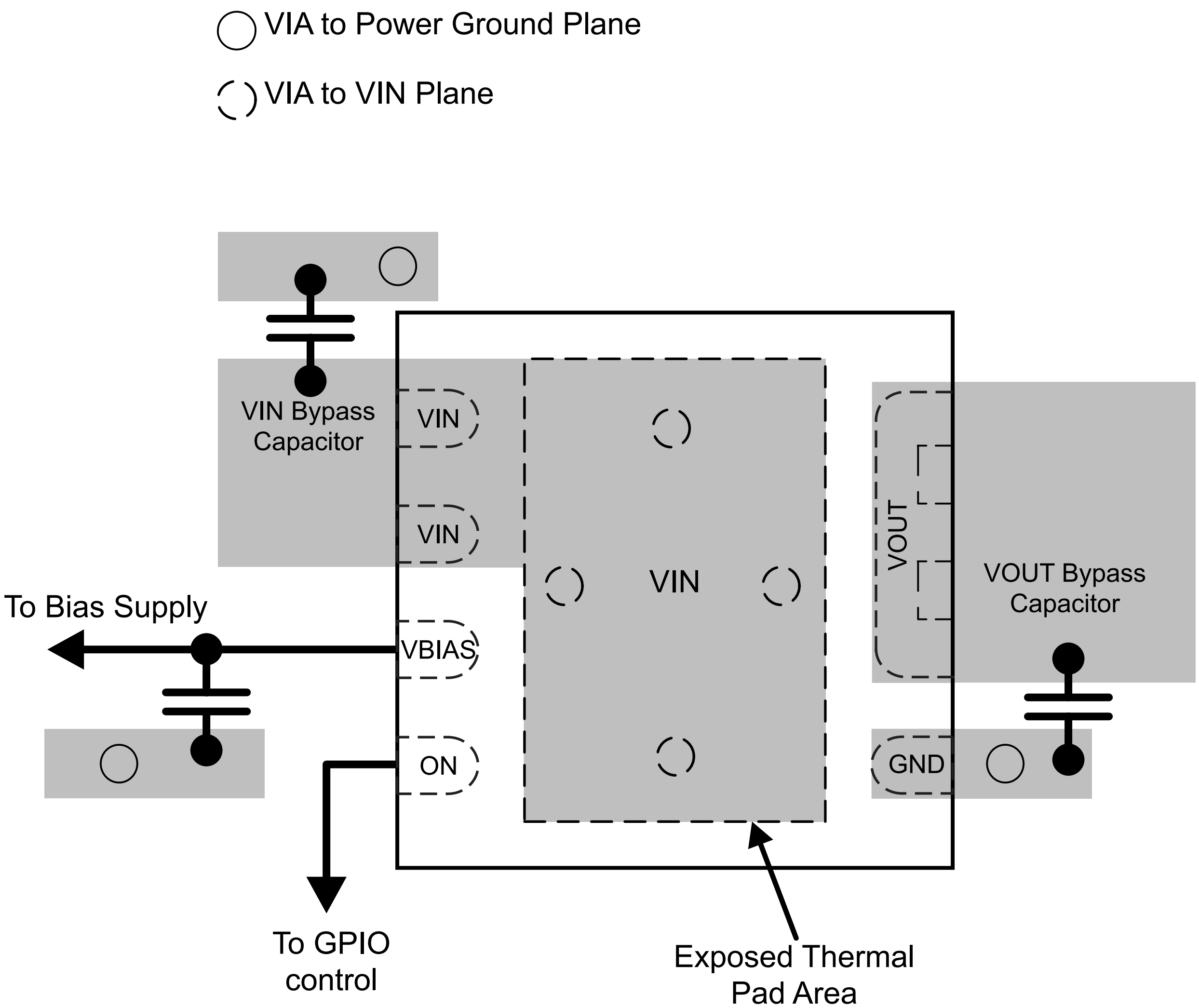


Figure 39. Recommended Board Layout

12 Device and Documentation Support

12.1 Trademarks

Ultrabook is a trademark of Intel.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22969DNYR	ACTIVE	WSON	DNY	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	969A0	Samples
TPS22969DNYT	ACTIVE	WSON	DNY	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	969A0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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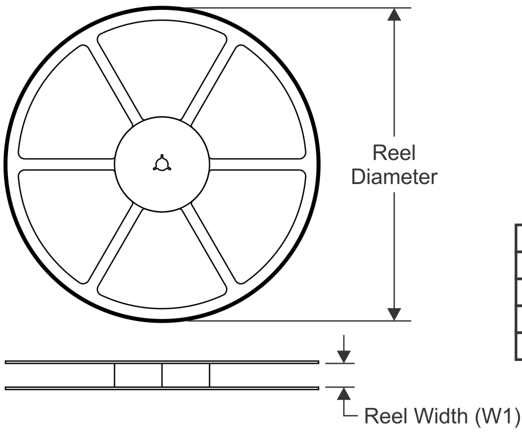
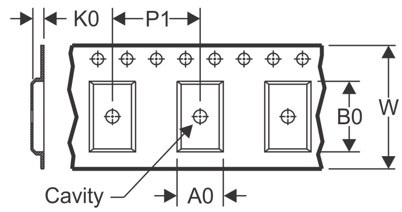
TAPE AND REEL INFORMATION

REEL DIMENSIONS

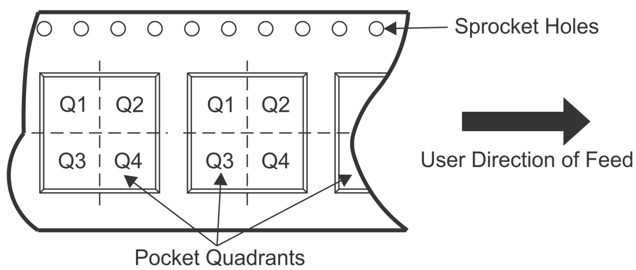


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

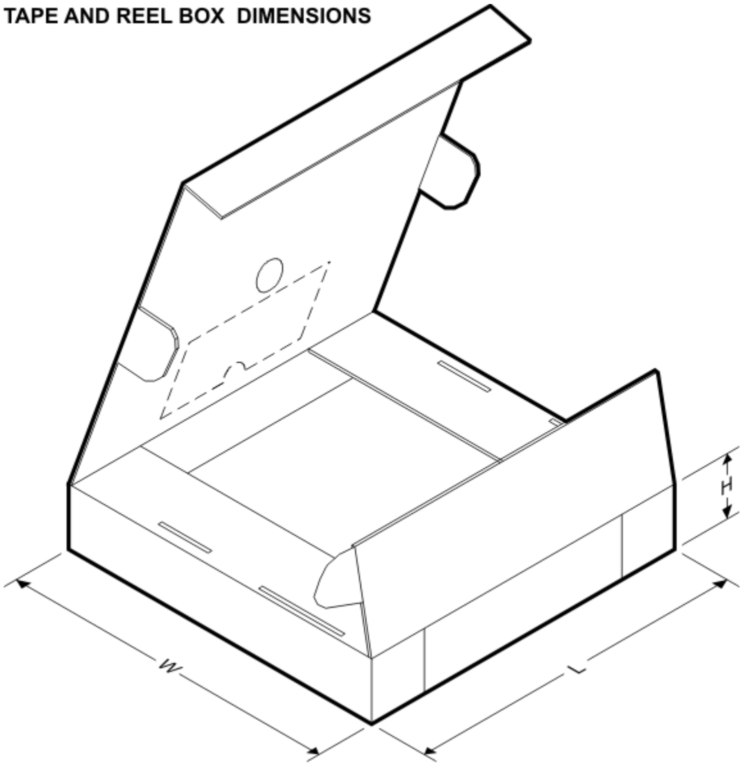
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

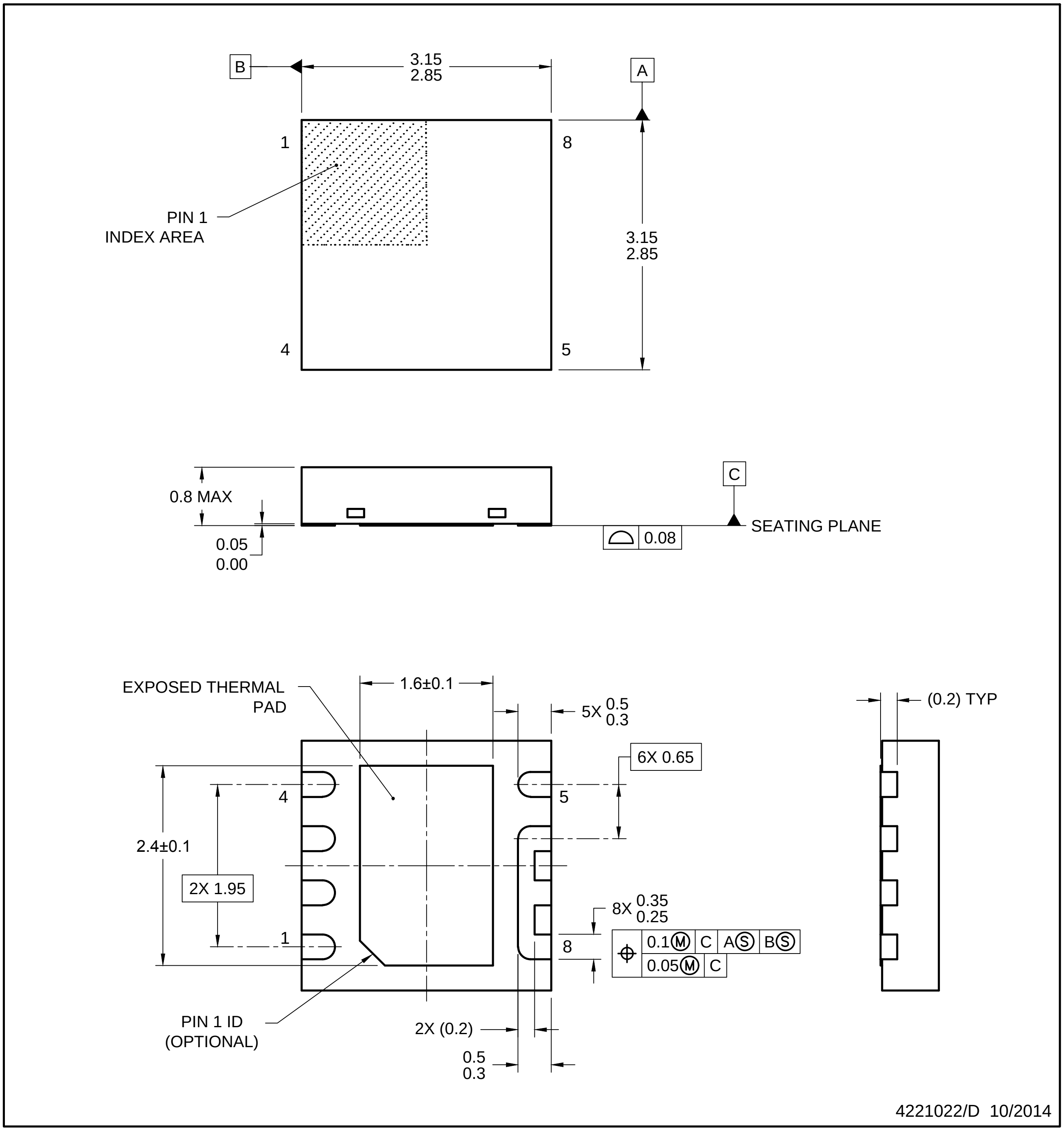
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22969DNYR	WSON	DNY	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS22969DNYT	WSON	DNY	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



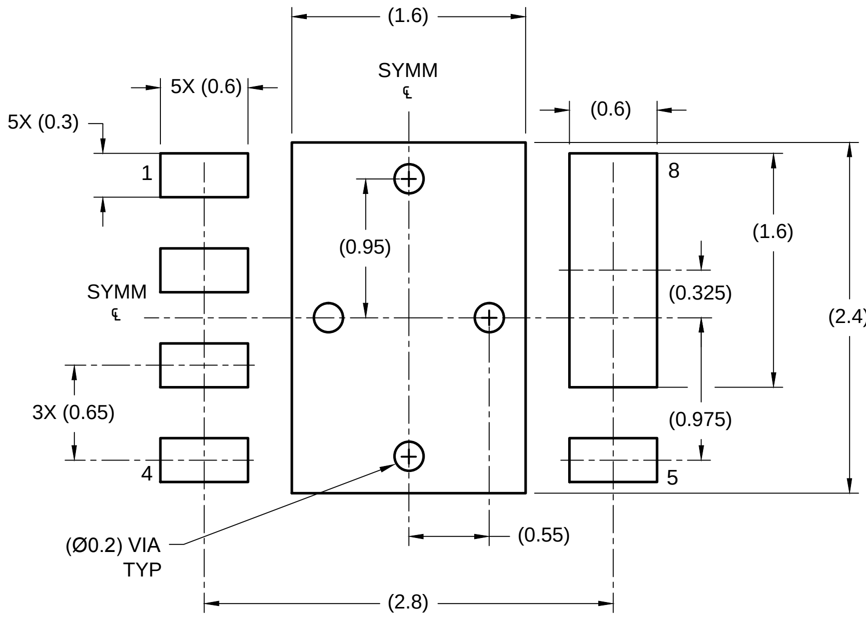
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22969DNYR	WSON	DNY	8	3000	370.0	355.0	55.0
TPS22969DNYT	WSON	DNY	8	250	195.0	200.0	45.0

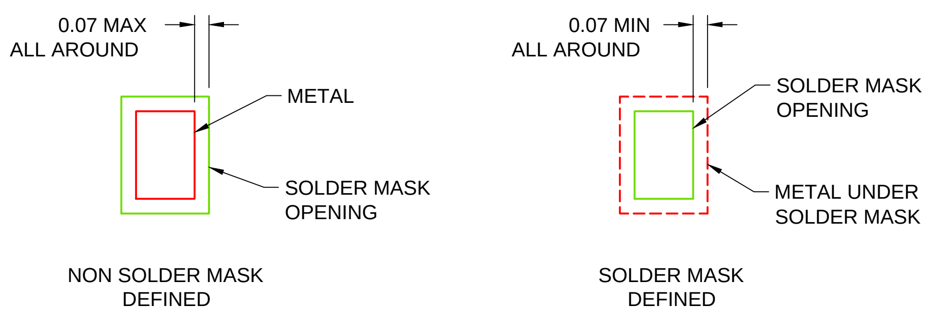


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

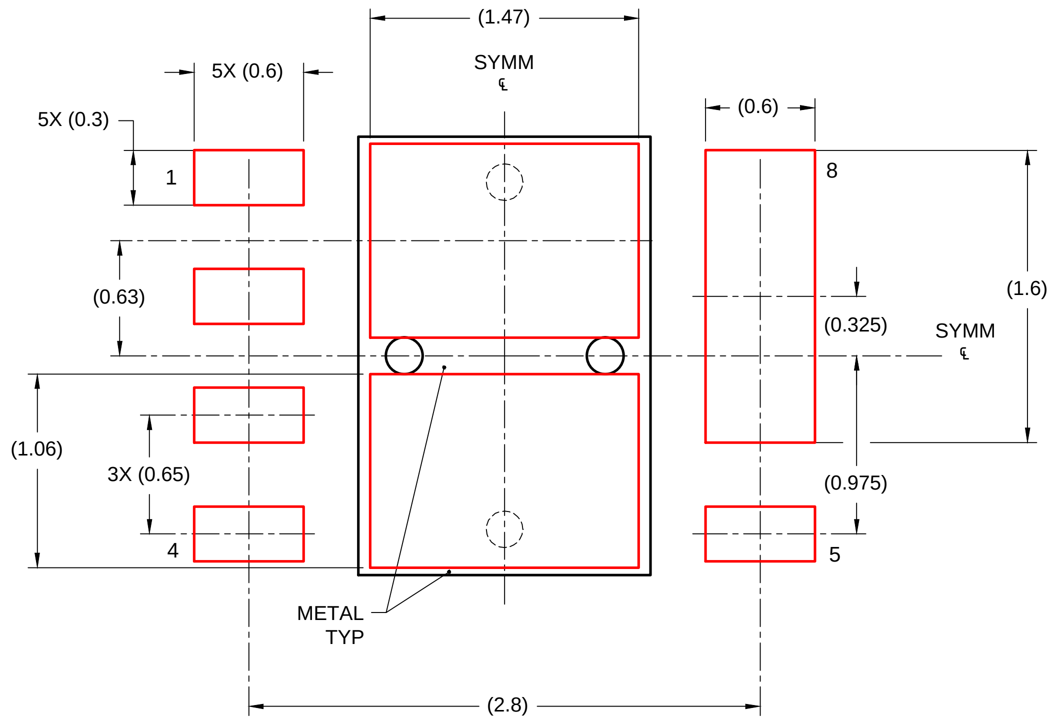


SOLDER MASK DETAILS

4221022/D 10/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE: 25X

4221022/D 10/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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