TPS709-Q1 150-mA, 30-V, 1-µA I_Q Voltage Regulators with Enable

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range: 2.7 V to 30 V
- Ultralow I_Q: 1 µA
- Reverse Current Protection
- Low $I_{SHUTDOWN}$: 150 nA
- Supports 200-mA Peak Output
- 2% Accuracy Over Temperature
- Available in Fixed-Output Voltages: 1.2 V to 6.5 V
- Thermal Shutdown and Overcurrent Protection
- Packages: SOT-23-5, WSON-6

2 Applications

- Automotive
- Infotainment
- Body Control Modules
- Navigation Systems
- Standby Power for Microcontrollers

3 Description

The TPS709-Q1 series of linear regulators are ultralow, quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typical.

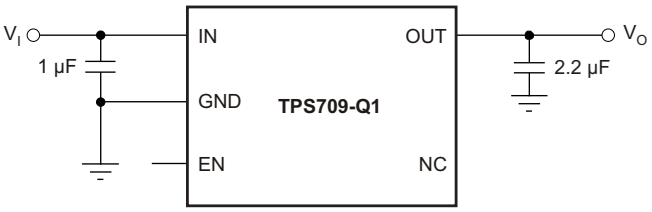
The TPS709-Q1 series is available in WSON-6 and SOT-23-5 packages.

Device Information(1)

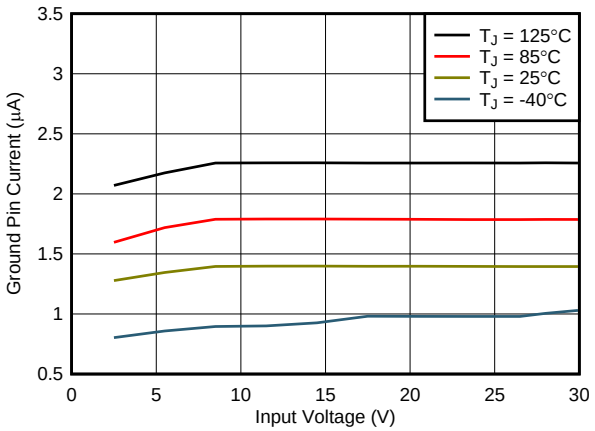
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS709-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



GND Current vs V_{IN} and Temperature



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2013) to Revision B — **Page**

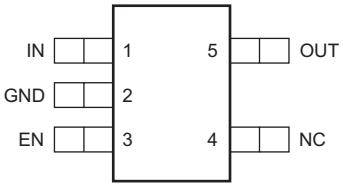
- Added DRV package to document, *ESD Ratings*, *Recommended Operating Conditions*, and *Timing Requirements* tables, and *Overview*, *Device Functional Modes*, *Typical Application*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Changed *Application Information*, *Feature Description*, *Power Supply Recommendations*, and *Layout* sections ... 1
- Deleted *Low Dropout* Features bullet ... 1
- Changed *Applications* section ... 1
- Changed last sentence of *Description* section ... 1
- Added Device Information table ... 1
- Added front-page curve ... 1
- Added DRV package drawing to *Pin Configuration and Functions* section ... 3
- Changed *Pin Functions* table: added DRV and I/O columns, added Thermal pad row, and changed EN pin description ... 3
- Changed *Recommended Operating Conditions* table ... 4
- Added DRV column to *Thermal Information* table ... 4
- Changed *Electrical Characteristics* conditions ... 5
- Changed V_{OUT}, I_{CL}, I_{SHDN}, and I_{REV} symbols in *Electrical Characteristics* table ... 5
- Changed $V_{EN(HI)}$ parameter into $V_{EN(HI)}$ and $V_{EN(LO)}$ parameters in *Electrical Characteristics* table ... 5
- Changed T_A parameter to T_J in *Electrical Characteristics* table ... 5
- Changed *Typical Characteristics* section ... 6
- Changed junction temperature values in first paragraph of *Thermal Protection* section ... 14
- Changed 6.3-V to 10-V in second sentence of *Detailed Design Procedure* section ... 17

Changes from Original (December 2013) to Revision A — **Page**

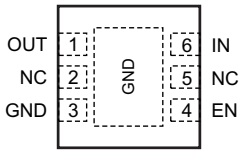
- Changed to production data ... 1

5 Pin Configuration and Functions

DBV Package
SOT-23-5
(Top View)



DRV Package
WSON-6
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. DRV	NO. DBV		
EN	4	3	I	Enable pin. Driving this pin high enables the device. Driving this pin low puts the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	—	Ground
IN	6	1	I	Unregulated input to the device
NC	2, 5	4	—	No internal connection
OUT	1	5	O	Regulated output voltage. Connect a small 2.2-µF or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad		—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

specified at T_J = –40°C to 125°C, unless otherwise noted; all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	32	V
	V_{EN}	–0.3	7	V
	V_{OUT}	–0.3	7	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C
Ambient temperature, T_A		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		30	V
V_{OUT}	Output voltage	1.2		6.5	V
I_{OUT}	Output current	0		150	mA
V_{EN}	Enable voltage	0		6.5	V
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor	2	2.2	47	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS709-Q1		UNIT
		DBV (SOT-23)	DRV (WSON)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	73.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.4	97.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	42.6	
ψ_{JT}	Junction-to-top characterization parameter	16.8	2.9	
ψ_{JB}	Junction-to-board characterization parameter	38.4	42.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At –40°C ≤ T_J, T_A ≤ 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-µF ceramic, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_{OUT}	DC output accuracy	V_{OUT} < 3.3 V	–2%		2%	
		V_{OUT} ≥ 3.3 V	–1%		1%	
ΔV_{OUT}	Line regulation	($V_{OUT(nom)}$ + 1 V, 2.7 V) ≤ V_{IN} ≤ 30 V		3	10	mV
	Load regulation	V_{IN} = $V_{OUT(nom)}$ + 1.5 V or 3 V (whichever is greater), 100 µA ≤ I_{OUT} ≤ 150 mA		20	50	mV
V_{DO}	Dropout voltage(1)(2)	TPS70933-Q1, I_{OUT} = 50 mA		295	650	mV
		TPS70933-Q1, I_{OUT} = 150 mA		975	1540	mV
		TPS70950-Q1, I_{OUT} = 50 mA		245	500	mV
		TPS70950-Q1, I_{OUT} = 150 mA		690	1200	mV
I_{CL}	Output current limit(3)	V_{OUT} = 0.9 × $V_{OUT(nom)}$	200	320	500	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA, V_{OUT} ≤ 3.3 V		1.3	2.55	µA
		I_{OUT} = 0 mA, V_{OUT} > 3.3 V		1.4	2.7	µA
		I_{OUT} = 100 µA, V_{IN} = 30 V		6.7	10	µA
		I_{OUT} = 150 mA		350		µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.7 V		150		nA
PSRR	Power-supply rejection ratio	f = 10 Hz		80		dB
		f = 100 Hz		62		dB
		f = 1 kHz		52		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 10 mA, V_{IN} = 2.7 V, V_{OUT} = 1.2 V		190		μV_{RMS}
$V_{EN(HI)}$	Enable pin high (enabled)		0.9			V
$V_{EN(LO)}$	Enable pin high (disabled)		0		0.4	V
I_{EN}	Enable pin current	EN = 1.0 V, V_{IN} = 5.5 V		300		nA
I_{REV}	Reverse current (flowing out of IN pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		10		nA
	Reverse current (flowing into OUT pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		100		nA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		158		°C
		Reset, temperature decreasing		140		°C
T_J	Operating junction temperature		–40		125	°C

(1) V_{DO} is measured with V_{IN} = 0.98 × $V_{OUT(nom)}$.
(2) Dropout is only valid when V_{OUT} ≥ 2.8 V because of the minimum input voltage limits.
(3) Measured with V_{IN} = V_{OUT} + 3 V for V_{OUT} ≤ 2.5 V. Measured with V_{IN} = V_{OUT} + 2.5 V for V_{OUT} > 2.5 V.

6.6 Timing Requirements

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), R_L = 47 Ω, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-µF ceramic, unless otherwise noted. Typical values are at T_J = 25°C.

			MIN	NOM	MAX	UNIT
t_{STR}	Start-up time(1)	$V_{OUT(nom)}$ ≤ 3.3 V		200	600	µs
		$V_{OUT(nom)}$ > 3.3 V		500	1500	µs

(1) Startup time = time from EN assertion to 0.95 × $V_{OUT(nom)}$ and load = 47 Ω.

6.7 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

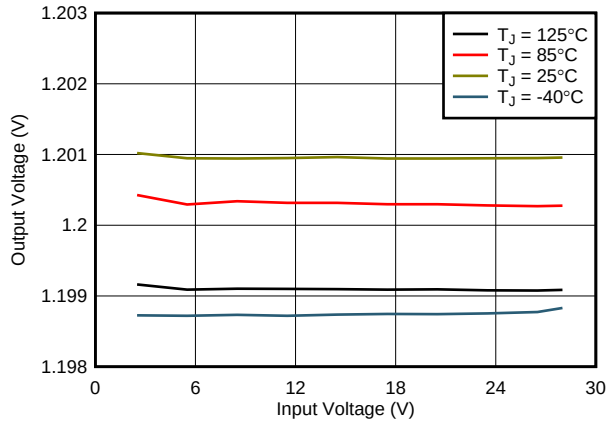


Figure 1. 1.2-V Line Regulation vs V_{IN} and Temperature

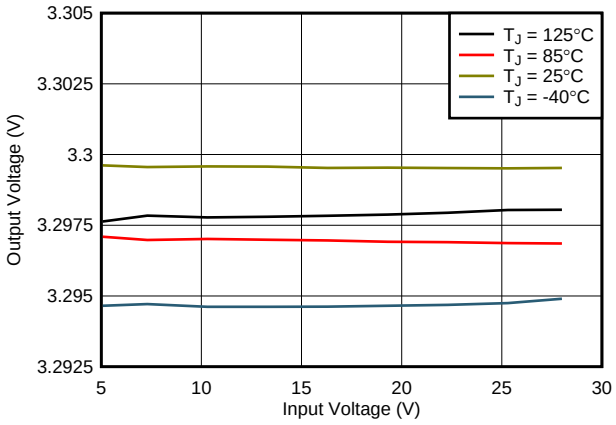


Figure 2. 3.3-V Line Regulation vs V_{IN} and Temperature

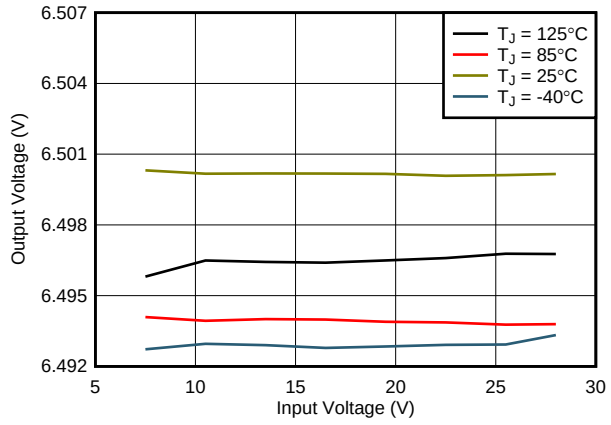


Figure 3. 6.5-V Line Regulation vs V_{IN} and Temperature

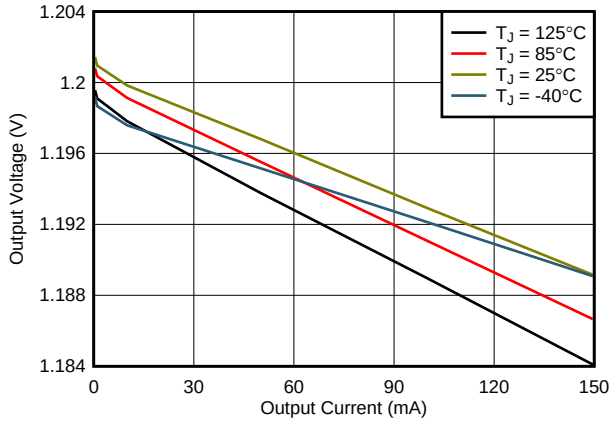


Figure 4. 1.2-V Load Regulation vs I_{OUT} and Temperature

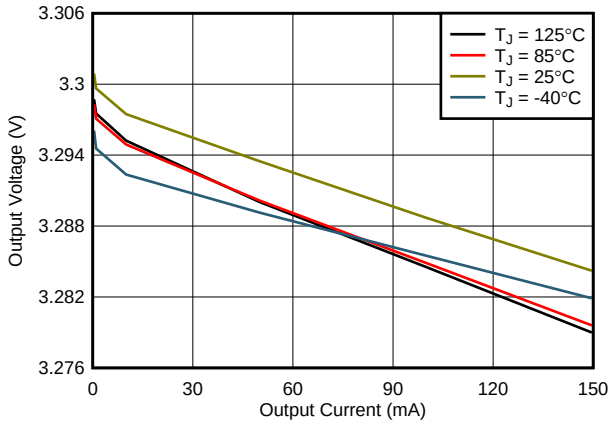


Figure 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

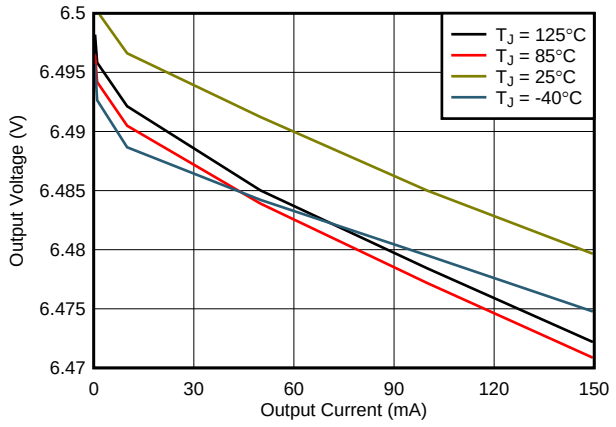


Figure 6. 6.5-V Load Regulation vs I_{OUT} and Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

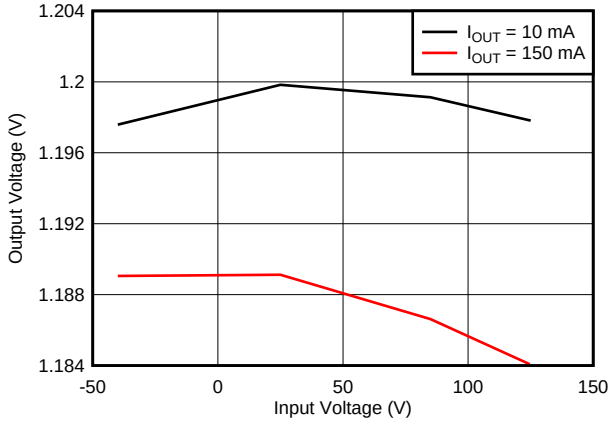


Figure 7. 1.2-V Output Voltage vs Temperature

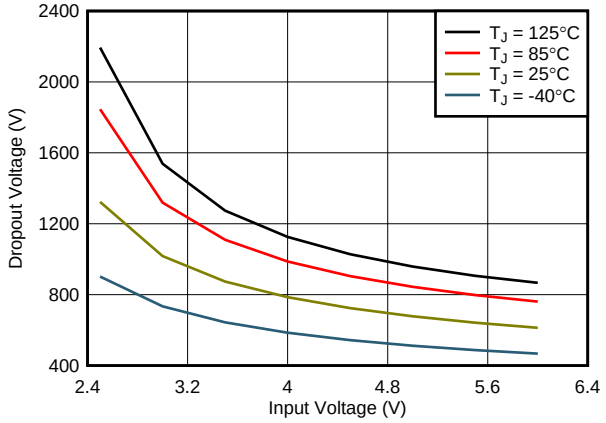


Figure 8. 6.5-V Dropout Voltage vs V_{IN} and Temperature

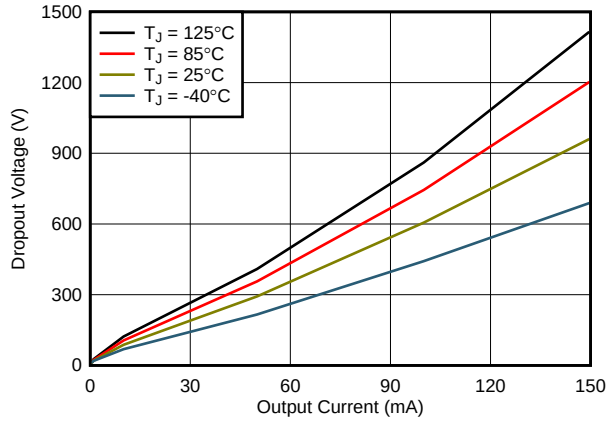


Figure 9. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

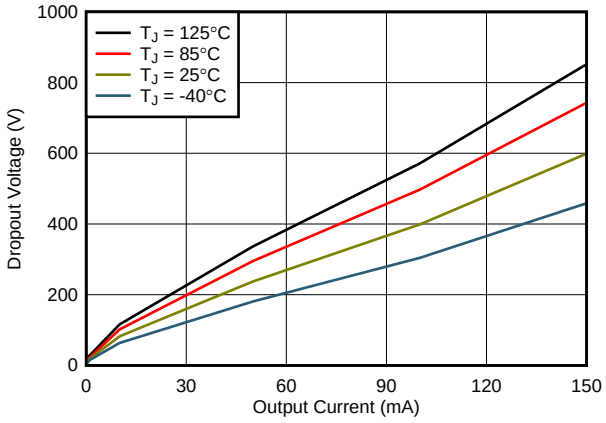


Figure 10. Dropout Voltage vs I_{OUT} and Temperature

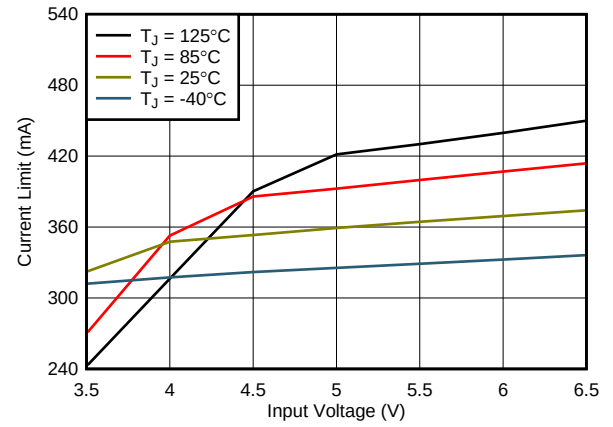


Figure 11. 1.2-V Current Limit vs V_{IN} and Temperature

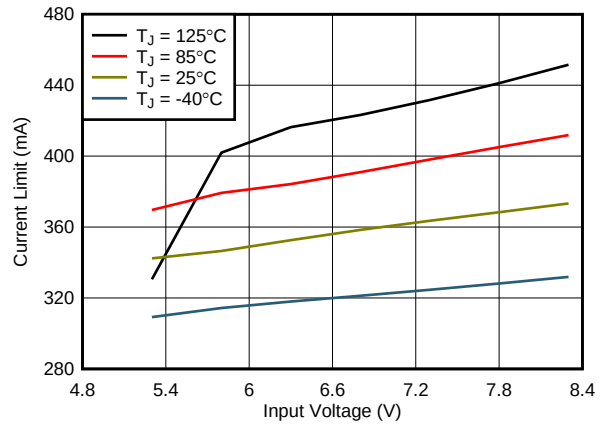


Figure 12. 3.3-V Current Limit vs V_{IN} and Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

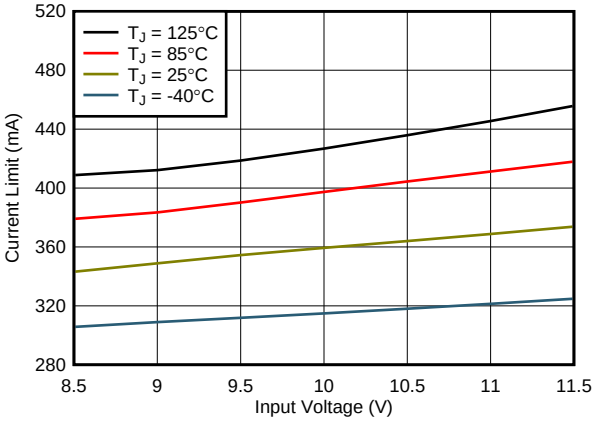


Figure 13. 6.5-V Current Limit vs V_{IN} and Temperature

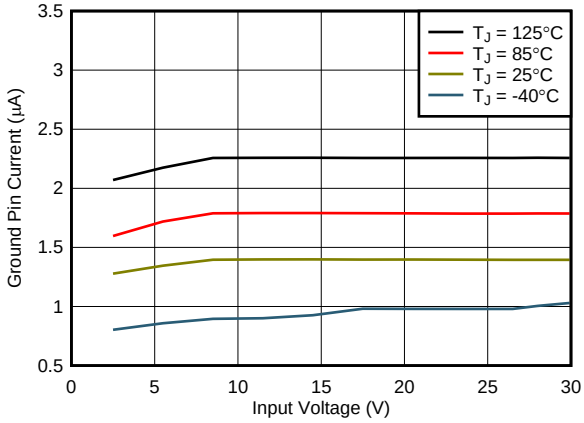


Figure 14. 1.2-V Ground Pin Current vs V_{IN} and Temperature

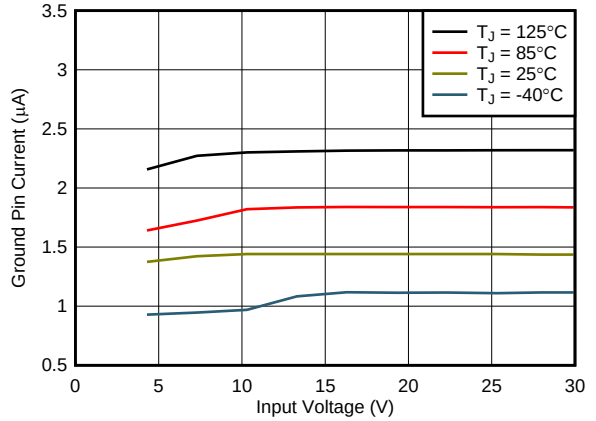


Figure 15. 3.3-V Ground Pin Current vs V_{IN} and Temperature

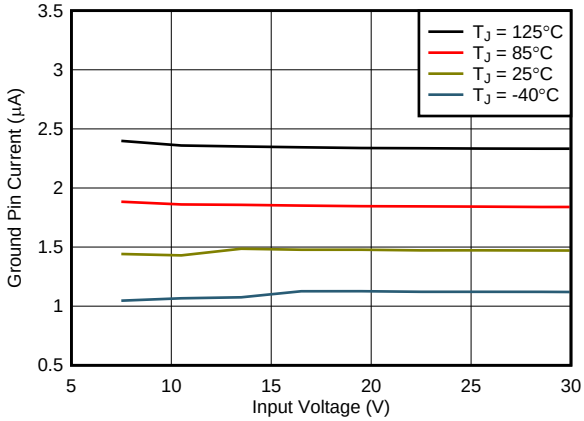


Figure 16. 6.5-V Ground Pin Current vs V_{IN} and Temperature

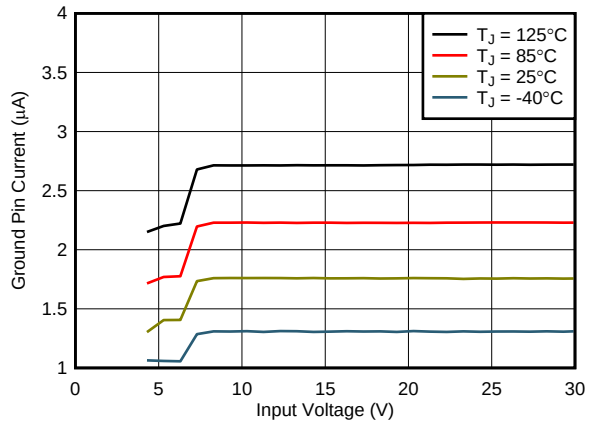


Figure 17. 3.3-V Ground Current vs V_{IN} and Temperature with EN Floating

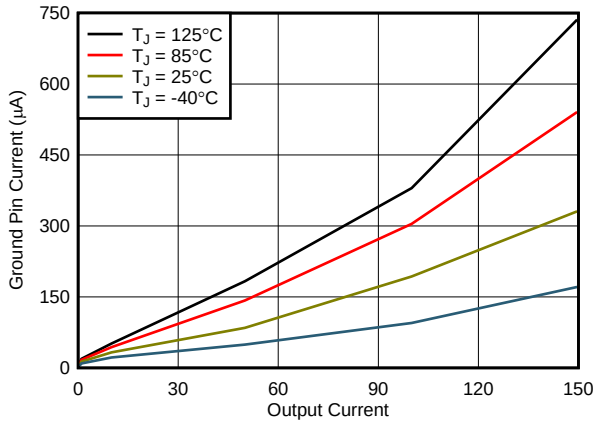


Figure 18. 1.2-V Ground Pin Current vs I_{OUT} and Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

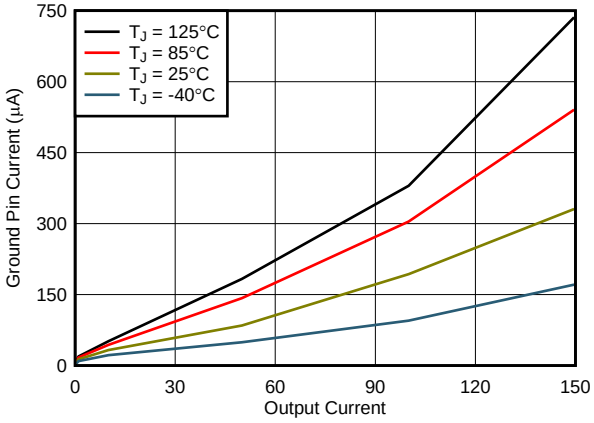


Figure 19. 3.3-V Ground Pin Current vs I_{OUT} and Temperature

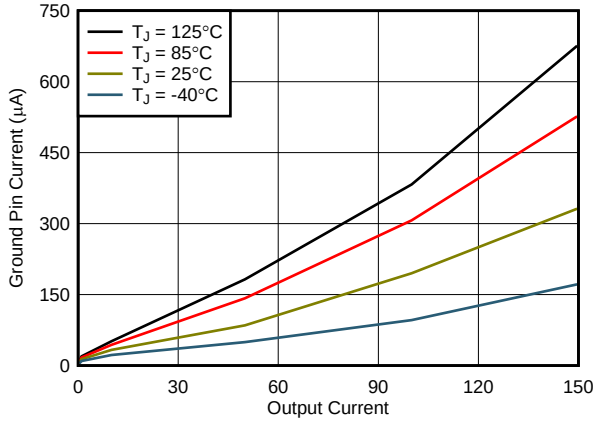


Figure 20. 6.5-V Ground Pin Current vs I_{OUT} and Temperature

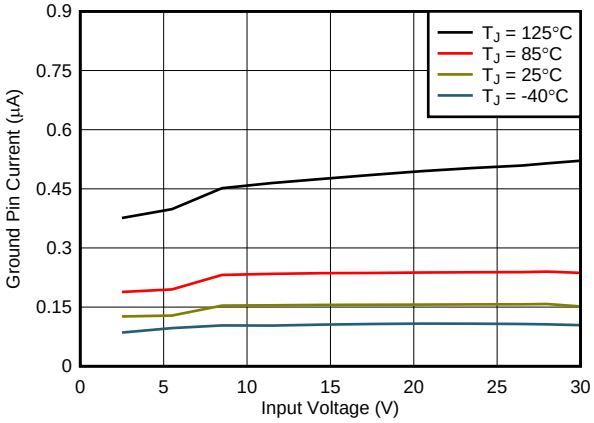


Figure 21. 1.2-V Shutdown Current vs V_{IN} and Temperature

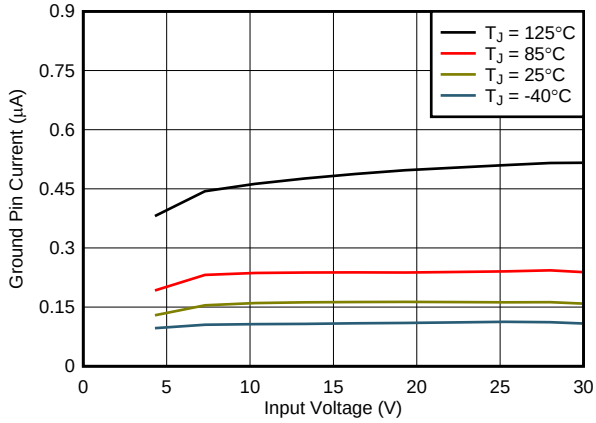


Figure 22. 3.3-V Shutdown Current vs V_{IN} and Temperature

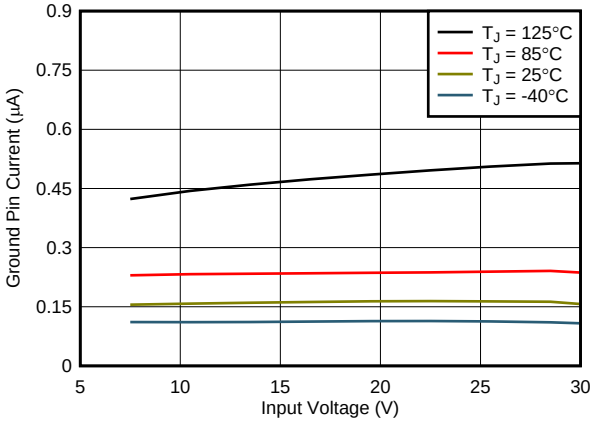


Figure 23. 6.5-V Shutdown Current vs V_{IN} and Temperature

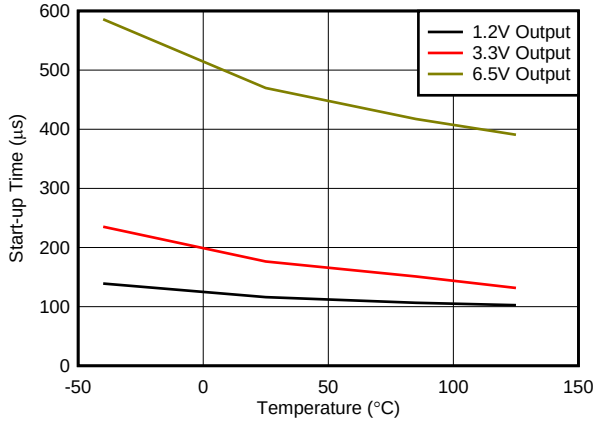


Figure 24. Start-Up Time vs Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

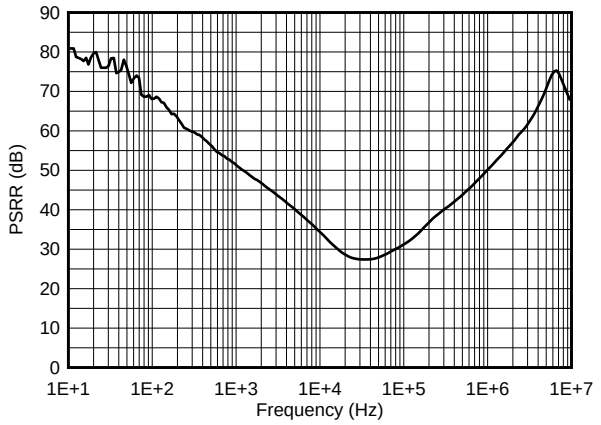


Figure 25. Power-Supply Rejection Ratio vs Frequency

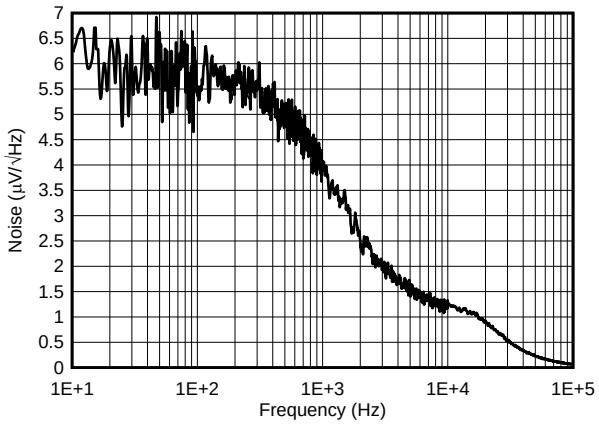
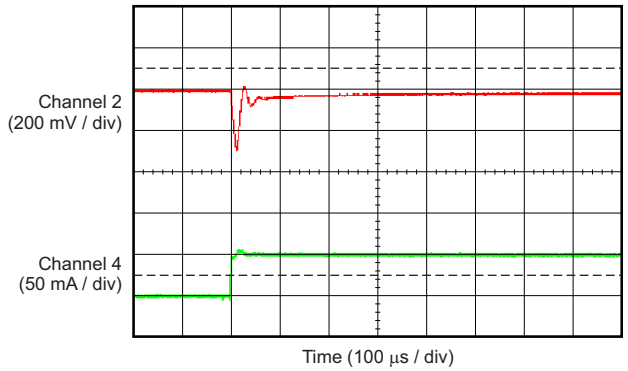
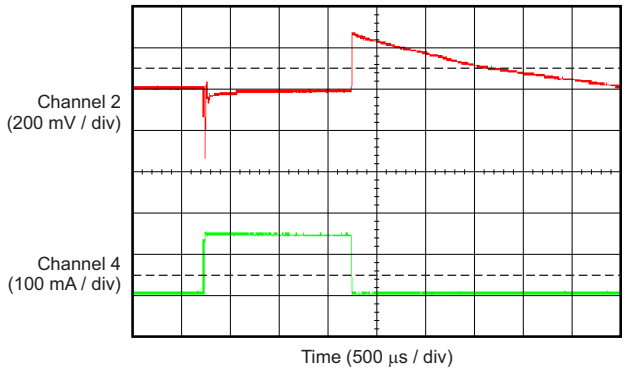


Figure 26. Noise



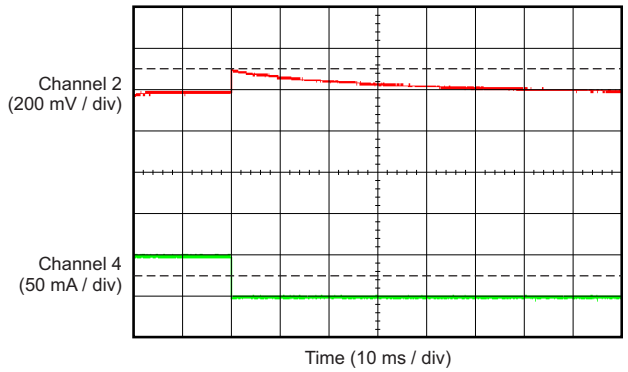
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 27. TPS70912-Q1 Load Transient (0 mA to 50 mA)



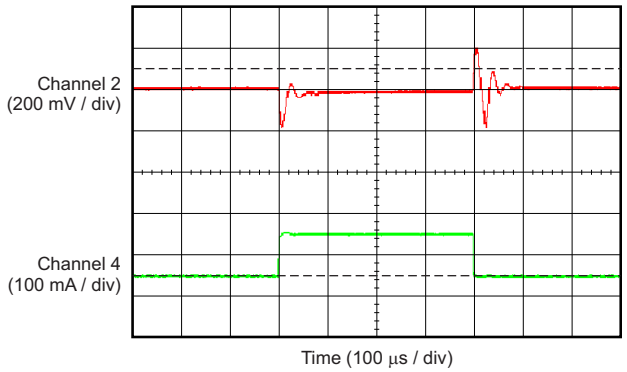
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 28. TPS70912-Q1 Load Transient (1 mA to 150 mA)



Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 29. TPS70912-Q1 Load Transient (50 mA to 0 mA)

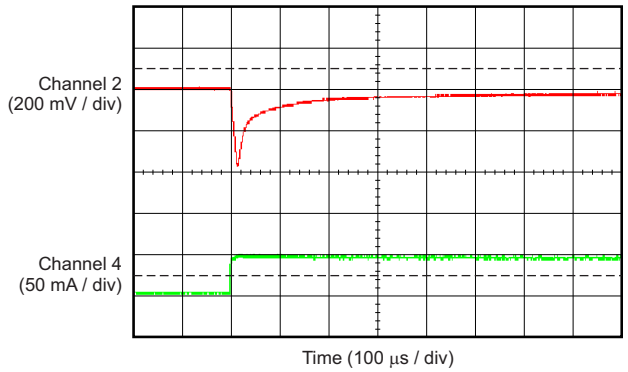


Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 30. TPS70912-Q1 Load Transient (50 mA to 150 mA)

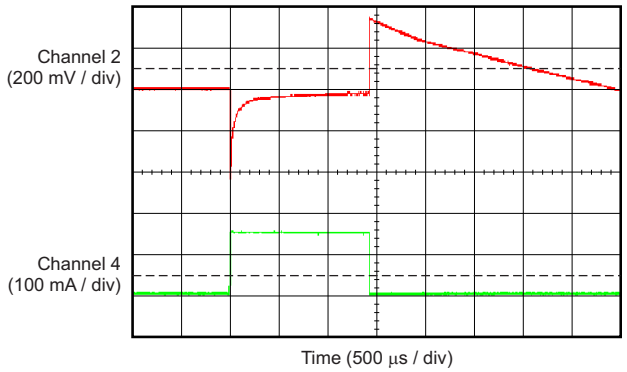
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.



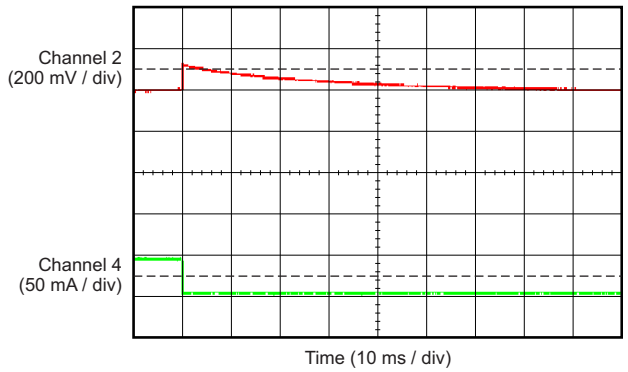
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 31. TPS70933-Q1 Load Transient (0 mA to 50 mA)



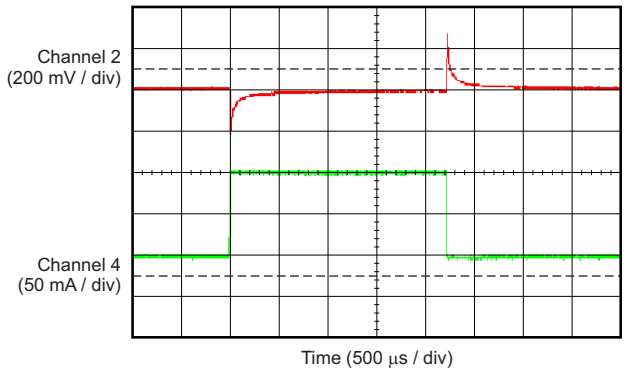
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 32. TPS70933-Q1 Load Transient (1 mA to 150 mA)



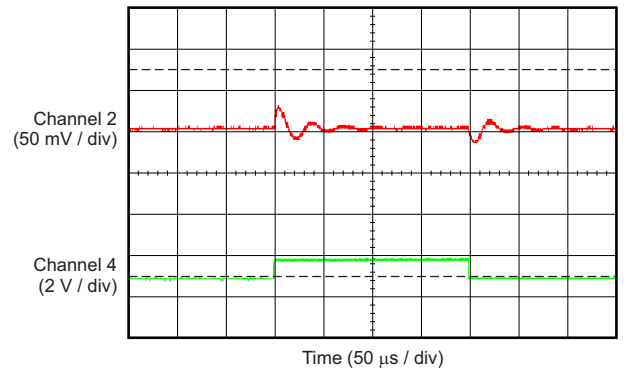
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 33. TPS70933-Q1 Load Transient (50 mA to 0 mA)



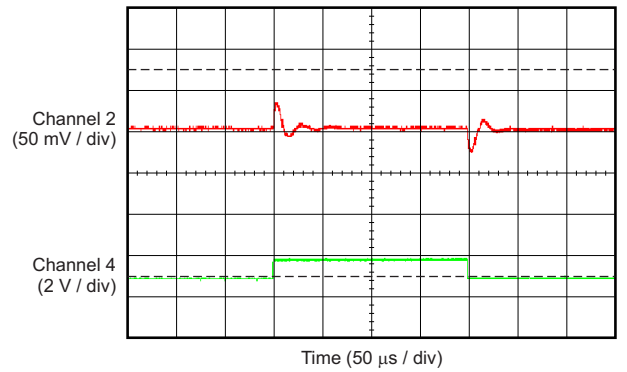
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 34. TPS70933-Q1 Load Transient (50 mA to 150 mA)



Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 10 mA

Figure 35. TPS70912-Q1 Line Transient (2.7 V to 3.7 V)

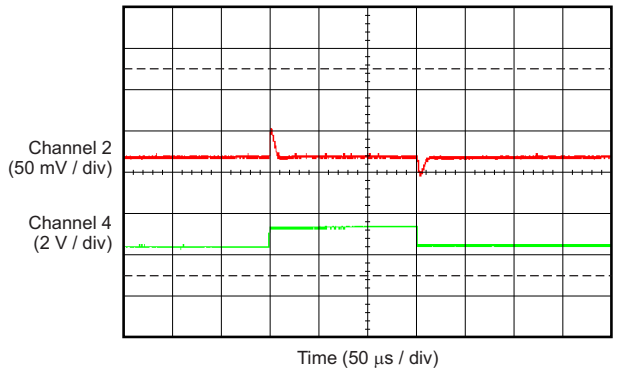


Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 50 mA

Figure 36. TPS70912-Q1 Line Transient (2.7 V to 3.7 V)

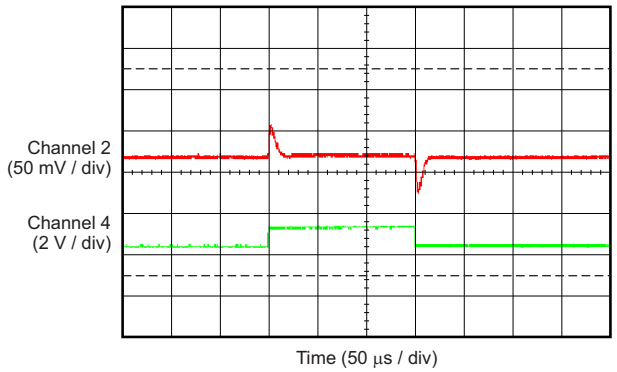
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.



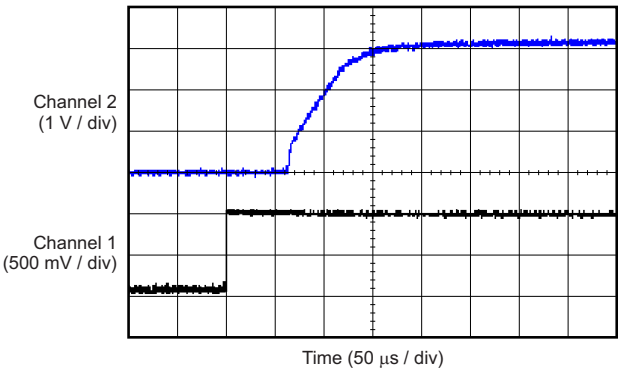
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 10 mA

Figure 37. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



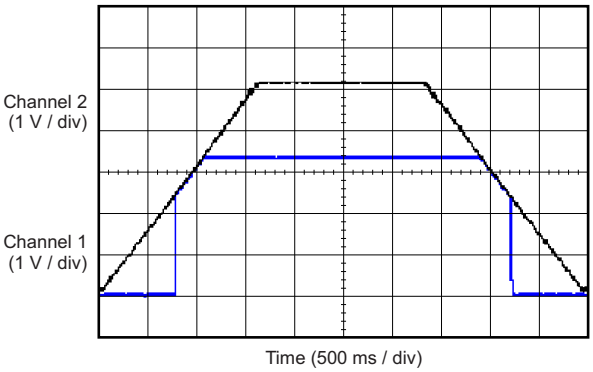
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 50 mA

Figure 38. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



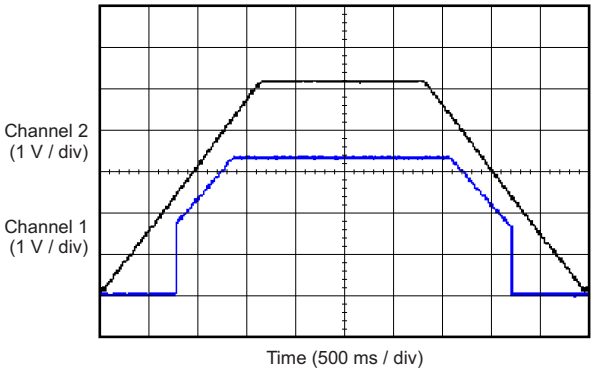
Channel 1 = EN, channel 2 = V_{OUT}, V_{IN} = 4.3 V, C_{OUT} = 2.2 µF, TPS70633

Figure 39. Power-Up with Enable



Channel 1 = V_{IN}, channel 2 = V_{OUT}, I_{OUT} = 3 mA, TPS70633

Figure 40. Power-Up and Power-Down Response



Channel 1 = V_{IN}, channel 2 = V_{OUT}, I_{OUT} = 150 mA, TPS70633

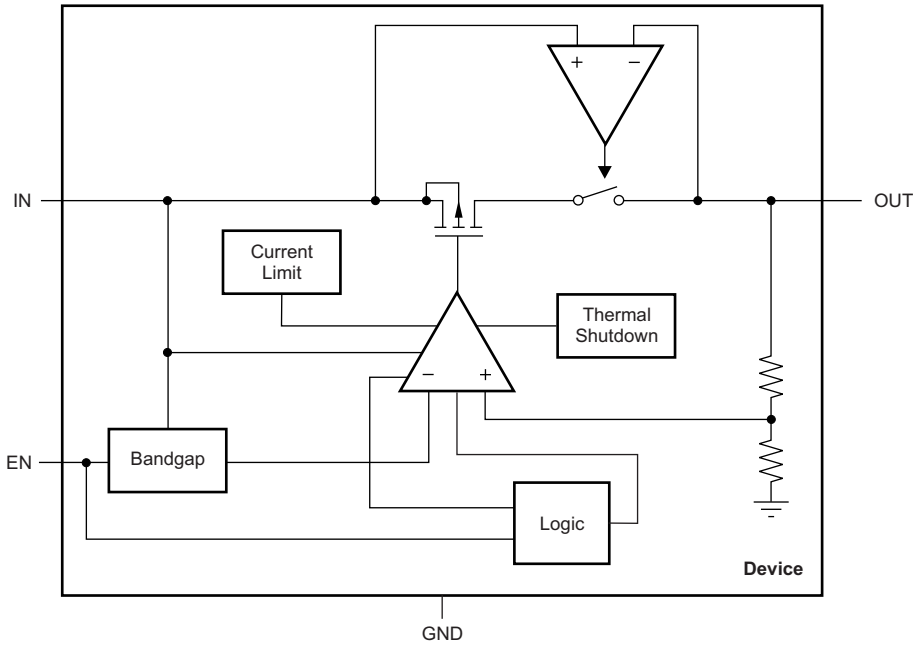
Figure 41. Power-Up and Power-Down Response

7 Detailed Description

7.1 Overview

The TPS709-Q1 series are ultralow quiescent current, low-dropout (LDO) linear regulators. The TPS709-Q1 offers reverse current protection to block any discharge current from the output into the input. The TPS709-Q1 also features current limit and thermal shutdown for reliable operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS709-Q1 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V. If shutdown capability is not required, connect EN to IN.

7.3.3 Reverse Current Protection

The TPS709-Q1 has integrated reverse current protection. Reverse current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 3.3-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

Feature Description (continued)

7.3.4 Internal Current Limit

The TPS709-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [($V_{IN} - V_{OUT}$) × I_{LIMIT}] until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* section for more details.

The TPS709-Q1 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current.

7.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS709-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS709-Q1 consumes low quiescent current and delivers excellent line and load transient performance. This performance, combined with low noise and good PSRR with little (V_{IN} – V_{OUT}) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709-Q1 devices are specified from –40°C to 125°C.

8.1.1 Input and Output Capacitor Considerations

The TPS709-Q1 devices are stable with output capacitors with an effective capacitance of 2.0 µF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 µF. The maximum capacitance for stability is 47 µF. The equivalent series resistance (ESR) of the output capacitor must be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 2.2-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR.

8.1.2 Dropout Voltage

The TPS709-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709-Q1 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

8.1.3 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

8.2 Typical Application

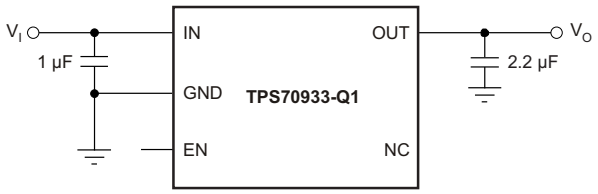


Figure 42. 3.3-V, Low-I_Q Rail

8.2.1 Design Requirements

Table 2 summarizes the design requirements for Figure 42.

Table 2. Design Requirements for a 3.3-V, Low-I_Q Rail Application

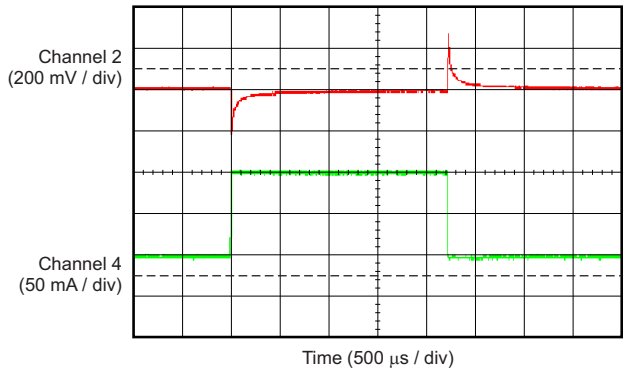
PARAMETER	DESIGN SPECIFICATION
V_{IN}	4.3 V
V_{OUT}	3.3 V
$I_{(IN)}$ (no load)	< 5 µA
I_{OUT} (max)	150 mA

8.2.2 Detailed Design Procedure

Select a 2.2-µF, 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

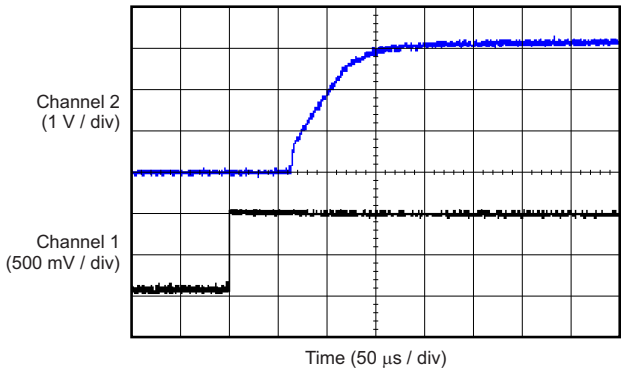
Select a 1.0-µF, 10-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

8.2.3 Application Curves



Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 43. TPS70933-Q1 Load Transient (50 mA to 150 mA)



Channel 1 = EN, channel 2 = V_{OUT}, V_{IN} = 4.3 V, C_{OUT} = 2.2 µF, TPS70933-Q1

Figure 44. Power-Up with Enable

9 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 6.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Figure 45 shows the maximum ambient temperature versus the power dissipation of the TPS709-Q1. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS709-Q1 does not operate above a junction temperature of 125°C.

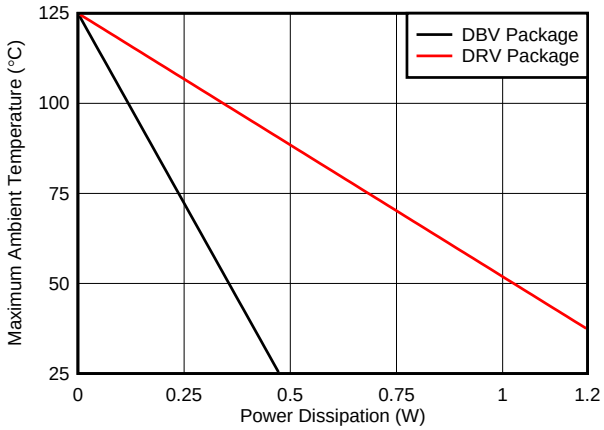


Figure 45. Maximum Ambient Temperature vs Device Power Dissipation

Layout Guidelines (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 2.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D \tag{2}$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where:

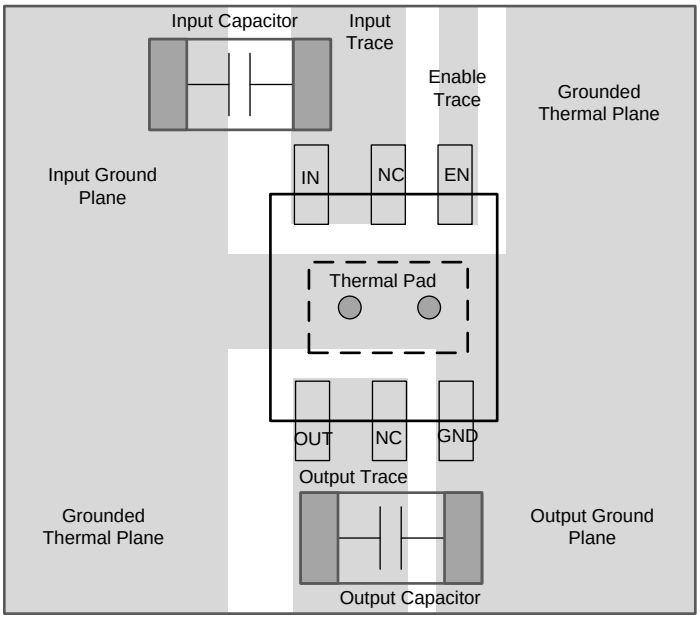
- P_D is the power dissipation shown by Equation 1,
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

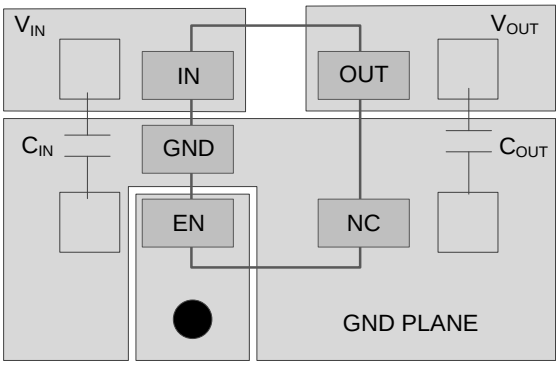
For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

10.2 Layout Examples



Designates thermal vias.

Figure 46. WSON Layout Example



Represents via used for application-specific connections.

Figure 47. SOT23-5 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS709-Q1. The TPS70933EVM-110 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS709 is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS709**xx(x)***yyyz*-Q1	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

SLVU689 — TPS70933EVM-110 Evaluation Module User Guide

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70912QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLR	Samples
TPS70912QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJD	Samples
TPS70915QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJE	Samples
TPS70918QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLS	Samples
TPS70918QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJF	Samples
TPS70925QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLT	Samples
TPS70925QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJG	Samples
TPS70927QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJH	Samples
TPS70928QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLU	Samples
TPS70928QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJI	Samples
TPS70930QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV	Samples
TPS70930QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJJ	Samples
TPS70933QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ	Samples
TPS70933QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJK	Samples
TPS70936QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLW	Samples
TPS70950QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLX	Samples
TPS70950QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS709-Q1 :

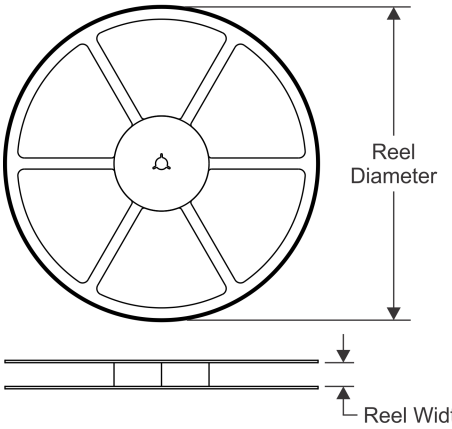
- Catalog: TPS709

NOTE: Qualified Version Definitions:

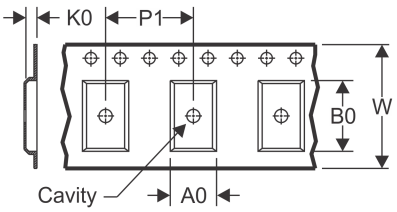
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

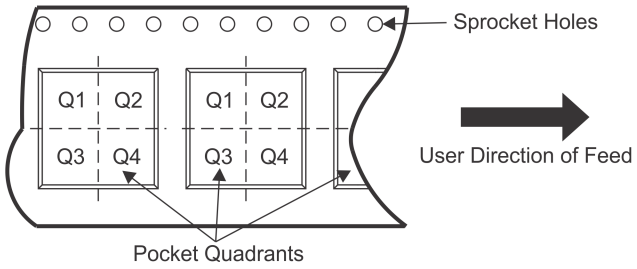


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

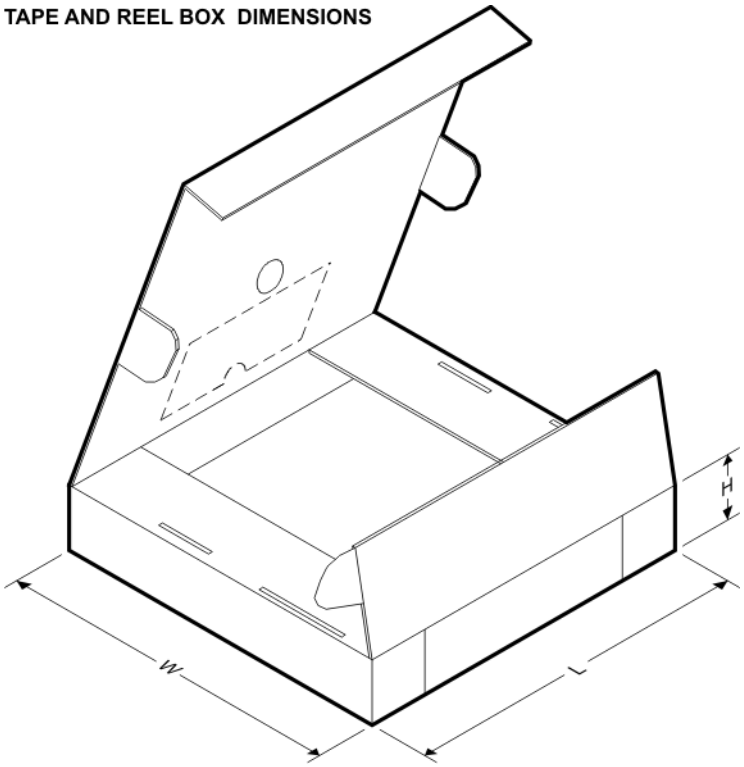
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70927QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

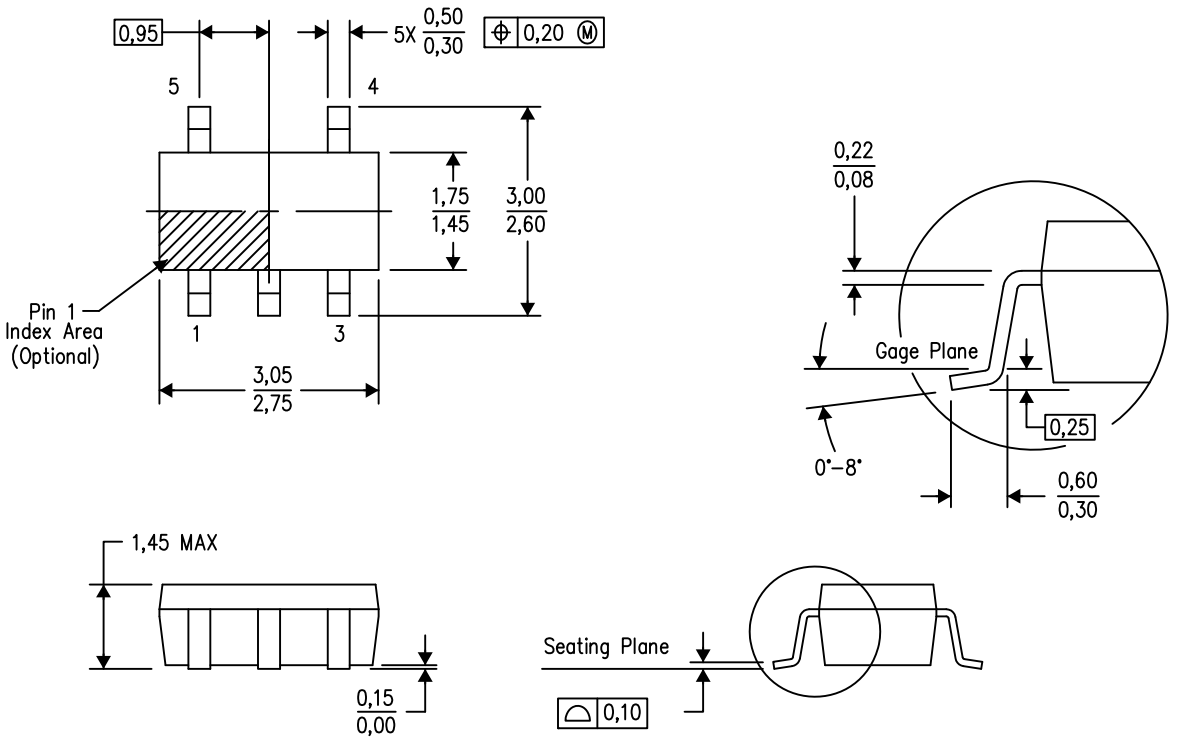
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70915QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70927QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDRVRQ1	SON	DRV	6	3000	203.0	203.0	35.0

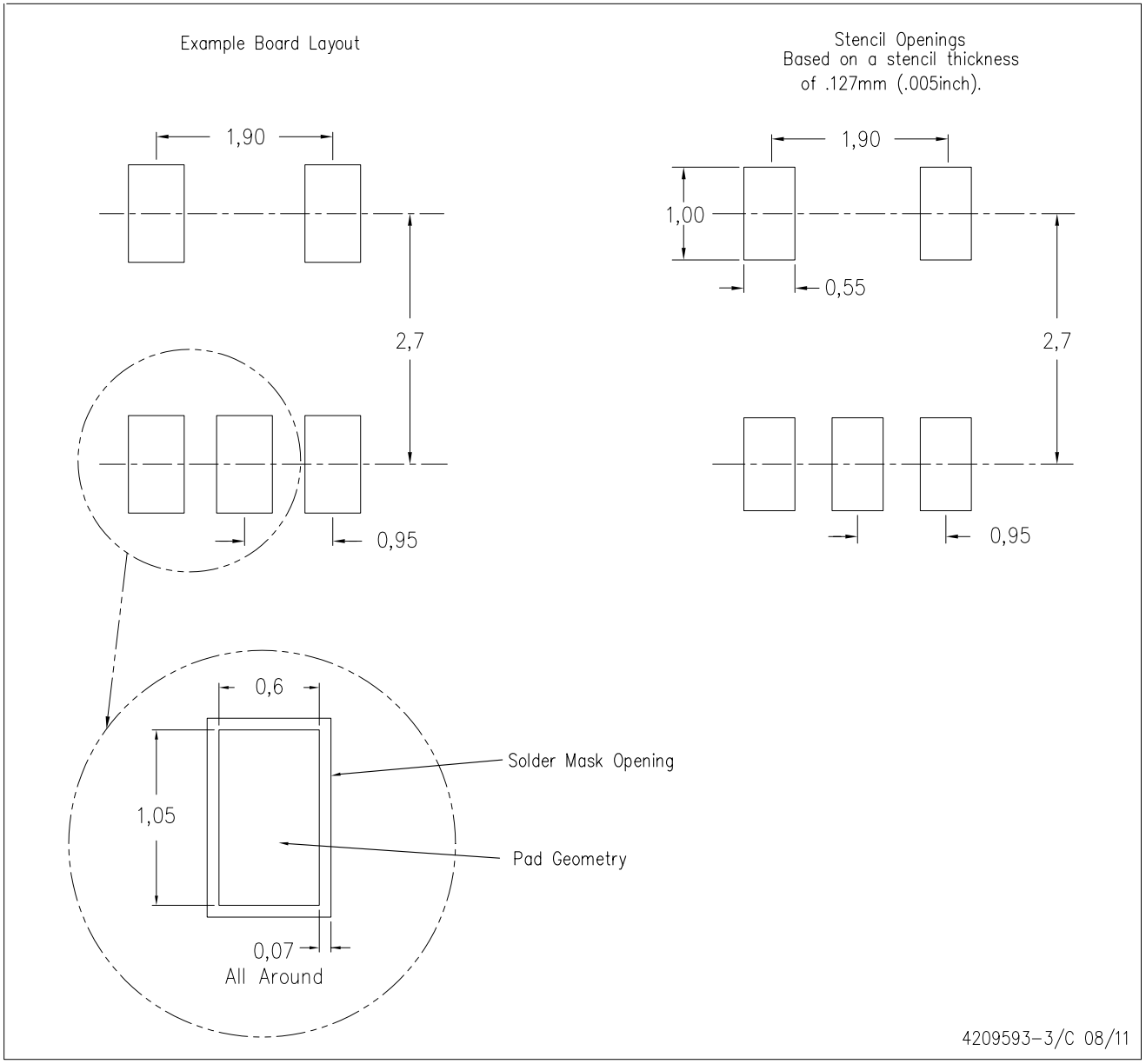
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

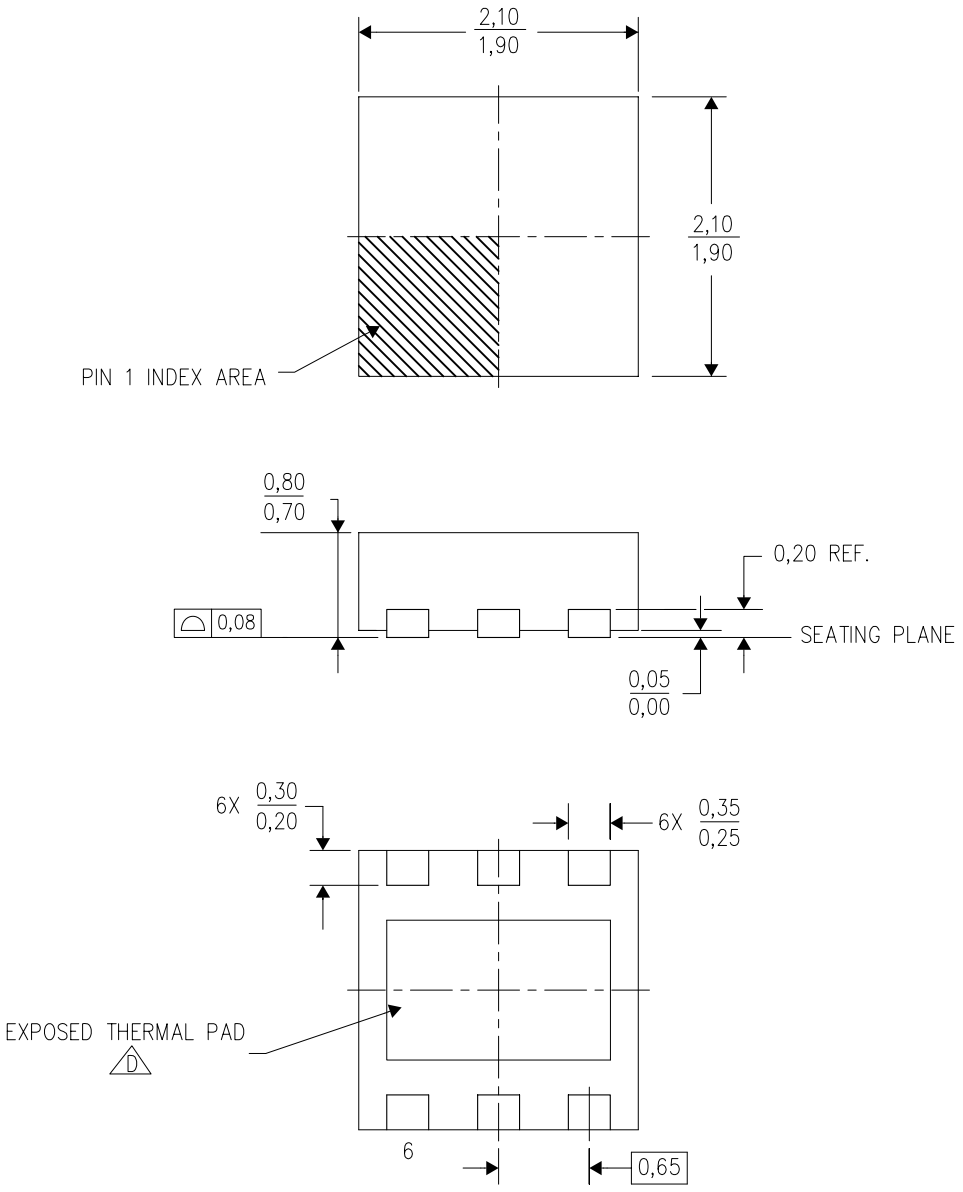
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

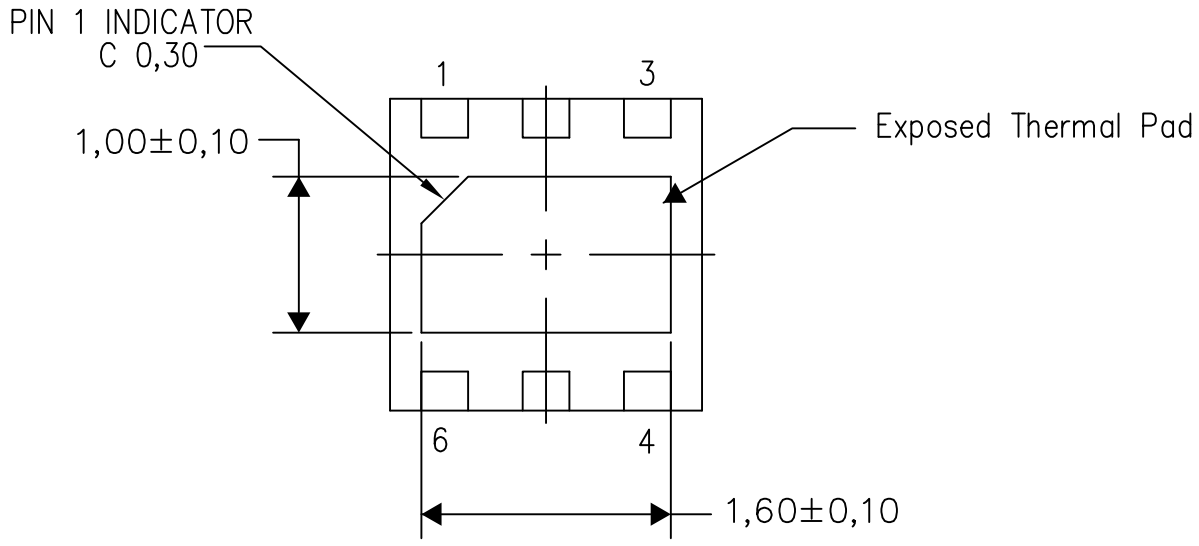
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



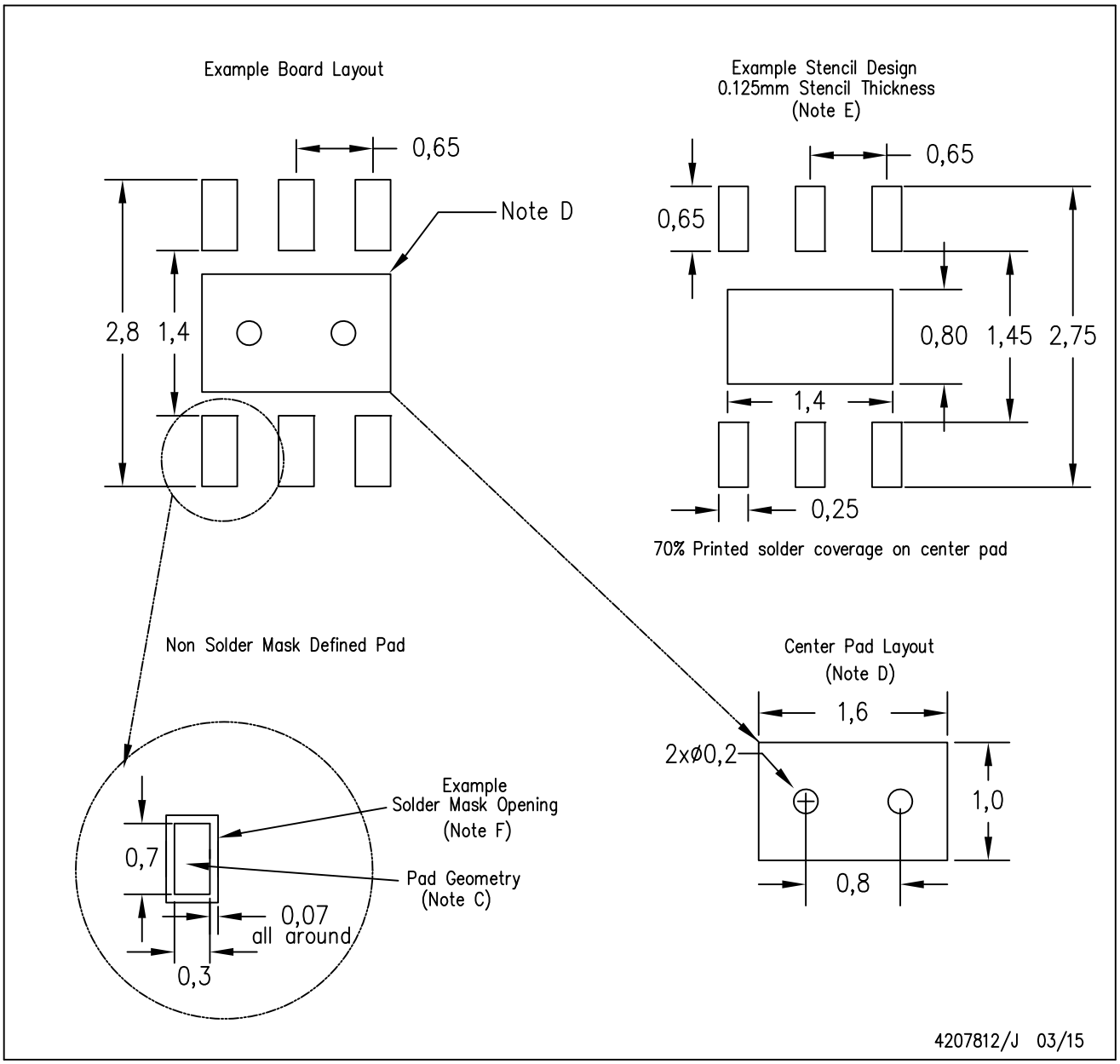
Bottom View

Exposed Thermal Pad Dimensions

4206926/P 03/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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