

50-mA, 24-V, 3.2- μ A Supply Current Low-Dropout Linear Regulators in SC70 Package

Check for Samples: [TPS71501-Q1](#), [TPS71525-Q1](#), [TPS71530-Q1](#), [TPS71533-Q1](#), [TPS71550-Q1](#)

FEATURES

- **Qualified for Automotive Applications**
 - Automotive grade 1 (Q-temperature range)
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C4B
- **24-V Maximum Input Voltage**
- **Low 3.2- μ A Quiescent Current at 50 mA**
- **Stable With Any Capacitor (>0.47 μ F)**
- **50-mA Low-Dropout Regulator**
- **Available in 2.5 V, 3 V, 3.3 V, 5 V, and Adjustable (1.2 V to 15 V)**
- **Minimum/Maximum Specified Current Limit**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **–40°C to 125°C Specified Junction Temperature Range**

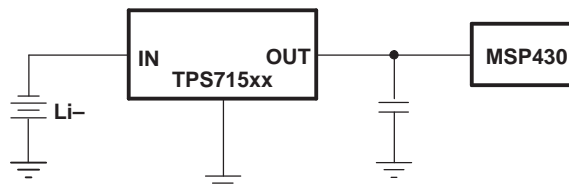
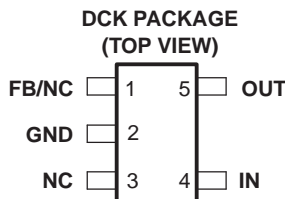
APPLICATIONS

- **Ultra-Low-Power Microcontrollers**
- **Cellular/Cordless Handsets**
- **Portable/Battery-Powered Equipment**

DESCRIPTION

The TPS715xx low-dropout (LDO) voltage regulators offer the benefits of high input voltage, LDO voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (>0.47 μ F). The LDO voltage and low quiescent current allow operations at extremely low power levels. Therefore, the devices are ideal for powering battery-management ICs. Specifically, since the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery-charging ICs.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the LDO voltage, typically 415 mV at 50 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 μ A typ) is stable over the entire range of output load current (0 mA to 50 mA).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Contact Texas Instruments for other voltage options between 1.25 V and 5.85 V.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)^{(1) (2)}

	UNIT
V _{IN} range	–0.3 V to 24 V
V _{OUT} range	–0.3 V to 16.5 V
Peak output current	Internally limited
ESD rating, HBM H2	2 kV
ESD rating, CDM C4B	750 V
Continuous total power dissipation	See Dissipation Rating Table
Junction temperature range, T _J	–40°C to 150°C
Storage temperature range, T _{stg}	–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	R _{θJC} °C/W	R _{θJA} °C/W	DERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
Low-K ⁽¹⁾	DCK	165	395	2.52 mW/°C	250 mW	140 mW	100 mW
High-K ⁽²⁾	DCK	165	315	3.18 mW/°C	320 mW	175 mW	130 mW

- (1) The JEDEC Low-K (1s) board design used to derive this data was a 3-in × 3-in, two-layer board with 2-oz copper traces on top of the board.
- (2) The JEDEC High-K (2s2p) board design used to derive this data was a 3-in × 3-in, multilayer board with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

over operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage ⁽¹⁾	$I_O = 10\text{ mA}$	2.5		24	V
		$I_O = 50\text{ mA}$	3		24	
	V_{OUT} voltage range (TPS71501)		1.2		15	V
	V_{OUT} accuracy ⁽¹⁾ over V_{IN} , I_{OUT} , and T	$V_{IN} + 1\text{ V} \leq V_{IN} \leq 24\text{ V}$, $100\text{ }\mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$	-4%		4%	
I_{GND}	Ground-pin current	$0\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$		3.2	12	μA
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	$I_{OUT} = 100\text{ }\mu\text{A}$ to 50 mA		22		mV
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation ⁽¹⁾	$V_{OUT} + 1\text{ V} < V_{IN} \leq 24\text{ V}$		20	60	mV
V_n	Output noise voltage	BW = 200 Hz to 100 kHz, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 50\text{ mA}$		575		μVrms
I_{CL}	Output current limit	$V_{OUT} = 0\text{ V}$, $V_{IN} \geq 3.5\text{ V}$	125		750	mA
		$V_{OUT} = 0\text{ V}$, $V_{IN} < 3.5\text{ V}$	90		750	
PSRR	Power-supply ripple rejection	$f = 100\text{ kHz}$, $C_{OUT} = 10\text{ }\mu\text{F}$		60		dB
V_{DO}	Dropout voltage, $V_{IN} = V_{OUT(NOM)} - 1\text{ V}$	$I_{OUT} = 50\text{ mA}$		415	750	mV

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or the value shown for input voltage in this table, whichever is greater.

FUNCTIONAL BLOCK DIAGRAMS

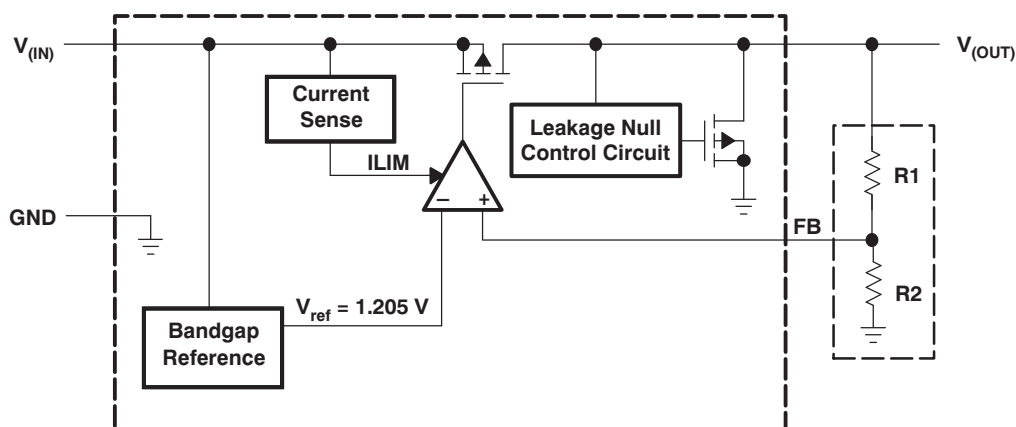


Figure 1. Functional Block Diagram—Adjustable Version

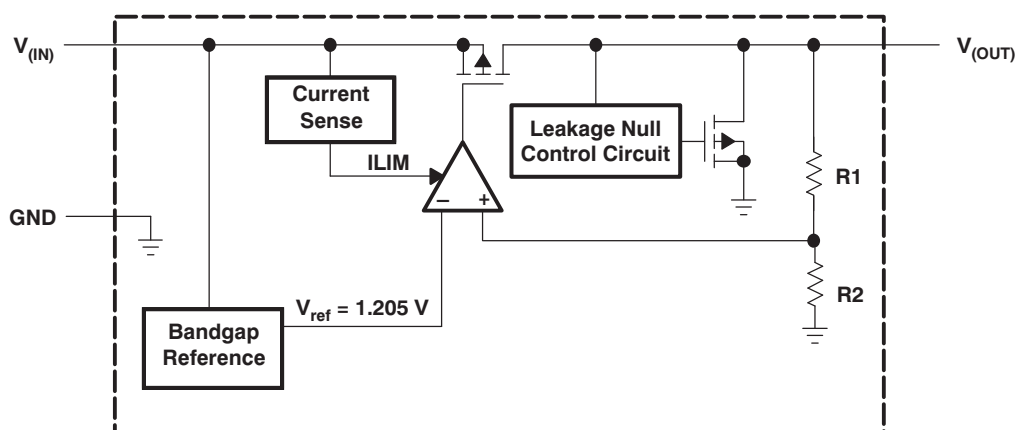


Figure 2. Functional Block Diagram—Fixed Version

Table 1. Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.		
	FIXED	ADJ.	
FB		1	Adjustable version only. This terminal is used to set the output voltage.
NC	1		No connection
GND	2	2	Ground
NC	3	3	No connection
IN	4	4	Input supply.
OUT	5	5	Output of the regulator, any output capacitor $\geq 0.47\text{ }\mu\text{F}$ can be used for stability.

TYPICAL CHARACTERISTICS

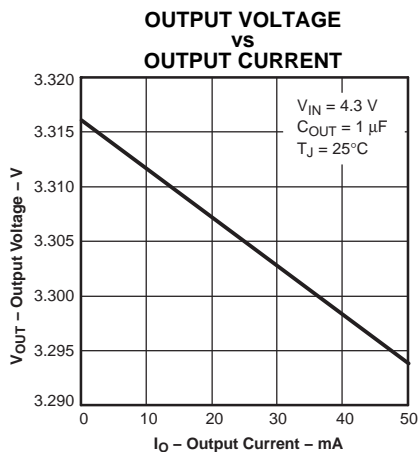


Figure 3.

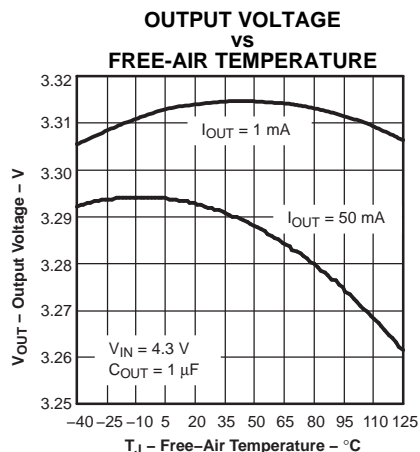


Figure 4.

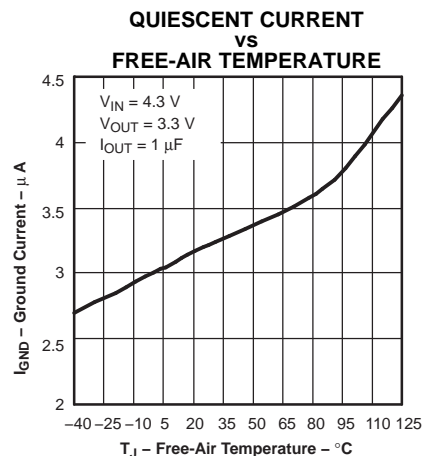


Figure 5.

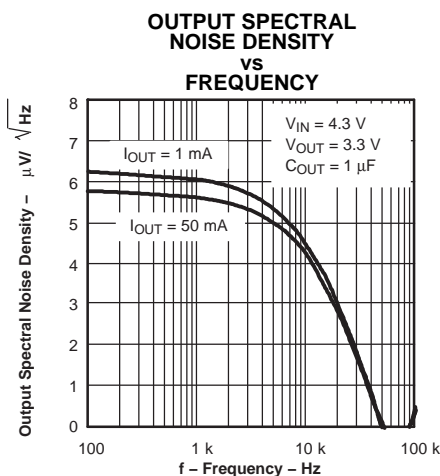


Figure 6.

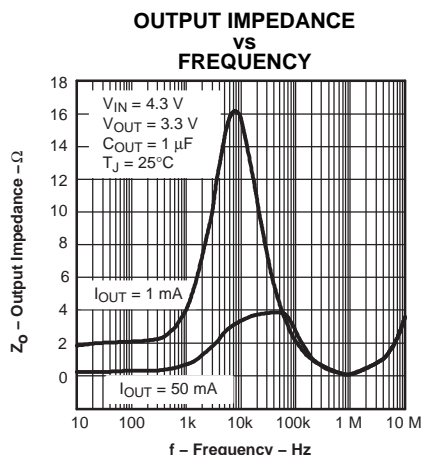


Figure 7.

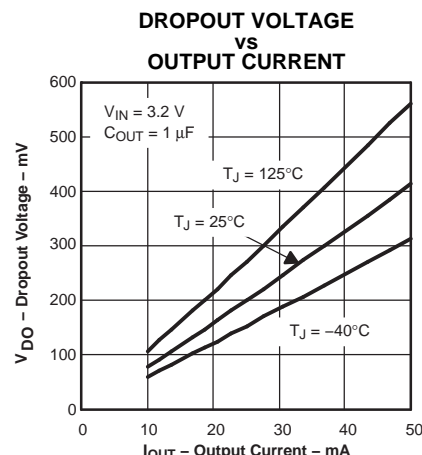


Figure 8.

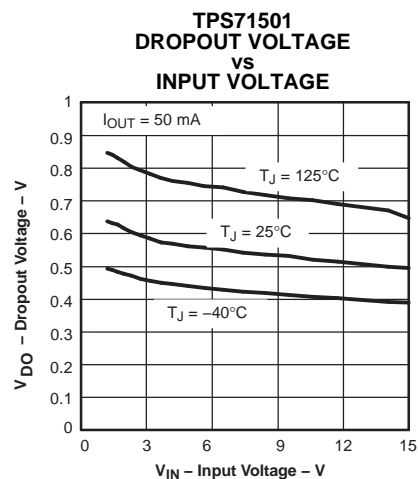


Figure 9.

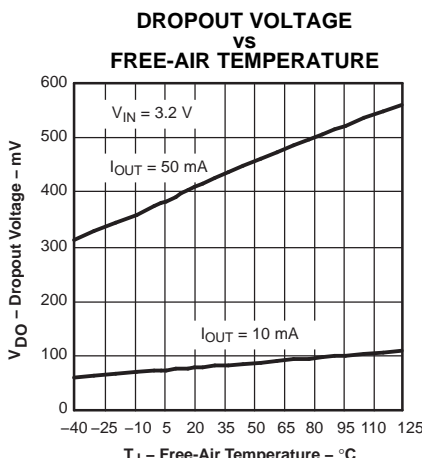


Figure 10.

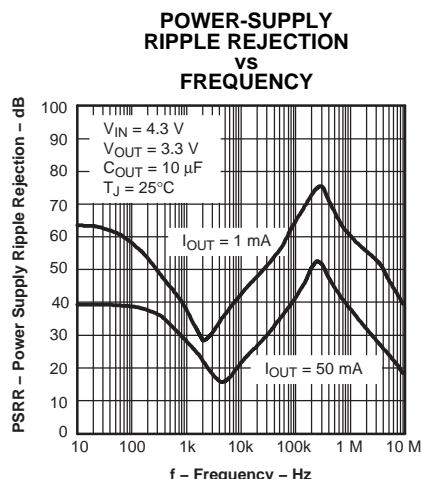


Figure 11.

TYPICAL CHARACTERISTICS (continued)

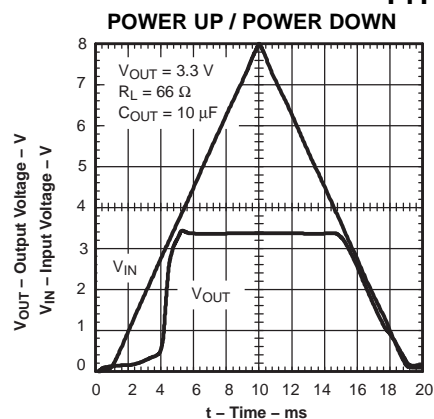


Figure 12.

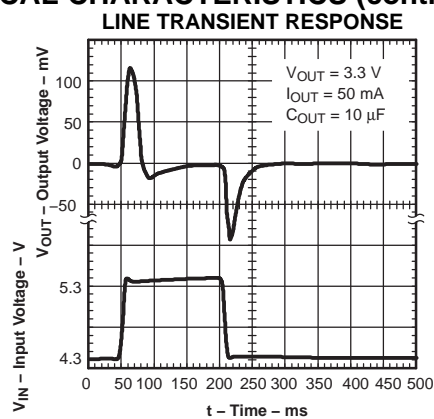


Figure 13.

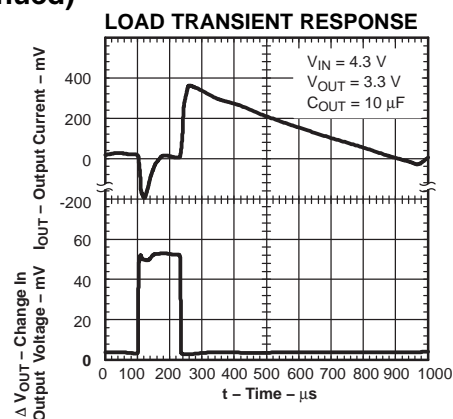


Figure 14.

APPLICATION INFORMATION

The TPS715xx family of LDO regulators has been optimized for ultra-low power applications such as the MSP430 microcontroller. Its ultralow supply current maximizes efficiency at light loads and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

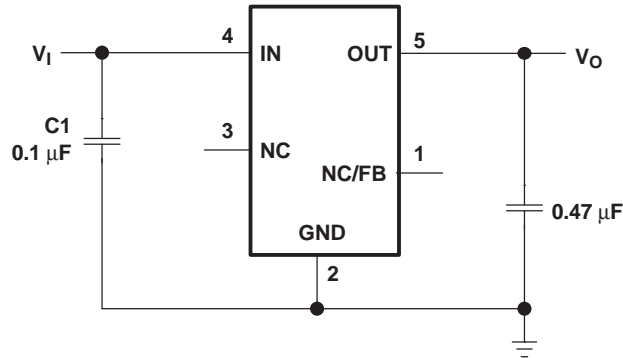


Figure 15. Typical Application Circuit (Fixed Voltage Version)

External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) $\geq 0.47 \mu\text{F}$ properly stabilizes this loop.

Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\text{max})}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\text{max})}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(\text{max})} = \frac{T_{J\text{max}} - T_A}{R_{\theta JA}} \quad (1)$$

where:

$T_{J\text{max}}$ = Maximum allowable junction temperature

$R_{\theta JA}$ = Thermal resistance junction-to-ambient for the package (see the Dissipation Ratings table)

T_A = Ambient temperature

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

Regulator Protection

The TPS715xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS715xx features internal current limiting. During normal operation, the TPS715xx limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

Programming the TPS71501 Adjustable LDO Regulator

The output voltage of the TPS71501 adjustable regulator is programmed using an external resistor divider as shown in [Figure 16](#). The output voltage is calculated using:

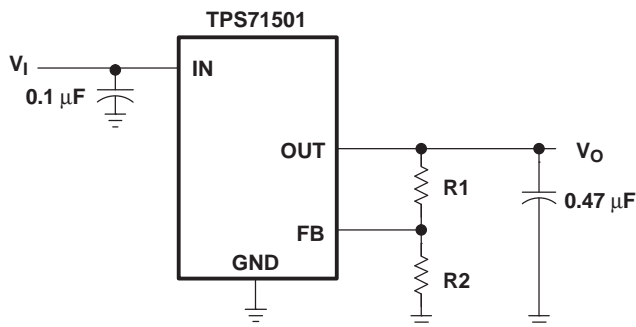
$$V_O = V_{\text{ref}} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where:

$V_{\text{REF}} = 1.205 \text{ V typ}$ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 1.5- μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O . The recommended design procedure is to choose $R2 = 1 \text{ M}\Omega$ to set the divider current at 1.5 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R2 \quad (4)$$



OUTPUT VOLTAGE
PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	0.499 M Ω	1 M Ω
2.8 V	1.33 M Ω	1 M Ω
5 V	3.16 M Ω	1 M Ω

Figure 16. TPS71501 Adjustable LDO Regulator Programming

REVISION HISTORY

Changes from Revision F (August 2011) to Revision G	Page
• Added Grade 1 and HBM and CDM classification to features list	1
• Added ESD classifications for HBM and CDM models in <i>ABSOLUTE MAXIMUM RATINGS</i> table	2
• Changed CDM absolute maximum value from 500 to 750	2
• Added additional test condition to Output current limit in <i>ELECTRICAL CHARACTERISTICS</i> table, and added V_{IN} value to condition to differentiate conditions	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS71501QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANS	Samples
TPS71525QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANU	Samples
TPS71530QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANV	Samples
TPS71533QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANW	Samples
TPS71550QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANX	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS71501-Q1, TPS71525-Q1, TPS71530-Q1, TPS71533-Q1, TPS71550-Q1 :

- Catalog: [TPS71501](#), [TPS71525](#), [TPS71530](#), [TPS71533](#), [TPS71550](#)
- Enhanced Product: [TPS71501-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71501QDCKRQ1	SC70	DCR	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71525QDCKRQ1	SC70	DCR	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71533QDCKRQ1	SC70	DCR	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71501QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71525QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0
TPS71533QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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