2-A, Fast-Transient, Low-Dropout Voltage Regulator

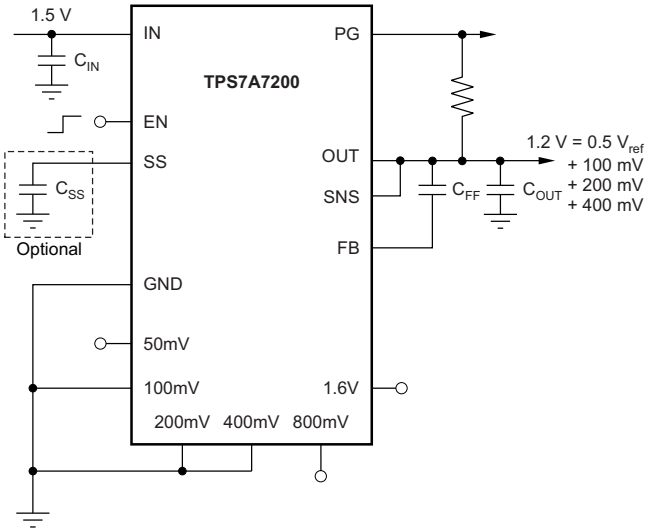
Check for Samples: TPS7A7200

FEATURES

- **Low Dropout Voltage: 180 mV at 2 A**
- **V_{IN} Range: 1.5 V to 6.5 V**
- **Configurable Fixed V_{OUT} Range: 0.9 V to 3.5 V Adjustable V_{OUT} Range: 0.9 V to 5.0 V**
- **Very Good Load and Line Transient Response**
- **Stable with Ceramic Output Capacitor**
- **1.5% Accuracy over Line, Load, and Temperature**
- **Programmable Softstart**
- **Power Good (PG) Output**
- **3-mm × 3-mm QFN-16 and 5-mm × 5-mm QFN-20 Packages**

APPLICATIONS

- **Wireless Infrastructure: SerDes, FPGA, DSP™**
- **RF Components: VCO, ADC, DAC, LVDS**
- **Set-Top Boxes: Amplifier, ADC, DAC, FPGA, DSP**
- **Wireless LAN, Bluetooth®**
- **PCs and Printers**
- **Audio and Visual**



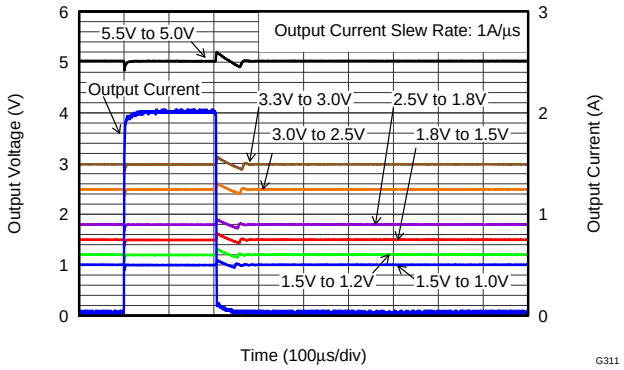
Typical Application

DESCRIPTION

The TPS7A7200 low-dropout (LDO) voltage regulator is designed for applications seeking very-low dropout capability (180 mV at 2 A) with an input voltage from 1.5 V to 6.5 V. The TPS7A7200 offers an innovative, user-configurable, output-voltage setting from 0.9 V to 3.5 V, eliminating external resistors and any associated error.

The TPS7A7200 has very fast load-transient response, is stable with ceramic output capacitors, and supports a better than 2% accuracy over line, load, and temperature. A soft-start pin allows for an application to reduce inrush into the load. Additionally, an open-drain, power-good signal allows for sequencing power rails.

The TPS7A7200 is available in 3-mm × 3-mm, 16-pin QFN and 5-mm × 5-mm, 20-pin QFN packages.



Load Transient Response with Seven Different Results: 1.5 V_{IN} to 1.0 V_{OUT}, 1.5 V_{IN} to 1.2 V_{OUT}, 1.8 V_{IN} to 1.5 V_{OUT}, 2.5 V_{IN} to 1.8 V_{OUT}, 3.0 V_{IN} to 2.5 V_{OUT}, 3.3 V_{IN} to 3.0 V_{OUT}, and 5.5 V_{IN} to 5.0 V_{OUT}

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	Description
TPS7A7200**yyyz**	**YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN, PG, EN	–0.3	+7.0	V
	SS, FB, SNS, OUT	–0.3	V_{IN} + 0.3(2)	V
	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	–0.3	V_{OUT} + 0.3	V
Current	OUT	Internally limited		A
	PG (sink current into IC)		5	mA
Temperature	Operating virtual junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating(3)	Human body model (HBM, JESD22-A114A)		2	kV
	Charged device model (CDM, JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or +7.0 V, whichever is smaller.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC[1][2]		TPS7A7200[3]		UNITS
		RGW (QFN)	RGT (QFN)	
		20 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[4]	35.7	44.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[5]	33.6	54.3	
θ_{JB}	Junction-to-board thermal resistance[6]	15.2	17.2	
ψ_{JT}	Junction-to-top characterization parameter[7]	0.4	1.1	
ψ_{JB}	Junction-to-board characterization parameter[8]	15.4	17.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[9]	3.8	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on printed circuit board (PCB) copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW package is derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. RGW: The exposed pad is connected to the PCB ground layer through a 4 × 4 thermal via array.
ii. RGT: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
(b) i. RGW: Both the top and bottom copper layers have a dedicated pattern for 4% copper coverage.
ii .RGT: Both the top and bottom copper layers have a dedicated pattern for 5% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inch × 3-inch copper area. To understand the effects of the copper area on thermal performance, refer to the *Power Dissipation* and *Estimating Junction Temperature* sections.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

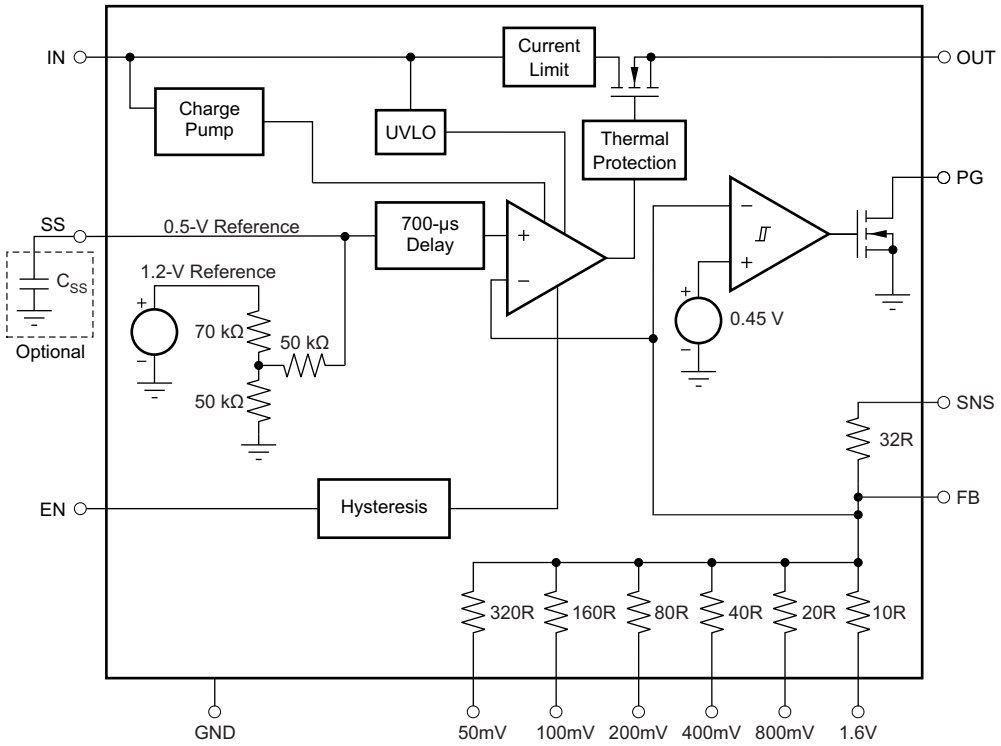
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), 1.425 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V or V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.5 V(1)(2), OUT connected to 50 Ω to GND(3),V_{EN} = 1.1 V, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{FF} = 0 pF (RGW package), C_{FF} = 220 pF (RGT package)(4), and PG pin pulled up to V_{IN} with 100 kΩ, 27 kΩ ≤ R2 ≤ 33 kΩ for adjustable configuration(5), unless otherwise noted.
Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.425		6.5	V
$V_{(SS)}$	SS pin voltage			0.5		V
V_{OUT}	Output voltage range	Adjustable with external feedback resistors	0.9		5.0	V
		Fixed with voltage setting pins	0.9		3.5	
	Output voltage accuracy(6)(7)	RGT package only, adjustable, –40°C ≤ T_A ≤ +85°C, 25 mA ≤ I_{OUT} ≤ 2 A	–1.5		+1.5	%
		RGT package only, fixed, –40°C ≤ T_A ≤ +85°C, 25 mA ≤ I_{OUT} ≤ 2 A	–2.0		+2.0	
		Adjustable, 25 mA ≤ I_{OUT} ≤ 2 A	–2.0		+2.0	
		Fixed, 25 mA ≤ I_{OUT} ≤ 2 A	–3.0		+3.0	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 25 mA		0.01		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	25 mA ≤ I_{OUT} ≤ 2 A		0.1		%/A
$V_{(DO)}$	Dropout voltage (8)	V_{OUT} ≤ 3.3 V, I_{OUT} = 2 A, $V_{(FB)}$ = GND			180	mV
		3.3 V < V_{OUT}, I_{OUT} = 2 A, $V_{(FB)}$ = GND			470	mV
$I_{(LIM)}$	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = 3.3 V, $V_{OUT(TARGET)}$ = 0.9 V	2.4	3.1		A
$I_{(GND)}$	GND pin current	Full load, I_{OUT} = 2 A		2.6		mA
		Minimum load, V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.9 V, I_{OUT} = 25 mA			4	mA
		Shutdown, PG = (open), V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.9 V, $V_{(EN)}$ < 0.5 V		0.1	5	µA
$I_{(EN)}$	EN pin current	V_{IN} = 6.5 V, $V_{(EN)}$ = 0 V and 6.5 V			±0.1	µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)		0		0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1		6.5	V
$V_{IT(PG)}$	PG pin threshold	For the direction PG↓ with decreasing V_{OUT}	0.85V_{OUT}	0.9V_{OUT}	0.96V_{OUT}	V
$V_{hys(PG)}$	PG pin hysteresis	For PG↑		0.02V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, $V_{(PG)}$ = 6.5 V			1	µA
$I_{(SS)}$	SS pin charging current	$V_{(SS)}$ = GND, V_{IN} = 3.3 V	3.5	5.1	7.2	µA
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A		40.65		μV_{RMS}
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature		–40		+125	°C

(1) When V_{OUT} ≤ 3.5 V, V_{IN} ≥ (V_{OUT} + 0.3 V) or 1.425 V, whichever is greater; when V_{OUT} > 3.5 V, V_{IN} ≥ (V_{OUT} + 0.5 V).
(2) $V_{OUT(TARGET)}$ is the calculated target V_{OUT} value from the output voltage setting pins: 50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V in fixed configuration, or the expected V_{OUT} value set by external feedback resistors in adjustable configuration.
(3) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(4) C_{FF} is the capacitor between FB pin and OUT
(5) R2 is the bottom-side of the feedback resistor between the FB pin and OUT. See Figure 40 for details.
(6) When the TPS7A7200 is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(7) The TPS7A7200 is not tested at V_{OUT} = 0.9 V, 2.7 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 2 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package.
(8) $V_{(DO)}$ is not defined for output voltage settings below 1.2 V.

FUNCTIONAL BLOCK DIAGRAM

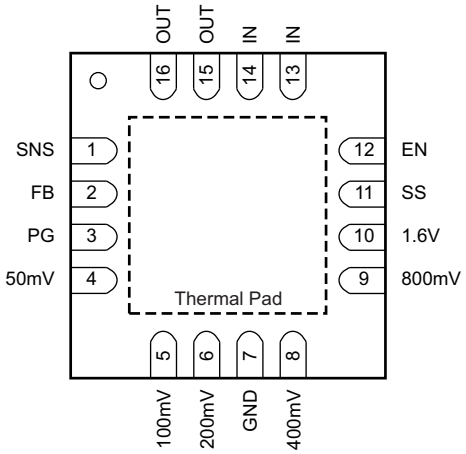


NOTE: 320R = 1.024 MΩ (that is, 1R = 3.2 kΩ).

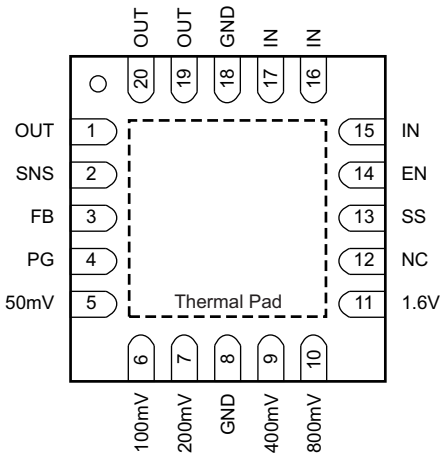
Figure 1. Functional Block Diagram

PIN CONFIGURATIONS

RGT PACKAGE
3-mm × 3-mm QFN-16
(TOP VIEW)



RGW PACKAGE
5-mm × 5-mm QFN-20
(TOP VIEW)



PIN DESCRIPTIONS

NAME	RGW	RGT	DESCRIPTION
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	5, 6, 7, 9, 10, 11	4, 5, 6, 8, 9, 10	Output voltage setting pins. These pins should be connected to ground or left floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the *USER-CONFIGURABLE OUTPUT VOLTAGE* section for more details.
EN	14	12	Enable pin. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. See the *ENABLE AND SHUTDOWN THE DEVICE* section for more details.
FB	3	2	Output voltage feedback pin. Connected to the error amplifier. See the *USER-CONFIGURABLE OUTPUT VOLTAGE* and *TRADITIONAL ADJUSTABLE CONFIGURATION* sections for more details. A 220-pF ceramic capacitor from FB pin to OUT is highly recommended.
GND	8, 18	7	Ground pin.
IN	15, 16, 17	13, 14	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin. See INPUT CAPACITOR REQUIREMENTS for more details.
NC	12	—	Not internally connected. The NC pin is not connected to any electrical node. It is strongly recommended to connect this pin and the thermal pad to a large-area ground plane. See the *Power Dissipation* section for more details.
OUT	1, 19, 20	15, 16	Regulated output pin. A 4.7-µF or larger capacitance is required for stability. See OUTPUT CAPACITOR REQUIREMENTS for more details.
PG	4	3	Active-high power good pin. An open-drain output that indicates when the output voltage reaches 90% of the target. See POWER GOOD for more details.
SNS	2	1	Output voltage sense input pin. See the *USER-CONFIGURABLE OUTPUT VOLTAGE* and *TRADITIONAL ADJUSTABLE CONFIGURATION* sections for more details.
SS	13	11	Soft-start pin. Leaving this pin open provides soft-start of the default setting. Connecting an external capacitor between this pin and the ground enables the soft-start function by forming an RC-delay circuit in combination with the integrated resistance on the silicon. See the *SOFT-START* section for more details.
Thermal Pad			It is strongly recommended to connect the thermal pad to a large-area ground plane. If available, connect an electrically-floating, dedicated thermal plane to the thermal pad as well.

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pull-up resistor, unless otherwise noted.

LOAD REGULATION (0.9 V, Adjustable)

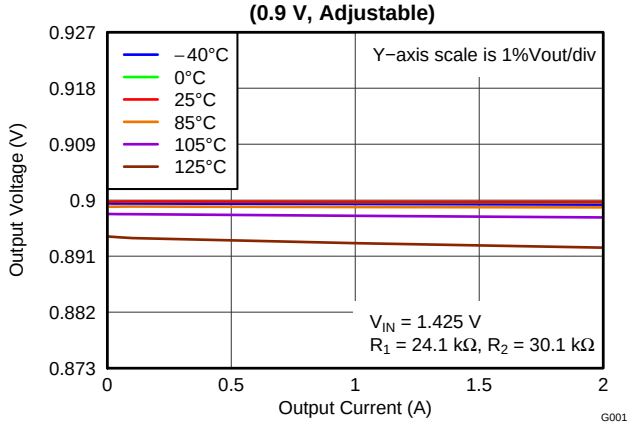


Figure 2.

LOAD REGULATION (5.0 V, Adjustable)

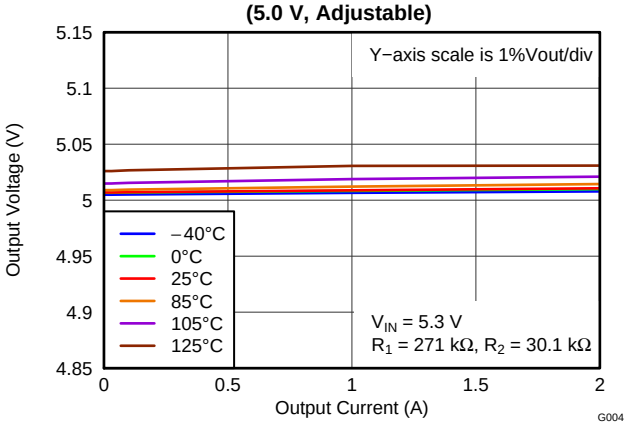


Figure 3.

LOAD REGULATION (0.9 V, Fixed by Setting Pins)

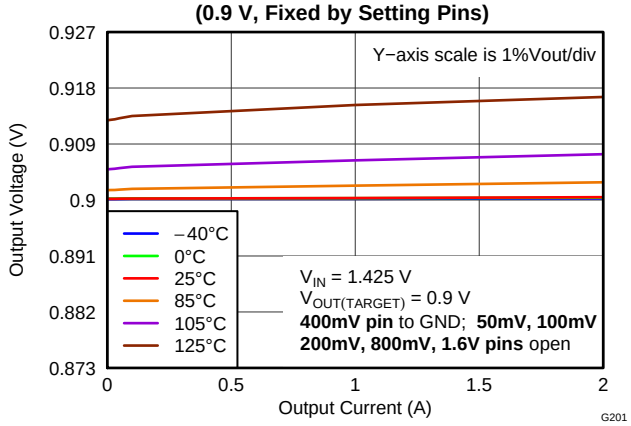


Figure 4.

LOAD REGULATION (3.5 V, Fixed by Setting Pins)

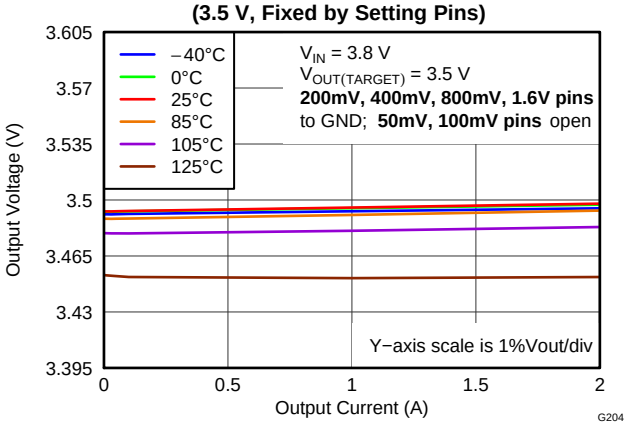


Figure 5.

DROPOUT VOLTAGE vs OUTPUT CURRENT

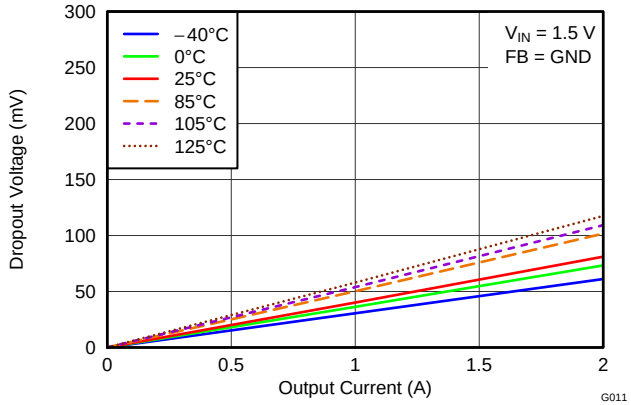


Figure 6.

DROPOUT VOLTAGE vs TEMPERATURE

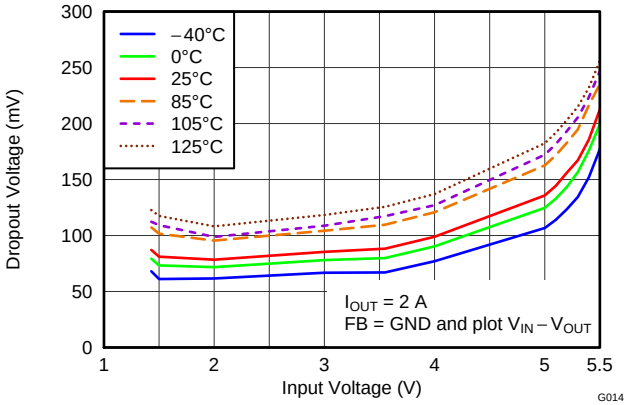


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pull-up resistor, unless otherwise noted.

LINE REGULATION (0.9 V, Adjustable)

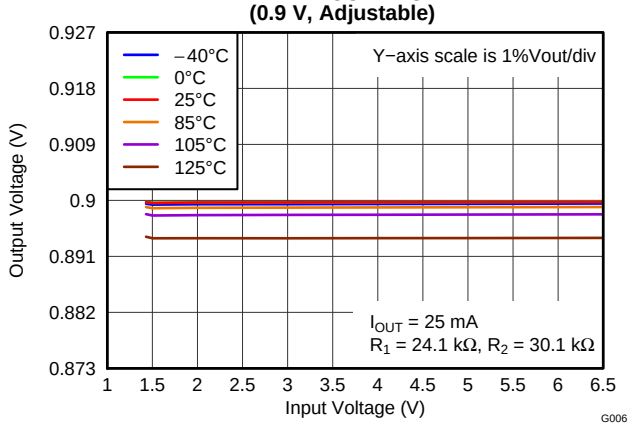


Figure 8.

LINE REGULATION (5.0 V, Adjustable)

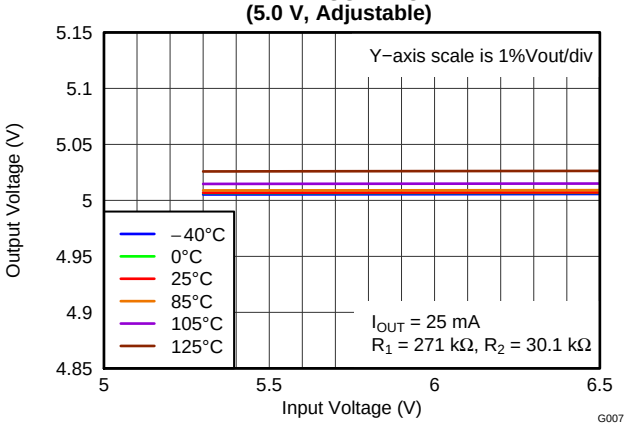


Figure 9.

LINE REGULATION (0.9 V, Fixed by Setting Pins)

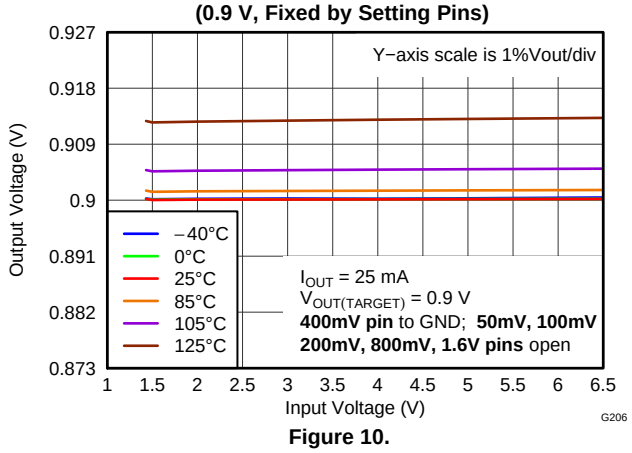


Figure 10.

LINE REGULATION (3.5 V, Fixed by Setting Pins)

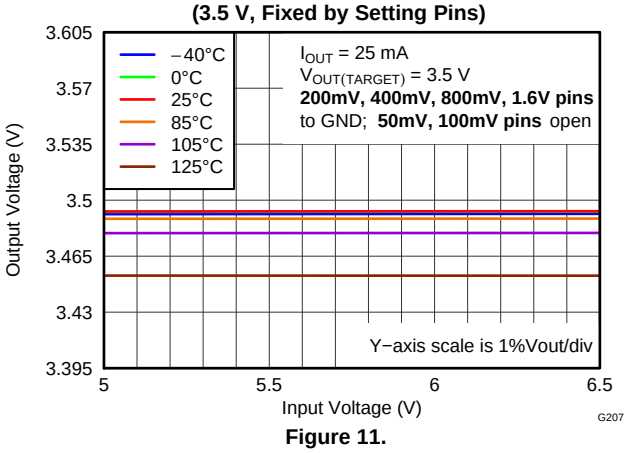


Figure 11.

OUTPUT VOLTAGE: ACTUAL vs PIN-SETTING

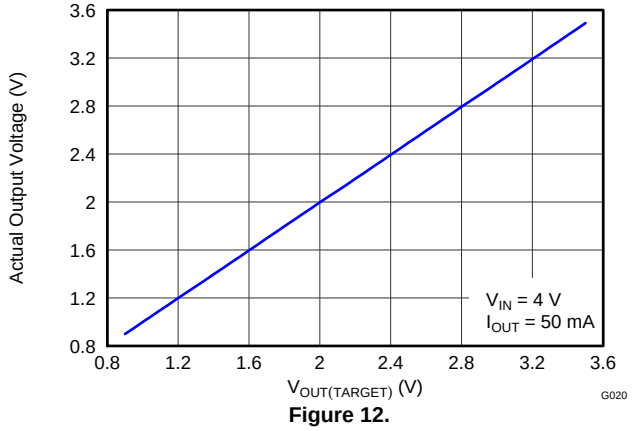


Figure 12.

OUTPUT VOLTAGE: ACTUAL (Normalized) vs PIN-SETTING

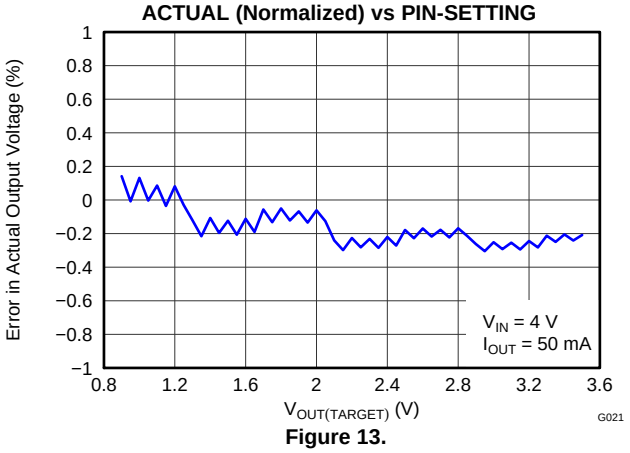


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pull-up resistor, unless otherwise noted.

GND PIN CURRENT vs OUTPUT CURRENT

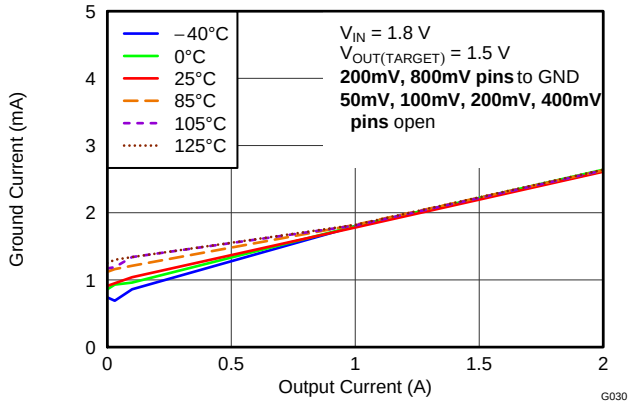


Figure 14.

GND PIN CURRENT vs INPUT VOLTAGE

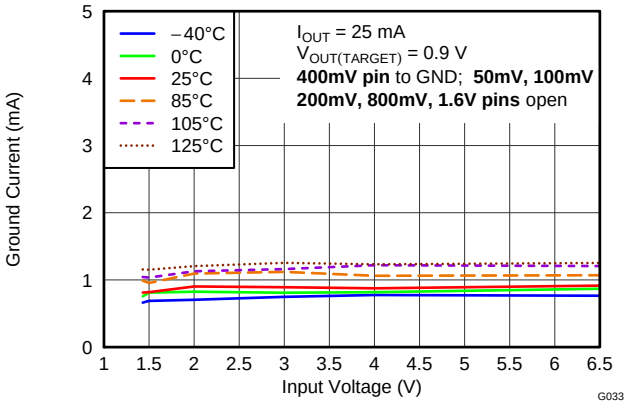


Figure 15.

GND PIN CURRENT IN SHUTDOWN vs TEMPERATURE

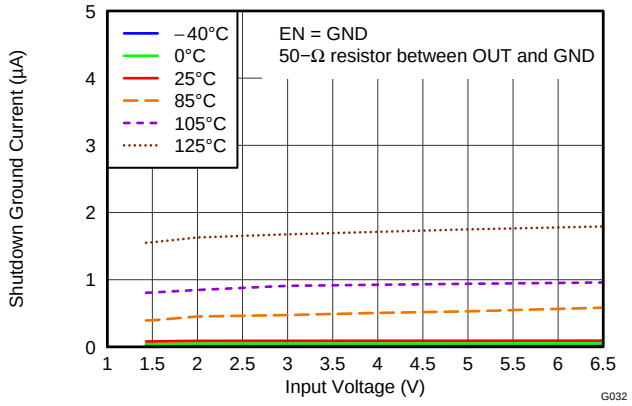


Figure 16.

CURRENT LIMIT vs OUTPUT VOLTAGE (Foldback)

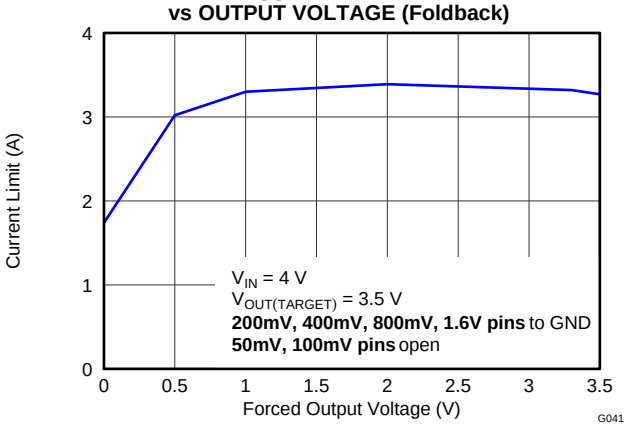


Figure 17.

POWER-GOOD THRESHOLD VOLTAGE vs TEMPERATURE

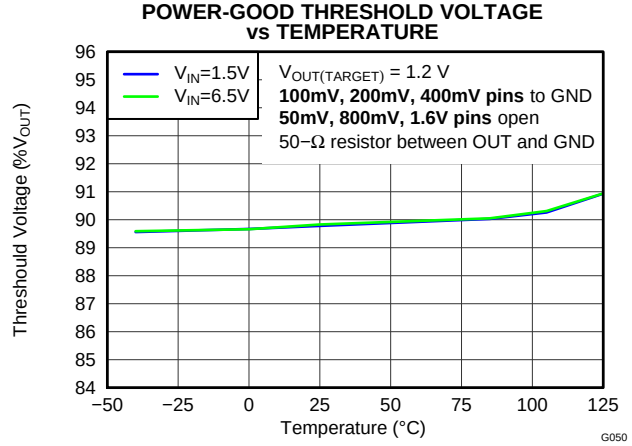


Figure 18.

POWER-GOOD PIN DRIVE CAPABILITY

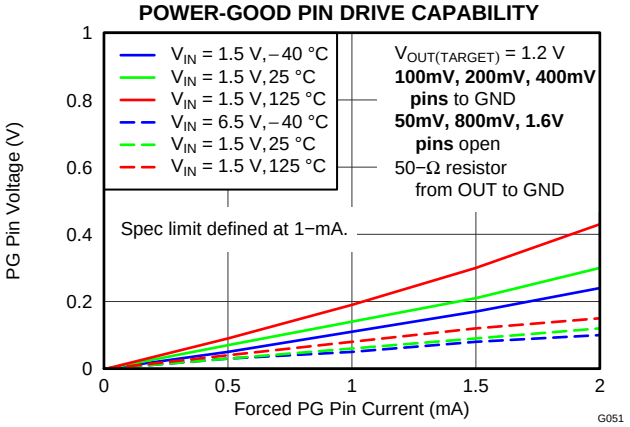


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pull-up resistor, unless otherwise noted.

NOISE SPECTRAL DENSITY BY OUTPUT VOLTAGE

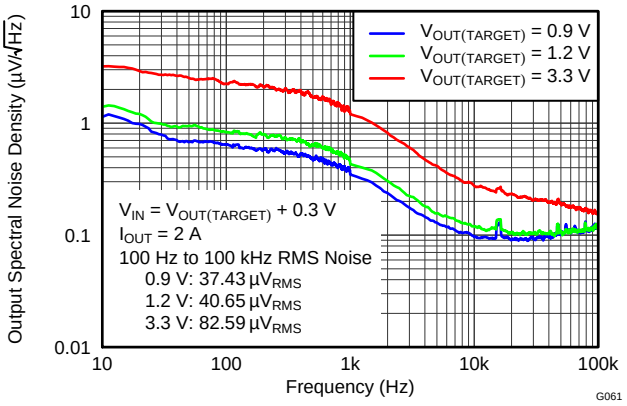


Figure 20.

NOISE SPECTRAL DENSITY BY EXTERNAL CAPACITORS

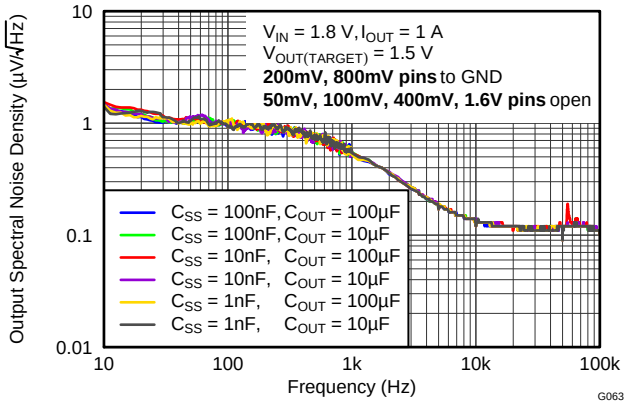


Figure 21.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

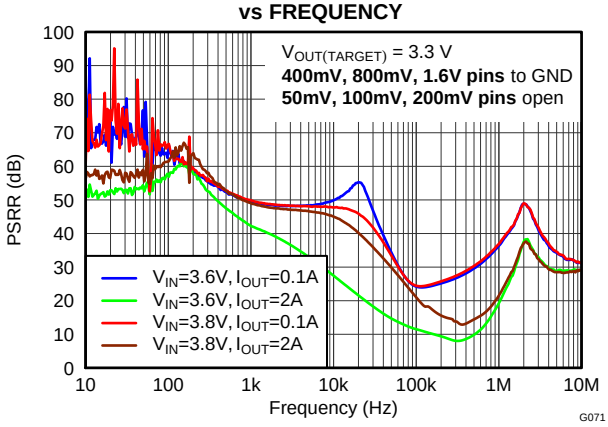


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pull-up resistor, unless otherwise noted.

LOAD TRANSIENT RESPONSE (V_{OUT} = 1.2 V)

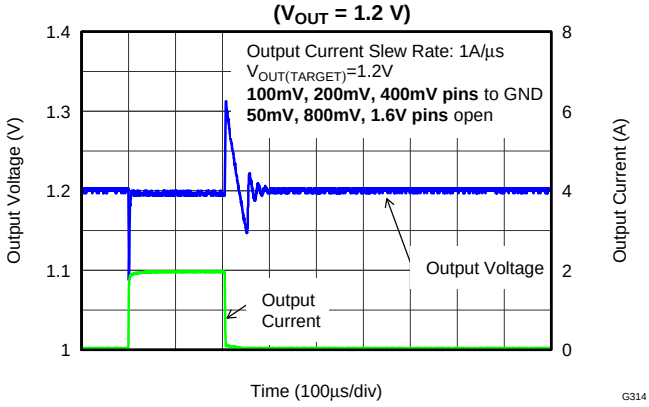


Figure 23.

LOAD TRANSIENT RESPONSE (V_{OUT} = 3.3 V)

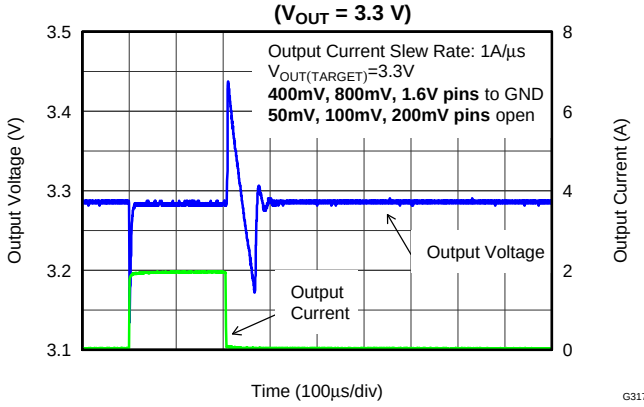


Figure 24.

LINE TRANSIENT RESPONSE

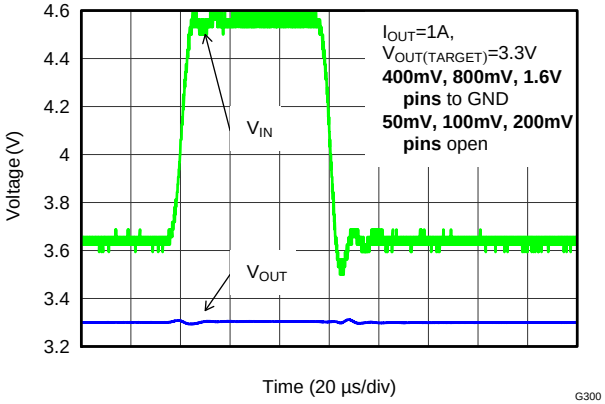


Figure 25.

POWER-UP/POWER-DOWN (IN = EN)

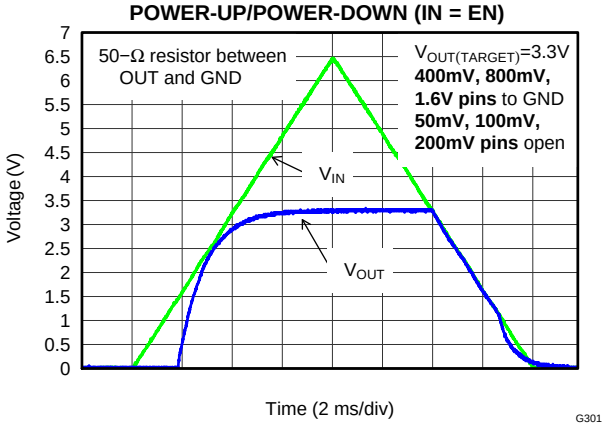


Figure 26.

TURN-ON RESPONSE (IN = EN)

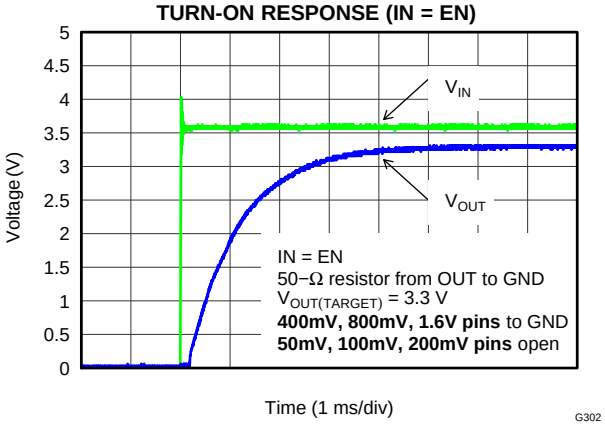


Figure 27.

TURN-OFF RESPONSE (IN = EN)

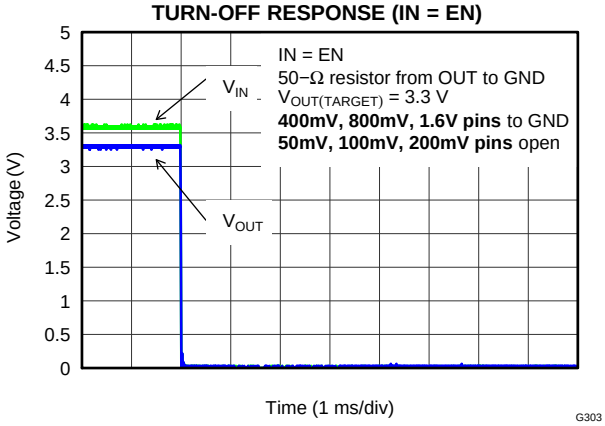


Figure 28.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with 100-kΩ pull-up resistor, unless otherwise noted.

EN PULSE ON RESPONSE (Over Stable V_{IN})

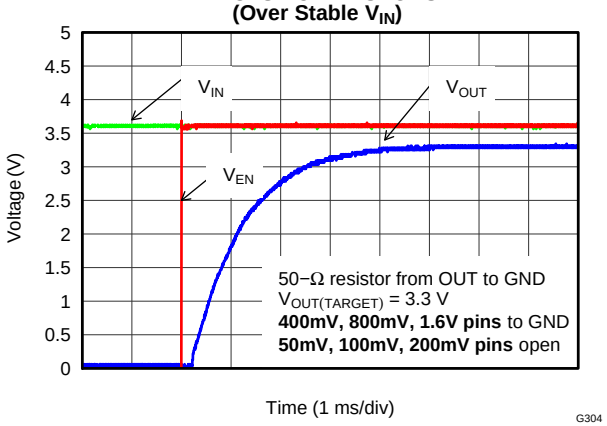


Figure 29.

EN PULSE OFF RESPONSE (Over Stable V_{IN})

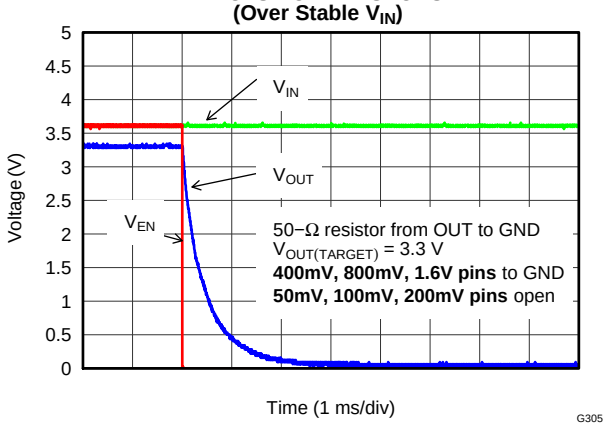


Figure 30.

SOFT-START DELAY vs C_{SS} (Enlarged View)

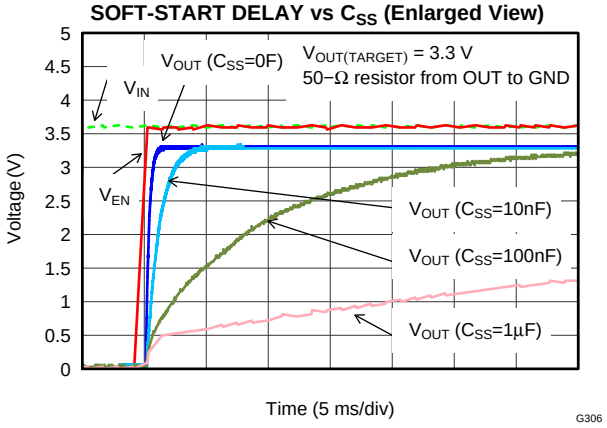


Figure 31.

SOFT-START DELAY vs C_{SS} (Reduced View)

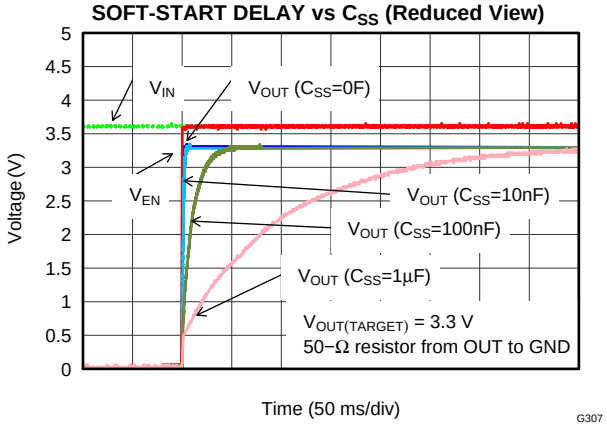


Figure 32.

SOFT-START DELAY vs C_{SS}

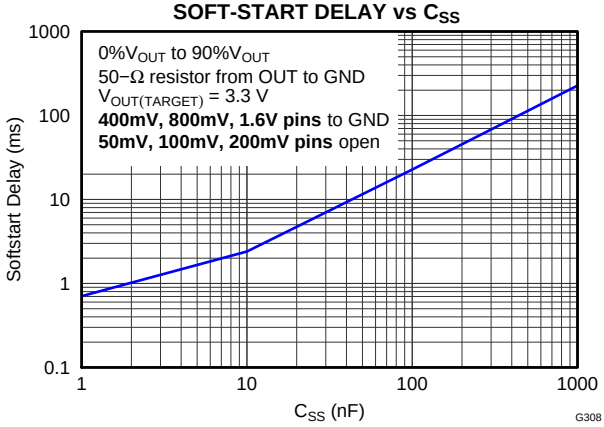


Figure 33.

APPLICATION INFORMATION

OVERVIEW

The TPS7A7200 belongs to a family of new-generation LDO regulators that uses innovative circuitry to offer very-low dropout voltage along with the flexibility of a programmable output voltage.

The dropout voltage for this LDO regulator family is 0.18 V at 2 A. This voltage is ideal for making the TPS7A7200 into a point-of-load (POL) regulator because 0.18 V at 2 A is lower than any voltage gap among the most common voltage rails: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, and 3.3 V. This device offers a fully user-configurable output voltage setting method. The TPS7A7200 output voltage can be programmed to any target value from 0.9 V to 3.5 V in 50-mV steps.

Another big advantage of using the TPS7A7200 is the wide range of available operating input voltages: from 1.5 V to 6.5 V. The TPS7A7200 also has very good line and load transient response. All these features allow the TPS7A7200 to meet most voltage-regulator needs for under-6-V applications, using only one device so that less time is spent on inventory control.

Texas Instruments also offers different output current ratings with other family devices: the TPS7A7100 (1 A) and TPS7A7300 (3 A).

USER-CONFIGURABLE OUTPUT VOLTAGE

Unlike traditional LDO devices, the TPS7A7200 comes with only one orderable part number; there is no adjustable or fixed output voltage option. The output voltage of the TPS7A7200 is selectable in accordance with the names given to the output voltage setting pins: 50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V. For each pin connected to the ground, the output voltage setting increases by the value associated with that pin name, starting from the value of the reference voltage of 0.5 V; floating the pin(s) has no effect on the output voltage. Figure 34 through Figure 39 show examples of how to program the output voltages.

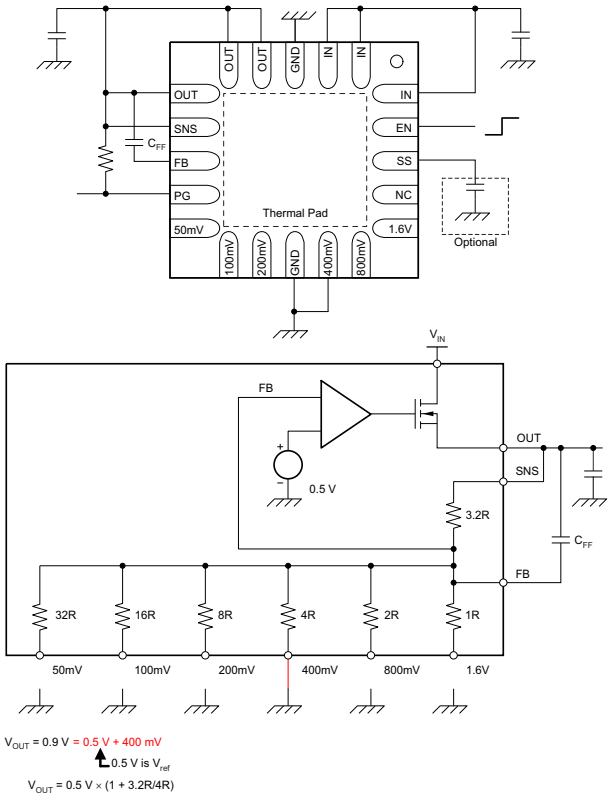


Figure 34. 0.9-V Configuration

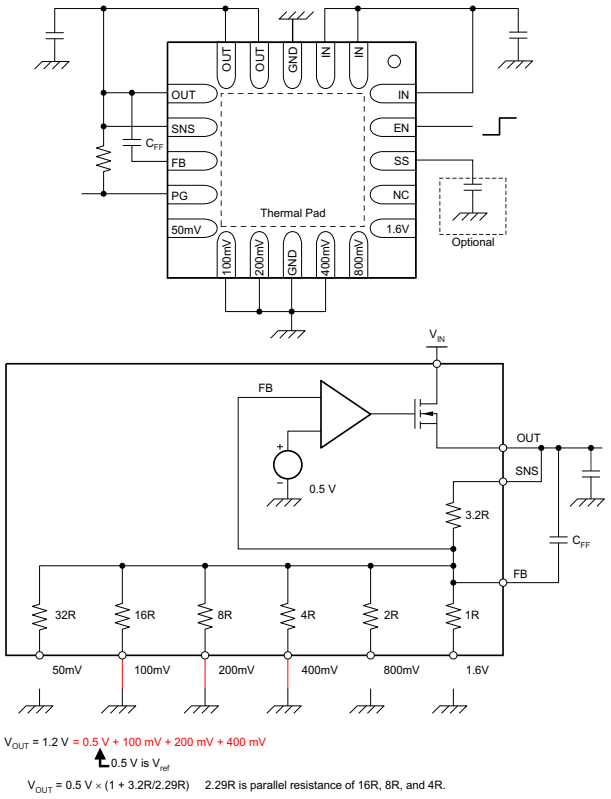
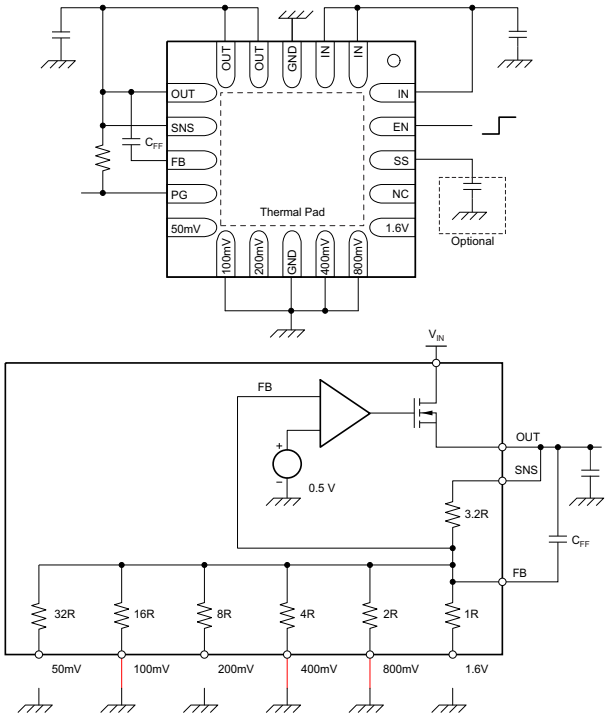


Figure 35. 1.2-V Configuration

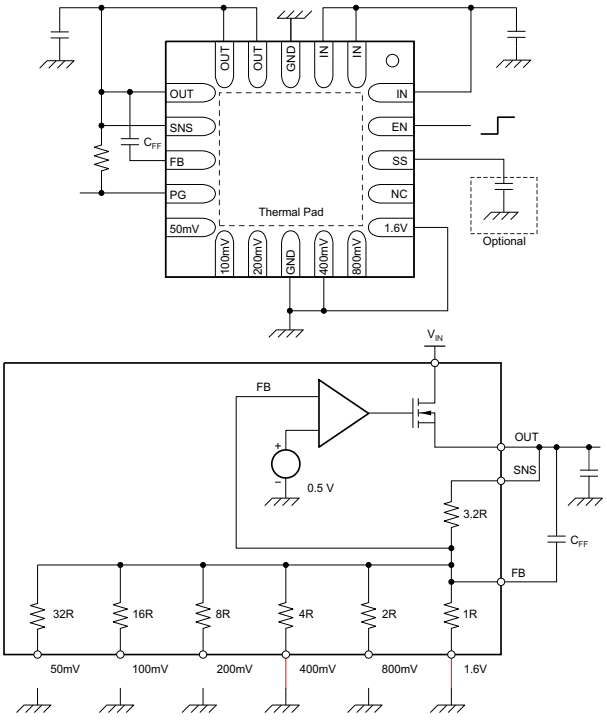


V_{OUT} = 1.8 V = 0.5 V + 100 mV + 400 mV + 800 mV

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/1.23R)$ 1.23R is parallel resistance of 16R, 4R, and 2R.

Figure 36. 1.8-V Configuration

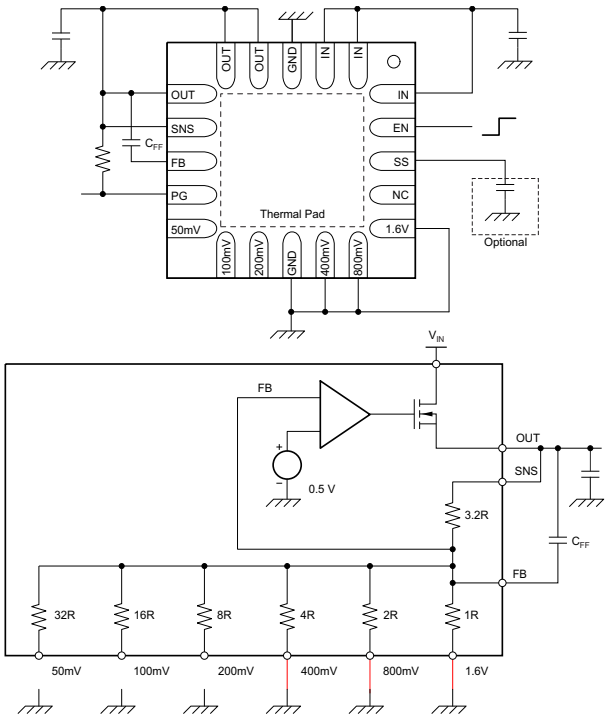


V_{OUT} = 2.5 V = 0.5 V + 400 mV + 1.6 V

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/0.8R)$ 0.8R is parallel resistance of 4R and 1R.

Figure 37. 2.5-V Configuration

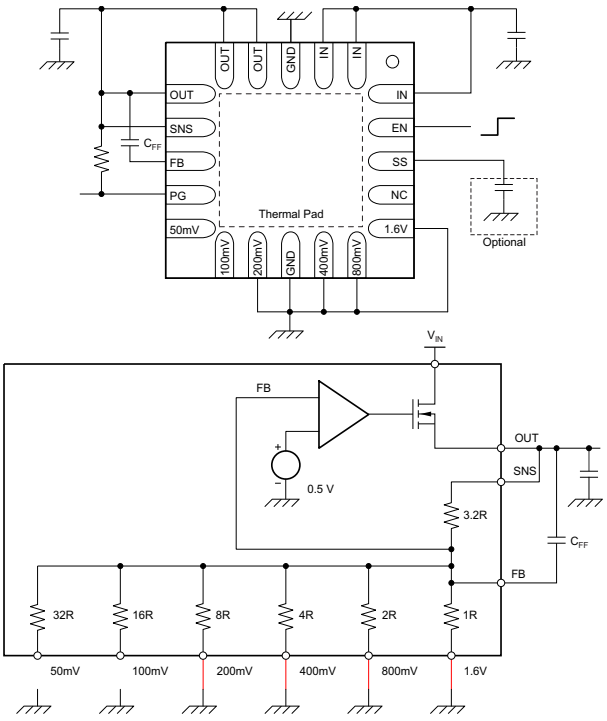


V_{OUT} = 3.3 V = 0.5 V + 400 mV + 800 mV + 1.6 V

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/0.571R)$ 0.571R is parallel resistance of 4R, 2R, and 1R.

Figure 38. 3.3-V Configuration



V_{OUT} = 3.5 V = 0.5 V + 200 mV + 400 mV + 800 mV + 1.6 V

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/0.533R)$ 0.533R is parallel resistance of 8R, 4R, 2R, and 1R.

Figure 39. 3.5-V Configuration

See Table 1 for a full list of target output voltages and corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.9 V to 3.5 V in 50-mV steps.

Figure 12 and Figure 13 shows this output voltage programming performance.

NOTE

Any output voltage setting that is not listed in Table 1 is not covered in the Electrical Characteristics. For output voltages greater than 3.5 V, use a traditional adjustable configuration (see the TRADITIONAL ADJUSTABLE CONFIGURATION section).

Table 1. User Configurable Output Voltage Setting

$V_{OUT(TARGET)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V	$V_{OUT(TARGET)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.90	open	open	open	GND	open	open	2.25	GND	GND	open	open	open	GND
0.95	GND	open	open	GND	open	open	2.30	open	open	GND	open	open	GND
1.00	open	GND	open	GND	open	open	2.35	GND	open	GND	open	open	GND
1.05	GND	GND	open	GND	open	open	2.40	open	GND	GND	open	open	GND
1.10	open	open	GND	GND	open	open	2.45	GND	GND	GND	open	open	GND
1.15	GND	open	GND	GND	open	open	2.50	open	open	open	GND	open	GND
1.20	open	GND	GND	GND	open	open	2.55	GND	open	open	GND	open	GND
1.25	GND	GND	GND	GND	open	open	2.60	open	GND	open	GND	open	GND
1.30	open	open	open	open	GND	open	2.65	GND	GND	open	GND	open	GND
1.35	GND	open	open	open	GND	open	2.70	open	open	GND	GND	open	GND
1.40	open	GND	open	open	GND	open	2.75	GND	open	GND	GND	open	GND
1.45	GND	GND	open	open	GND	open	2.80	open	GND	GND	GND	open	GND
1.50	open	open	GND	open	GND	open	2.85	GND	GND	GND	GND	open	GND
1.55	GND	open	GND	open	GND	open	2.90	open	open	open	open	GND	GND
1.60	open	GND	GND	open	GND	open	2.95	GND	open	open	open	GND	GND
1.65	GND	GND	GND	open	GND	open	3.00	open	GND	open	open	GND	GND
1.70	open	open	open	GND	GND	open	3.05	GND	GND	open	open	GND	GND
1.75	GND	open	open	GND	GND	open	3.10	open	open	GND	open	GND	GND
1.80	open	GND	open	GND	GND	open	3.15	GND	open	GND	open	GND	GND
1.85	GND	GND	open	GND	GND	open	3.20	open	GND	GND	open	GND	GND
1.90	open	open	GND	GND	GND	open	3.25	GND	GND	GND	open	GND	GND
1.95	GND	open	GND	GND	GND	open	3.30	open	open	open	GND	GND	GND
2.00	open	GND	GND	GND	GND	open	3.35	GND	open	open	GND	GND	GND
2.05	GND	GND	GND	GND	GND	open	3.40	open	GND	open	GND	GND	GND
2.10	open	open	open	open	open	GND	3.45	GND	GND	open	GND	GND	GND
2.15	GND	open	open	open	open	GND	3.50	open	open	GND	GND	GND	GND
2.20	open	GND	open	open	open	GND							

TRADITIONAL ADJUSTABLE CONFIGURATION

For any output voltage target that is not supported in the USER-CONFIGURABLE OUTPUT VOLTAGE section, a traditional adjustable configuration with external-feedback resistors can be used with the TPS7A7200. Figure 40 shows how to configure the TPS7A7200 as an adjustable regulator with an equation and Table 2 lists recommended pairs of feedback resistor values.

NOTE

The bottom side of feedback resistor R2 in Figure 40 should be in the range of 27 kΩ to 33 kΩ in order to maintain the specified regulation accuracy.

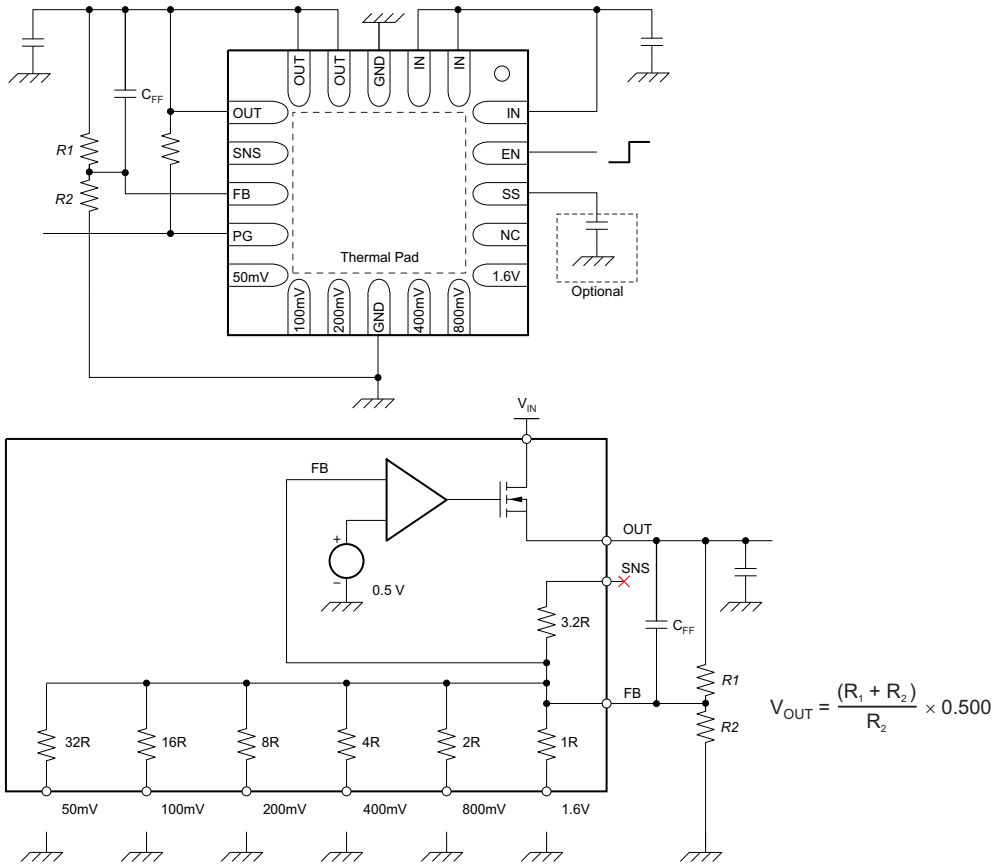


Figure 40. Traditional Adjustable Configuration with External Resistors

Table 2. Recommended Feedback-Resistor Values

$V_{OUT(TARGET)}$ (V)	E96 SERIES		R40 SERIES	
	R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	R2 (kΩ)
1.00	30.1	30.1	30.0	30.0
1.20	39.2	28.0	43.7	31.5
1.50	61.9	30.9	60.0	30.0
1.80	80.6	30.9	80.0	30.7
1.90	86.6	30.9	87.5	31.5
2.50	115	28.7	112	28.0
3.00	147	29.4	150	30.0
3.30	165	29.4	175	31.5
5.00	280	30.9	243	27.2

DROPOUT VOLTAGE

The TPS7A7200 maintains its output voltage regulation with a dropout voltage (V_{IN} – V_{OUT}) greater than 0.18 V under the test conditions specified in the Electrical Characteristics. In most power distribution tree (system) designs, the TPS7A7200 can be used with a 0.3-V difference in the common voltage rails (for example, from 3.3 V_{IN} to 3.0 V_{OUT}, from 1.8 V_{IN} to 1.5 V_{OUT}, or from 1.5 V_{IN} to 1.2 V_{IN}).

INPUT CAPACITOR REQUIREMENTS

As a result of its very fast transient response and low-dropout operation support, it is necessary to reduce the line impedance at the input pin of the TPS7A7200. The line impedance depends heavily on various factors, such as wire (PCB trace) resistance, wire inductance, and/or output impedance of the upstream voltage supply (power supply to the TPS7A7200). Therefore, a specific value for the input capacitance cannot be recommended until the previously listed factors are finalized.

In addition, simple usage of large input capacitance is known to form unwanted LC resonance in combination with input wire inductance. For example, a 5-nH inductor and a 10-µF input capacitor form an LC filter that has a resonance at 712 kHz. This value of 712 kHz is well inside the bandwidth of the TPS7A7200 control loop.

The best guideline is to use a capacitor of up to 1 µF with well-designed wire connections (PCB layout) to the upstream supply. In case it is difficult to optimize the input line, use a large tantalum capacitor in combination with a good-quality, low-ESR, 1-µF ceramic capacitor.

OUTPUT CAPACITOR REQUIREMENTS

The TPS7A7200 is designed to be stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF. The TPS7A7200 is evaluated using an X5R-type, 10-µF ceramic capacitor. X5R- and X7R-type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be below 1.0 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS7A7200 uses an undervoltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature that typically ignores undershoot of the input voltage upon the event of device start-up. Still, a poor input line impedance may cause a severe input voltage drop when the device powers on. As explained in the INPUT CAPACITOR REQUIREMENTS section, the input line impedance should be well-designed.

SOFT-START

The TPS7A7200 has a SS pin that provides a soft-start (slow start) function.

By leaving the SS pin open, the TPS7A7200 performes a soft-start by its default setting.

As shown in Figure 1, by connecting a capacitor between the SS pin and the ground, the C_{SS} capacitor forms an RC pair together with the integrated 50-kΩ resistor. The RC pair operates as an RC-delay circuit for the soft-start together with the internal 700-µs delay circuit.

The relationship between C_{SS} and the soft-start time is shown in Figure 31 through Figure 33.

CURRENT LIMIT

The TPS7A7200 internal current limit circuitry protects the regulator during fault conditions. During a current limit event, the output sources a fixed amount of current that is mostly independent of the output voltage. The current limit function is provided as a fail-safe mechanism and is not intended to be used regularly. Do not design any applications to use this current limit function as a part of expected normal operation. Extended periods of current limit operation degrade device reliability.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

ENABLE AND SHUTDOWN THE DEVICE

The EN pin switches the enable and disable (shutdown) states of the TPS7A7200. A logic high input at the EN pin enables the device; a logic low input disables the device. When disabled, the device consumption current is reduced.

POWER GOOD

The TPS7A7200 has a power good function that works with the PG output pin. When the output voltage undershoots the threshold voltage $V_{IT(PG)}$ during normal operation, the PG open-drain output turns from a high-impedance state to a low-impedance state. When the output voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than the PG hysteresis, $V_{hys(PG)}$, the PG open-drain output turns from a low-impedance state to high-impedance state. By connecting a pull-up resistor (usually between OUT and PG), any downstream device can receive an active-high enable logic signal.

When setting the output voltage to less than 1.8 V and using a pull-up resistor between OUT and PG, depending on the downstream device specifications, the downstream device may not accept the PG output as a valid high-level logic voltage. In such cases, put a pull-up resistor between IN and PG, not between OUT and PG.

Figure 19 shows the open-drain output drive capability. The on-resistance of the open-drain transistor is calculated using Figure 19, and is approximately 200 Ω. Any pull-up resistor greater than 10 kΩ works fine for this purpose.

THERMAL INFORMATION

Thermal Protection

The thermal protection feature disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal limit protects the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A7200 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A7200 into thermal shutdown degrades device reliability.

Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.
Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the QFN (RGW or RGT) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 2:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \quad (2)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 41 .

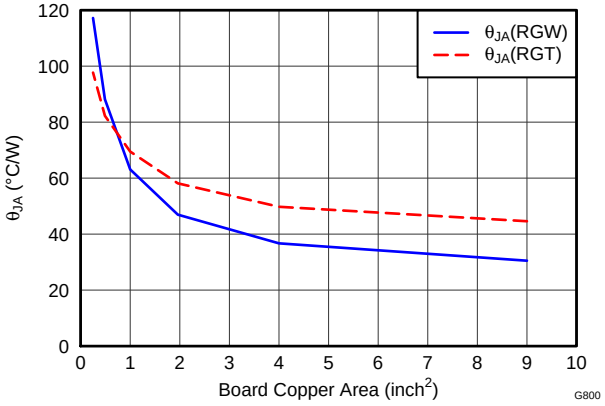


Figure 41. θ_{JA} vs Board Size

shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 3). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

Where:

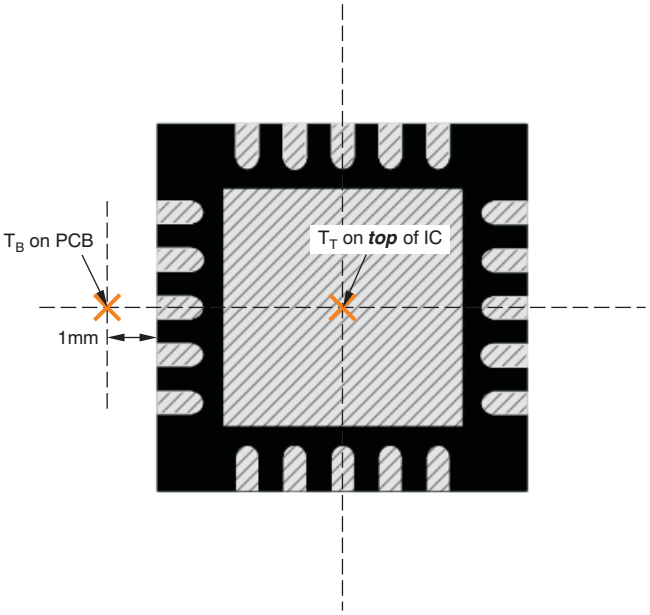
P_D is the power dissipation shown by Equation 2.

T_T is the temperature at the center-top of the IC package.

T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (see Figure 42). (3)

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see Application Report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.



(a) Example RGW (QFN) Package Measurement

Figure 42. Measuring Points for T_T and T_B

By looking at Figure 43, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 3 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

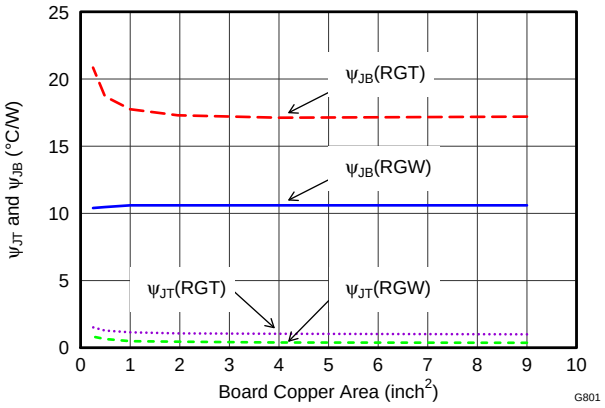


Figure 43. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to Application Report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to Application Report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2013) to Revision E **Page**

- Added new paragraph to *Current Limit* section 18

Changes from Revision C (May 2012) to Revision D **Page**

- Added C_{FF} capacitor to front page block diagram 1
- Added C_{FF} test condition and table note to Electrical Characteristics 4
- Deleted maximum value for Output Current Limit parameter in Electrical Characteristics table 4
- Added text to FB pin description 6
- Added C_{FF} capacitor to Figure 34 13
- Added C_{FF} capacitor to Figure 35 13
- Added C_{FF} capacitor to Figure 36 13
- Added C_{FF} capacitor to Figure 37 13
- Added C_{FF} capacitor to Figure 38 14
- Added C_{FF} capacitor to Figure 39 14
- Added C_{FF} capacitor to Figure 40 16
- Changed capacitor values in first sentence of OUTPUT CAPACITOR REQUIREMENTS section 17

Changes from Revision B (April 2012) to Revision C **Page**

- Added RGT package to Figure 41 19
- Added RGT package to Figure 43 20

Changes from Revision A (March 2012) to Revision B **Page**

- Changed *Accuracy* feature bullet 1
- Added RGT (QFN-16) package to Features 1
- Added RGT (QFN-16) package to Thermal Information table. 3
- Added test conditions for RGT package to *Output Voltage Accuracy* parameter 4
- Added RGT package pinout drawing 6
- Added RGT package to Pin Descriptions table 6

Changes from Original (March 2012) to Revision A **Page**

- Changed from product preview to production data 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7200RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYMQ	Samples
TPS7A7200RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYMQ	Samples
TPS7A7200RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SAC	Samples
TPS7A7200RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SAC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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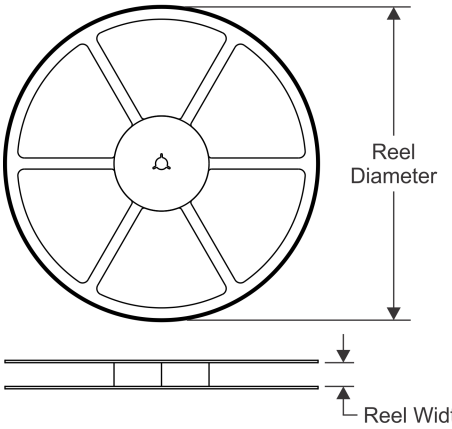
- Enhanced Product: TPS7A7200-EP

NOTE: Qualified Version Definitions:

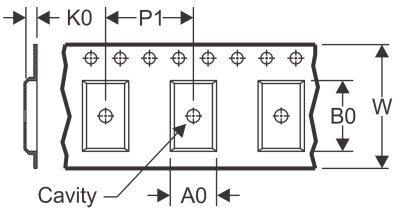
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

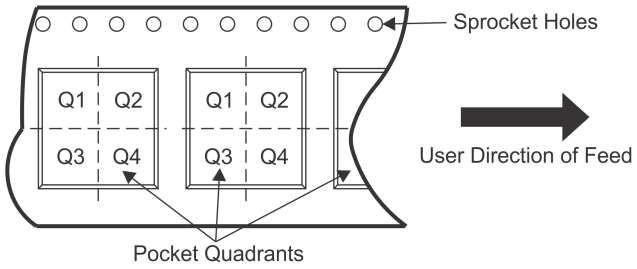


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

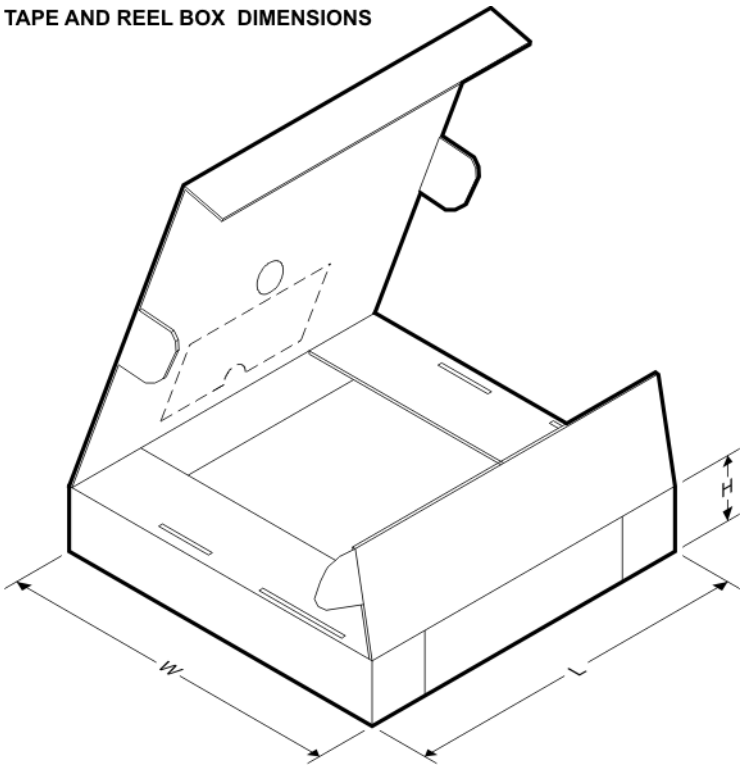
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7200RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7200RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7200RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A7200RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

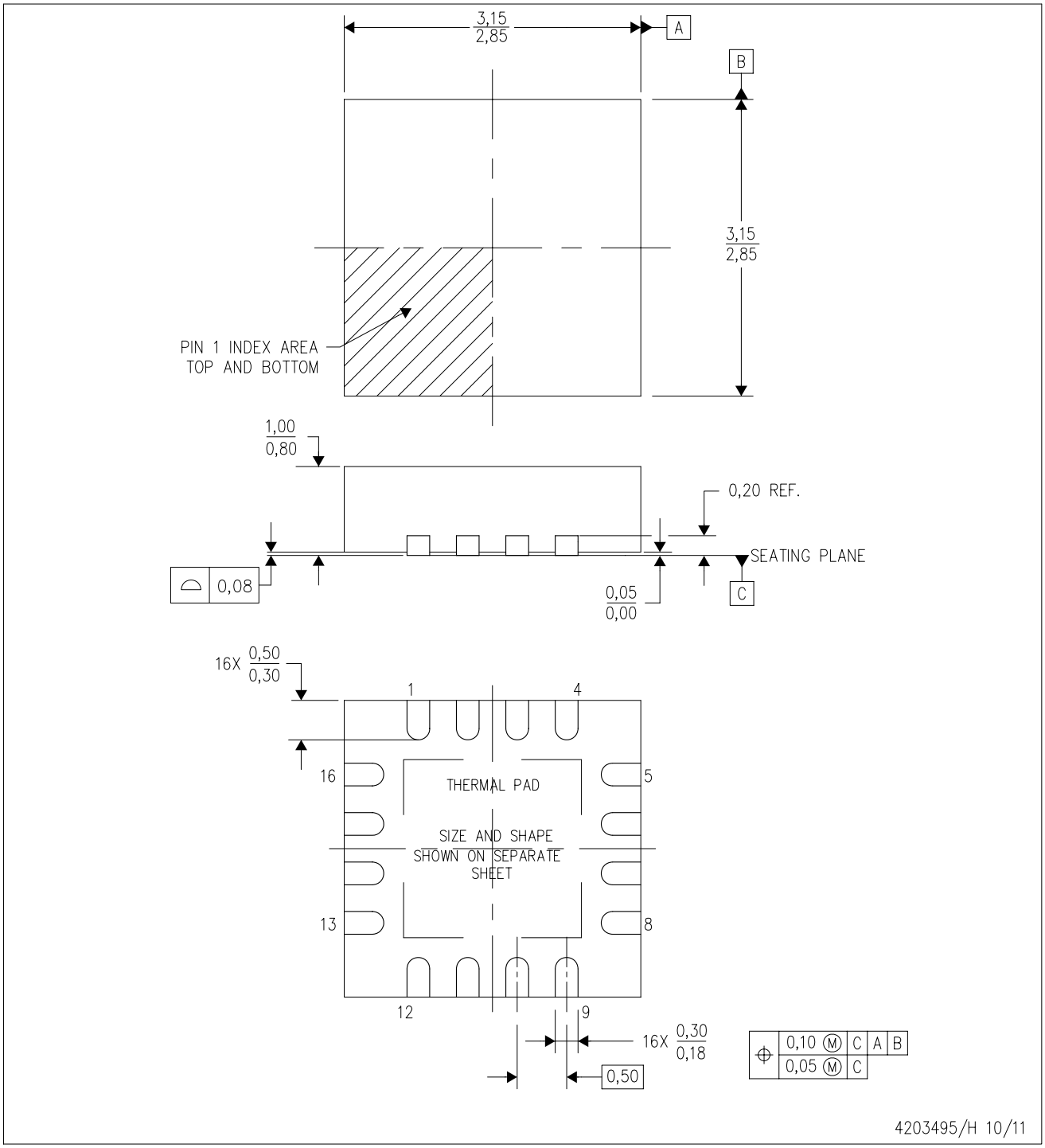
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7200RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TPS7A7200RGTT	QFN	RGT	16	250	210.0	185.0	35.0
TPS7A7200RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A7200RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

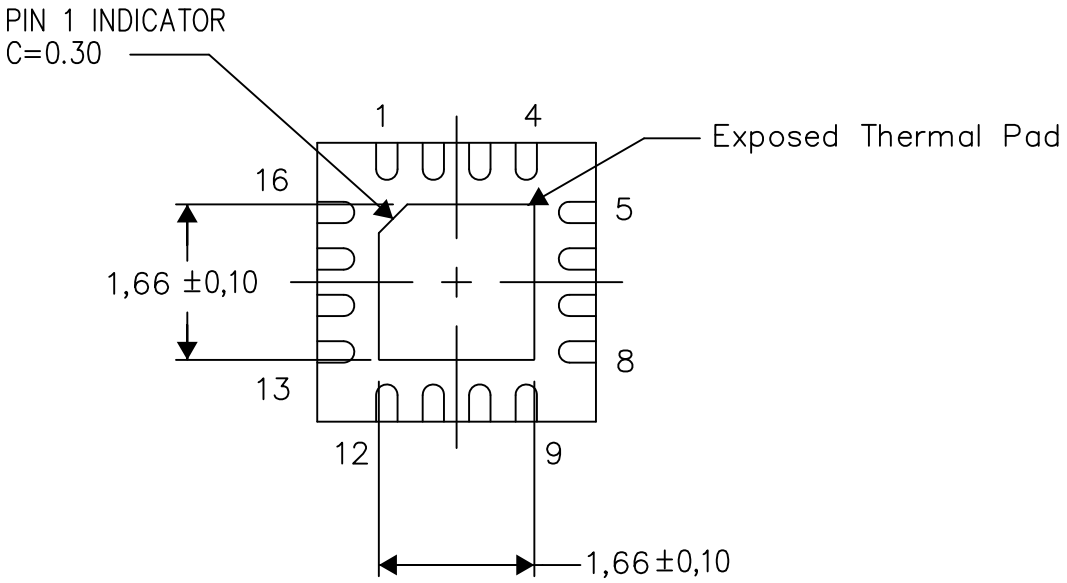
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



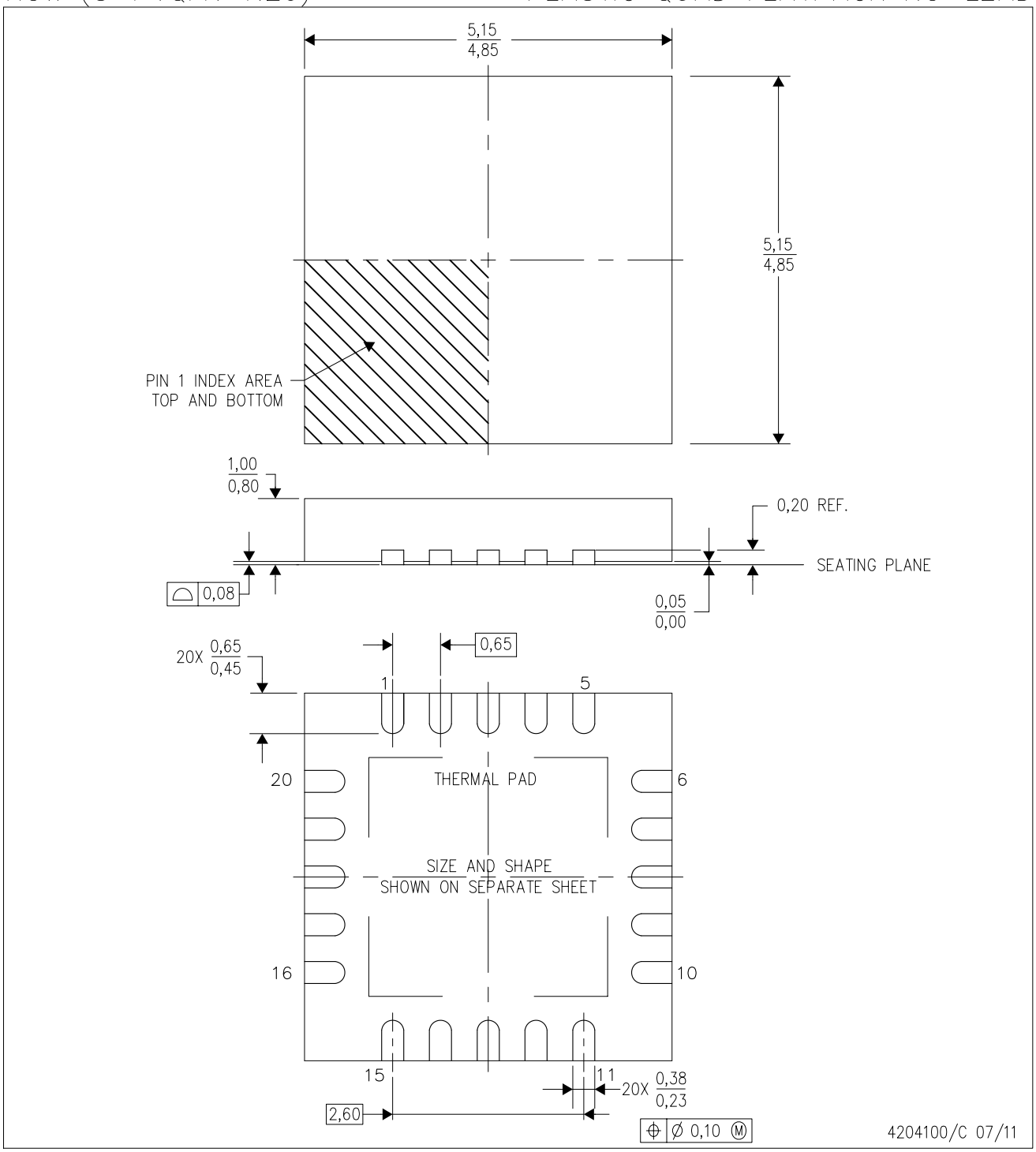
Bottom View

Exposed Thermal Pad Dimensions

4206349–10/W 10/14

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

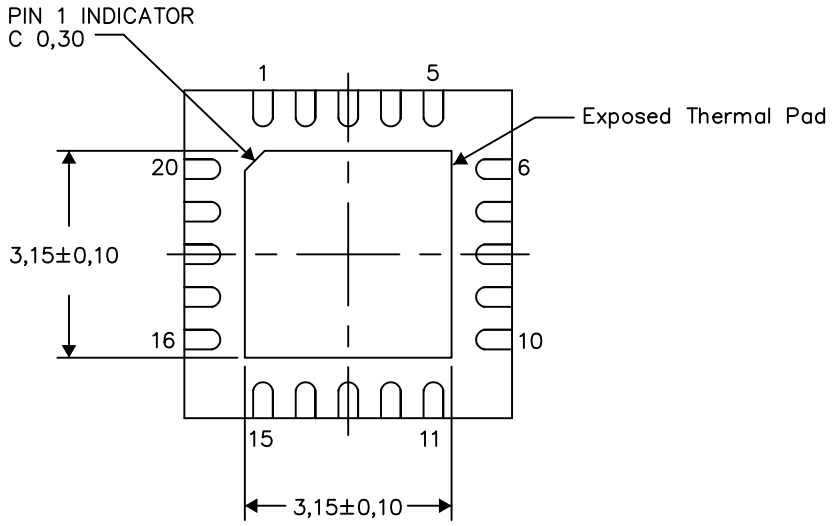
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



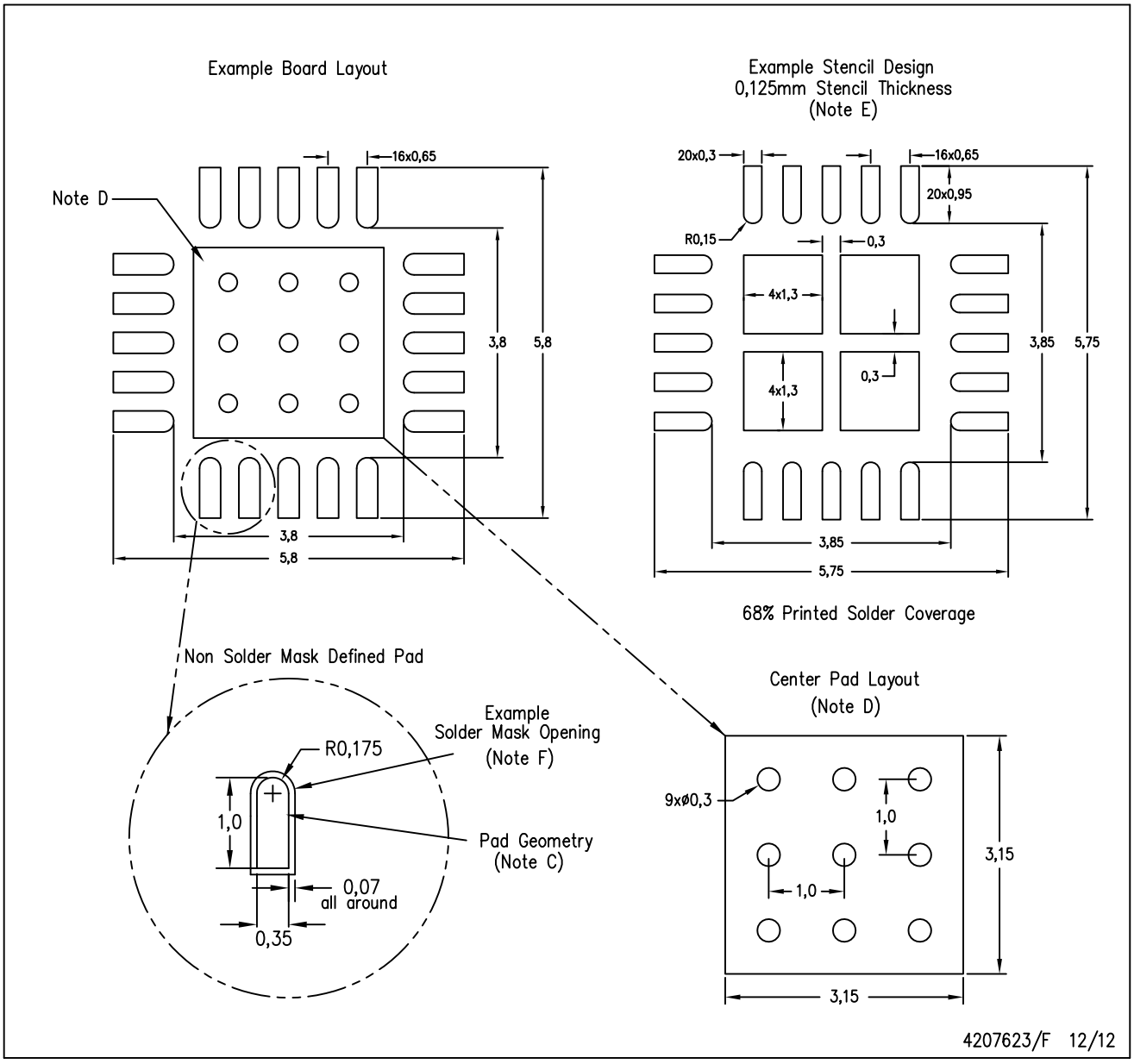
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/K 12/12

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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