Constant-Voltage, Constant-Current Controller With Primary-Side Regulation, BJT Drive

Check for Samples: UCC28722

FEATURES

- **< 50-mW No-Load Power**
- **Primary-Side Regulation (PSR) Eliminates Opto-Coupler**
- **Dynamic BJT Drive**
- **±5% Voltage and Current Regulation Across Line and Load**
- **80-kHz Maximum Switching Frequency Enables High-Power Density Charger Designs**
- **Quasi-Resonant Valley-Switching Operation for Highest Overall Efficiency**
- **Wide VDD Range Allows Small Bias Capacitor**
- **Output Overvoltage, Low-Line, and Overcurrent Protection Functions**
- **Programmable Cable Compensation**
- **SOT23-6 Package**

APPLICATIONS

- **USB-Compliant Adapters and Chargers for Consumer Electronics**
  - **Smart phones**
  - **Tablet computers**
  - **Cameras**
- **Standby Supply for TV and Desktop**
- **White Goods**

DESCRIPTION

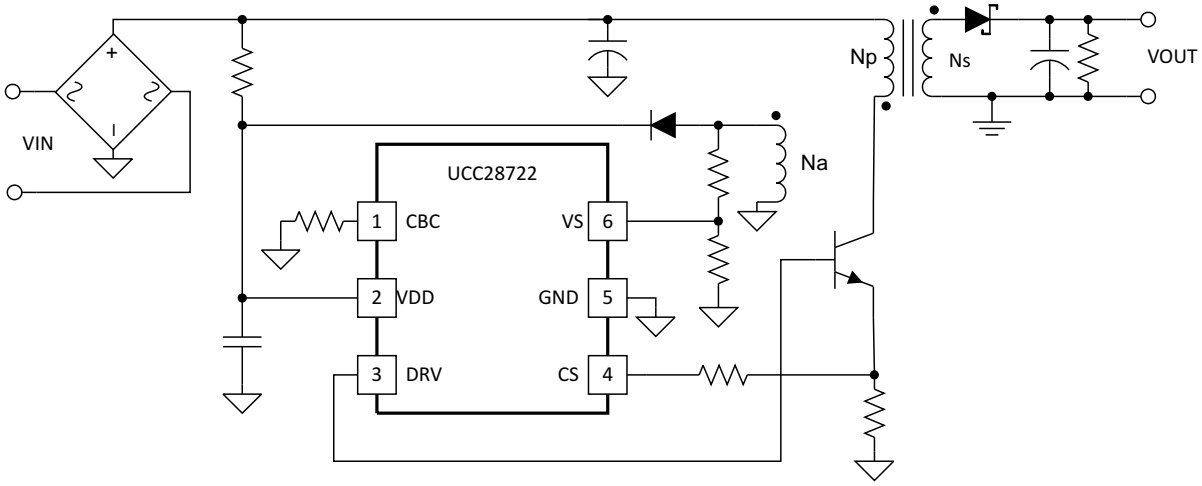
The UCC28722 flyback power supply controller provides isolated-output Constant-Voltage (CV) and Constant-Current (CC) output regulation without the use of an optical coupler. The device processes information from the primary power switch and an auxiliary flyback winding for precise control of output voltage and current.

Dynamically-controlled operating states and a tailored modulation profile support high efficiency operation at all load levels without sacrificing output transient response.

Control algorithms in the UCC28722 allow operating efficiencies to meet or exceed applicable standards. The output drive interfaces to a bipolar transistor power switch, enabling lower cost converter design. Discontinuous conduction mode (DCM) with valley switching reduces switching losses while modulation of switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

The controller has a maximum switching frequency of 80 kHz and always maintains control of the peak-primary current in the transformer. Output over voltage and overcurrent as well as input undervoltage protection features help keep primary and secondary component stresses in check. The UCC28722 also allows compensation for voltage drop in the cable to be programmed with an external resistor.

Simplified Application Diagram



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Bias supply voltage, VDD	V_{VDD}		38	V
Continuous base current sink	I_{DRV}		50	mA
Continuous base current source	I_{DRV}		Self- limiting	
Peak current, VS	I_{VS}		−1.2	
Base drive voltage at DRV	V_{DRV}	−0.5	Self- limiting	V
Voltage range	VS	−0.75	7	
	CS, CBC	−0.5	5	
Operating junction temperature range	T_J	−55	150	°C
Storage temperature	T_{STG}	−65	150	
Lead temperature 0.6 mm from case for 10 seconds			260	
ESD rating	Human-body model (HBM)		2000	V
	Charged-device model (CDM)		500	

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VDD	Bias supply operating voltage	9		35	V
C_{VDD}	VDD bypass capacitor	1.0		10	µF
R_{CBC}	Cable-compensation resistance	10			kΩ
I_{VS}	VS pin current	−1			mA
T_J	Operating junction temperature	−40		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		UCC28722 DBV 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	180.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	71.2	
θ_{JB}	Junction-to-board thermal resistance(4)	44.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	5.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	43.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, R_{CBC} = open, T_A = -40°C to 125°C, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2.00	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		95	170	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state, I_{HV} = 0		1.0	1.5	
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		2.00	2.65	mA
UNDERVOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	7.2	7.7	8.3	
VS INPUT						
V_{VSR}	Regulating level	Measured at no-load condition, T_J = 25°C(1)	3.99	4.05	4.11	V
V_{VSNC}	Negative clamp level	I_{VS} = -300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	-0.25	0	0.25	µA
CS INPUT						
$V_{CST(max)}$	Max CS threshold voltage	V_{VS} = 3.7 V	730	780	820	mV
$V_{CST(min)}$	Min CS threshold voltage	V_{VS} = 4.35 V	170	190	220	
K_{AM}	AM control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.6	4.0	4.4	V/V
V_{CCR}	Constant current regulating level	CC regulation constant	314	330	347	mV
K_{LC}	Line compensation current ratio	I_{VSLS} = -300 µA, I_{VSLS} / current out of CS pin	24.0	25.0	28.6	A/A
T_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	230	290	355	ns
DRIVER						
$I_{DRS(max)}$	Maximum DRV source current	V_{DRV} = 2 V, V_{VDD} = 9 V, V_{VS} = 3.85 V	31	37	42	mA
$I_{DRS(min)}$	Minimum DRV source current	V_{DRV} = 2 V, V_{VDD} = 9 V, V_{VS} = 4.30 V	15	19	23	
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		1	2.4	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		5.9	7	V
R_{DRVSS}	DRV pull-down in start state			20	25	kΩ
TIMING						
$f_{SW(max)}$	Maximum switching frequency	V_{VS} = 3.7 V	72	80	89	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} = 4.35 V	570	650	750	Hz
t_{ZTO}	Zero-crossing timeout delay		2.4	3.1	3.7	µs

(1) The regulating level and over voltage at VS decreases with temperature by 0.8 mV/°C. This compensation is included to reduce the power supply output voltage variance over temperature.

ELECTRICAL CHARACTERISTICS (continued)

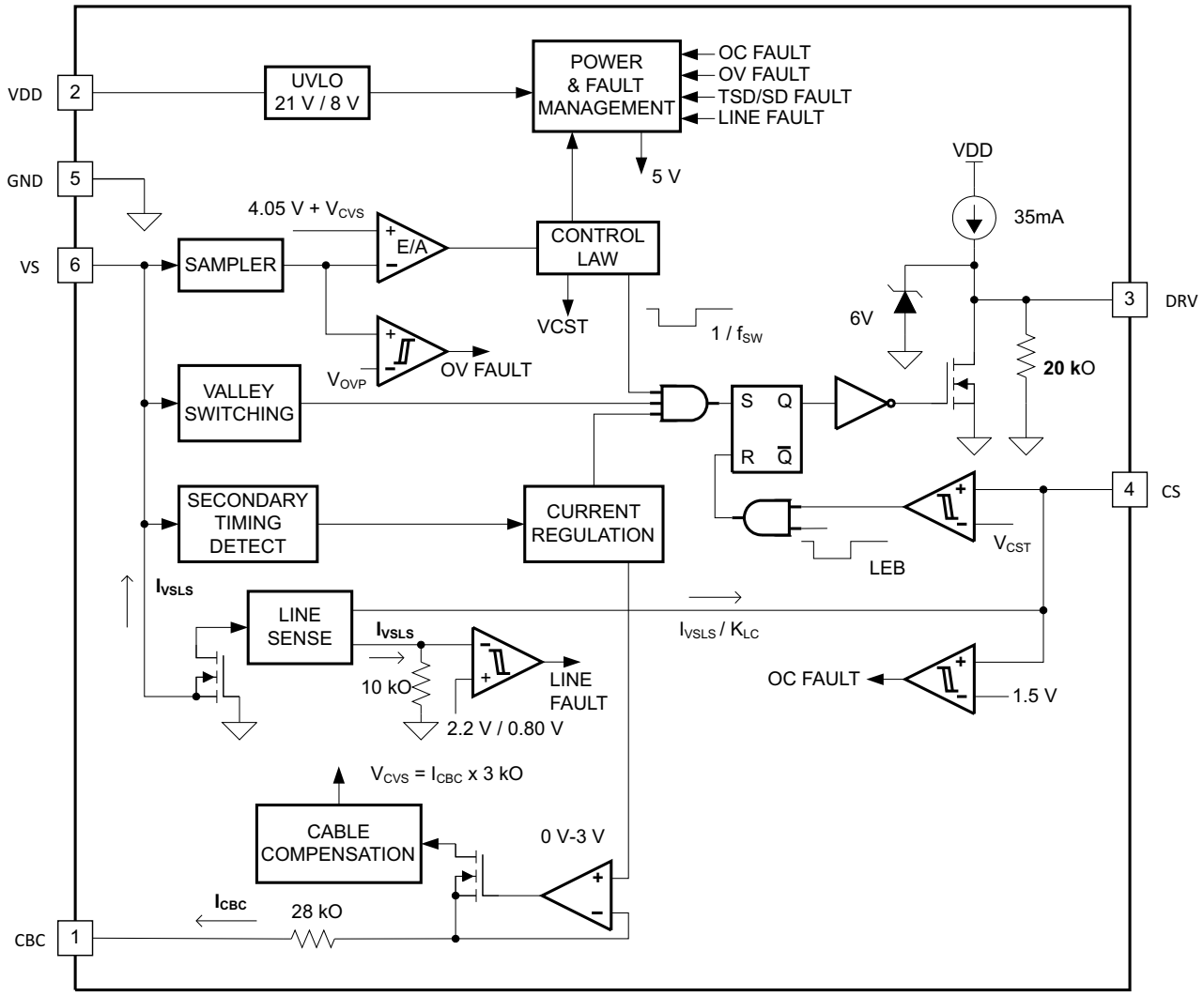
over operating free-air temperature range, V_{VDD} = 25 V, HV = open, R_{CBC} = open, T_A = -40°C to 125°C, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION						
V_{OVP}	Over-voltage threshold	At VS input, T_J = 25°C (2)	4.49	4.60	4.75	V
V_{OCP}	Over-current threshold	At CS input	1.4	1.5	1.6	
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing	188	225	277	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing	70	80	100	
K_{VSL}	VS line sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$	2.45	2.80	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature	Internal junction temperature		165		°C
CABLE COMPENSATION						
$V_{CBC(max)}$	Cable compensation maximum voltage	Voltage at CBC at full load	2.9	3.1	3.5	V
$V_{CVS(min)}$	Minimum compensation at VS	V_{CBC} = open, change in VS regulating level at full load	-55	-15	25	mV
$V_{CVS(max)}$	Maximum compensation at VS	V_{CBC} = 0 V, change in VS regulating level at full load	270	320	385	

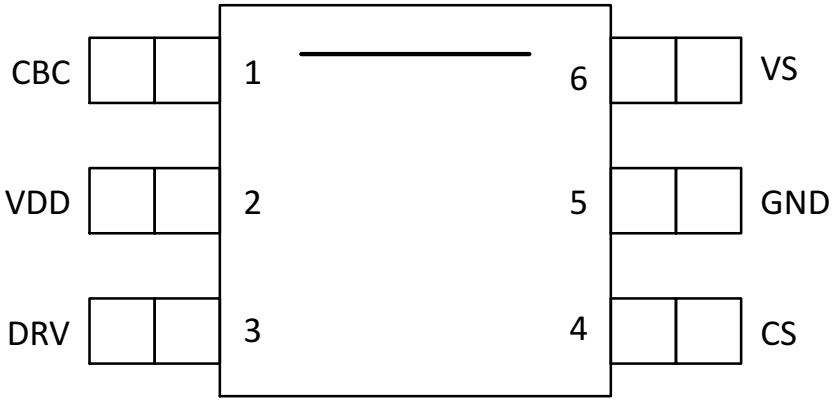
(2) The regulating level and over voltage at VS decreases with temperature by 0.8 mV/°C. This compensation is included to reduce the power supply output voltage variance over temperature.

DEVICE INFORMATION

Functional Block Diagram



DBV Package
(Top view)



PIN FUNCTIONS

NAME	NUMBER	I/O	DESCRIPTION
CBC	1	I	Cable compensation is a programming pin for compensation of cable voltage drop. Cable compensation is programmed with a resistor to GND.
CS	4	I	Current sense input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the AC-mains input varies.
DRV	3	O	Drive is an output used to drive the base of an external high voltage NPN transistor.
GND	5	—	The ground pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
VDD	2	I	VDD is the bias supply input pin to the controller. A carefully-placed bypass capacitor to GND is required on this pin.
VS	6	I	Voltage sense is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin.

Detailed Pin Description

VDD (Device Bias Voltage Supply): The VDD pin is connected to a bypass capacitor to ground. The VDD turn-on UVLO threshold is 21 V and turn-off UVLO threshold is 7.7 V, with an available operating range up to 35 V on VDD. The USB charging specification requires the output current to operate in constant-current mode from 5 V to a minimum of 2 V; this is easily achieved with a nominal VDD of approximately 22 V. The additional VDD headroom up to 35 V allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in high-load conditions. Note that it is possible for the startup resistor to supply more current to the VDD node than the IC will comsume at higher bulk input voltages. A zener diode clamp will be required on the VDD pin to keep the VDD pin voltage within limits if this is the case.

GND (Ground): There is a single ground reference external to the device for the base drive current and analog signal reference. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

VS (Voltage-Sense): The VS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Avoid placing a filter capacitor on this input which would interfere with accurate sensing of this waveform.

The VS pin also senses the bulk capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. During the transistor on-time the VS pin is clamped to approximately 250 mV below GND and the current out of the VS pin is sensed. For the AC-input run/stop function, the run threshold on VS is 225 µA and the stop threshold is 80 µA. The values for the auxilliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turn-on of the controller (run),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time. (see ELECTRICAL CHARACTERISTICS)

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (2)$$

where

- V_{OCV} is the converter regulated output voltage,
- V_F is the output rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary to secondary turns ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{VSR} is the CV regulating level at the VS input (see ELECTRICAL CHARACTERISTICS).

DRV (Base Drive): The DRV pin is connected to the NPN transistor base pin. The driver provides a base drive signal limited to 7 V. The turn-on characteristic of the driver is a 19 mA to 37 mA current source that is scaled with the current sense threshold dictated by the operating point in the control scheme. When the minimum current sense threshold is being used, the base drive current is also at its minimum value. As the current sense threshold is increased to the maximum, the base drive current scales linearly with it to its maximum of 35 mA typical. The turn-off current is determined by the low-side driver $R_{DS(on)}$

CS (Current Sense): The current-sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The current-sense threshold is 0.78 V for $I_{PP(max)}$ and 0.19 V for $I_{PP(min)}$. The series resistor R_{LC} provides the function of feed-forward line compensation to eliminate change in I_{PP} due to change in di/dt and the propagation delay of the internal comparator and NPN transistor turn-off time. There is an internal leading-edge blanking time of approximately 300 ns to eliminate sensitivity to the turn-on current spike. It should not be necessary to place a bypass capacitor on the CS pin. The value of R_{CS} is determined by the target output current in Constant Current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example: With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 1.5%. The η_{XFMR} value is approximately: 1 - 0.05 - 0.035 - 0.015 = 0.9.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (3)$$

where

- V_{CCR} is a current regulation constant (see ELECTRICAL CHARACTERISTICS),
- N_{PS} is the transformer primary-to-secondary turns ratio (a ratio of 13 to 15 is recommended for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (4)$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the current-sense delay including NPN transistor turn-off delay, add ~50 ns to transistor delay,
- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see ELECTRICAL CHARACTERISTICS).

CBC (Cable Compensation): The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation to offset cable resistance. The cable compensation block provides a 0-V to 3-V voltage level on the CBC pin corresponding to $I_{OCC(max)}$ output current. Connecting a resistance from CBC to GND programs a current that is summed into the VS feedback divider, increasing the regulation voltage as I_{OUT} increases. There is an internal series resistance of 28 kΩ to the CBC pin which sets a maximum cable compensation of a 5-V output to 400 mV when CBC is shorted to ground. The CBC resistance value can be determined by the equation below.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\,k\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28\,k\Omega \quad (5)$$

where

- V_{OCV} is the regulated output voltage,
- V_F is the diode forward voltage in V,
- V_{OCBC} is the target cable compensation voltage at the output terminals,
- $V_{CBC(max)}$ is the maximum voltage at the cable compensation pin at the maximum converter output current (see ELECTRICAL CHARACTERISTICS),
- V_{VSR} is the CV regulating level at the VS input (see ELECTRICAL CHARACTERISTICS).

TYPICAL CHARACTERISTICS

VDD = 25 V, unless otherwise noted.

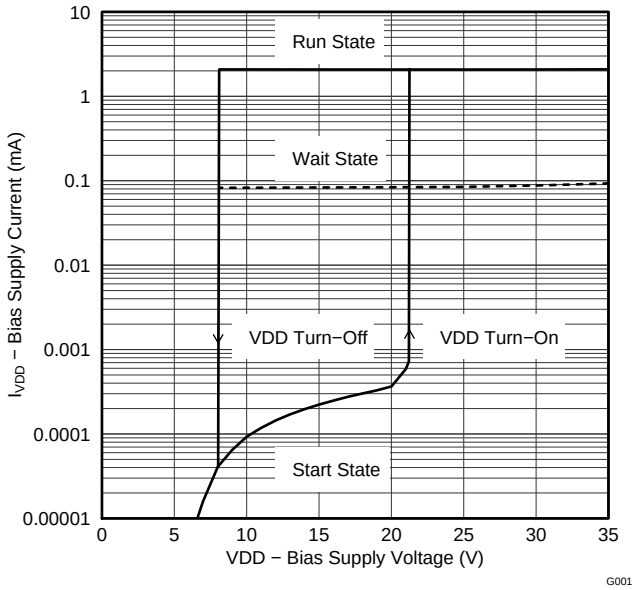


Figure 1. Bias Supply Current vs. VDD Voltage

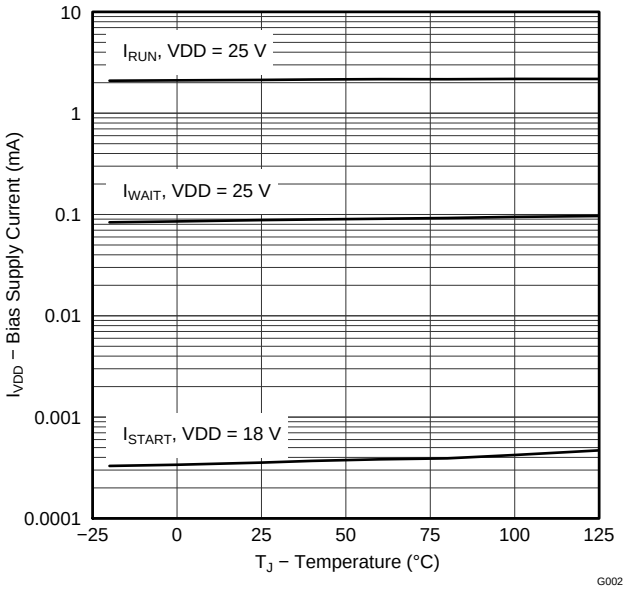


Figure 2. Operating Current vs. Junction Temperature

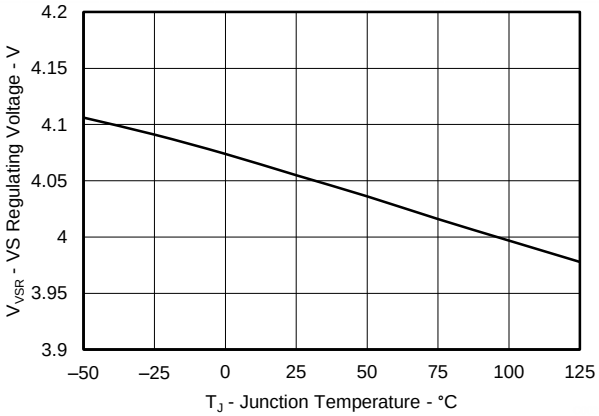


Figure 3. VS Pin Regulation Voltage vs. Junction Temperature

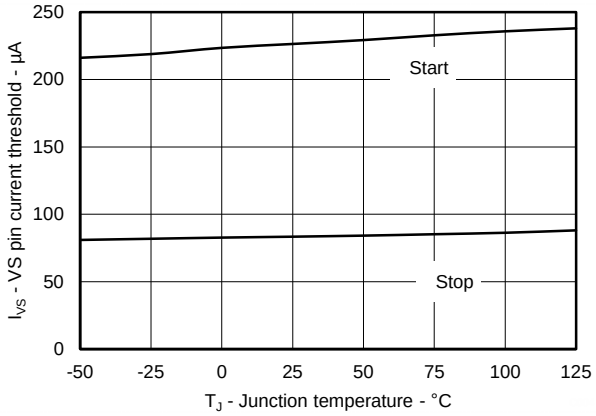


Figure 4. VS Pin Start and Stop Thresholds vs. Junction Temperature

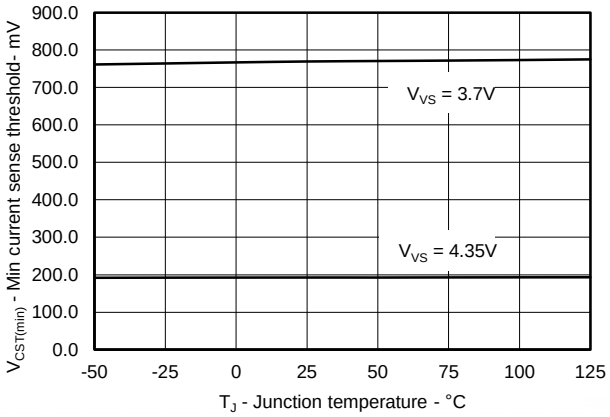


Figure 5. Current Sense Threshold vs. Temperature

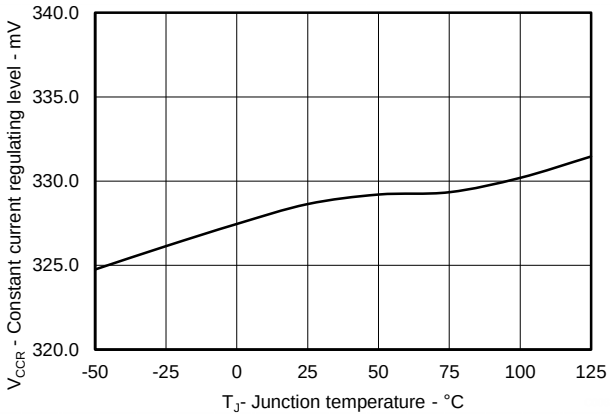


Figure 6. Constant Current Regulation Level vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

VDD = 25 V, unless otherwise noted.

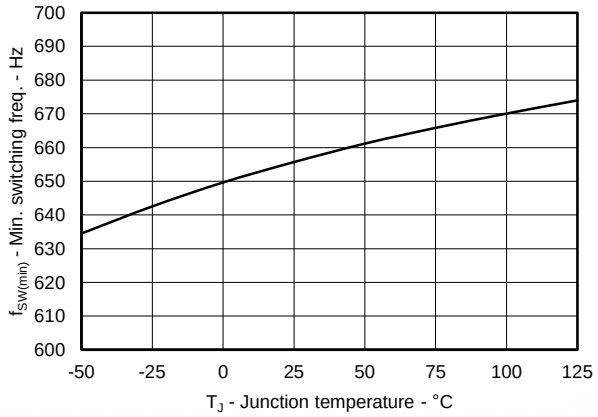


Figure 7. Minimum Switching Frequency vs. Junction Temperature

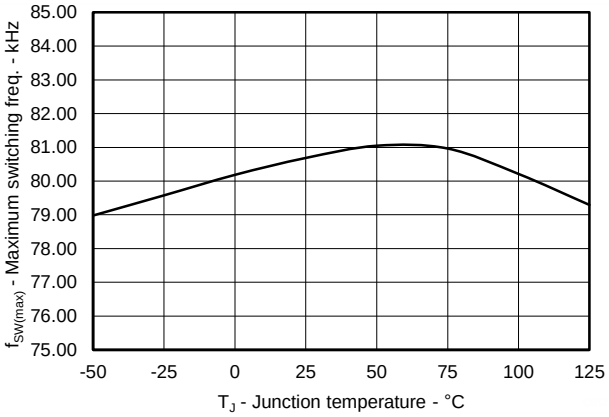


Figure 8. Maximum Switching Frequency vs. Junction Temperature

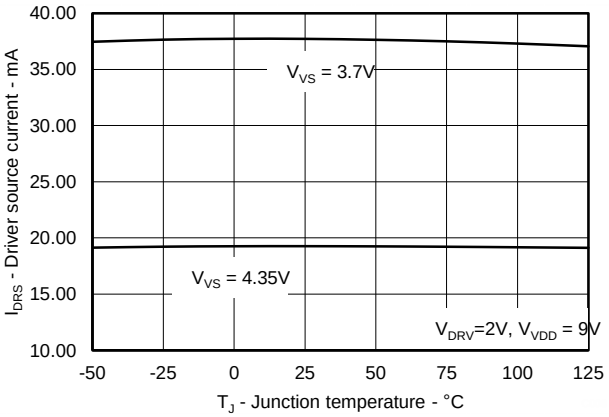


Figure 9. Driver Output Source Current vs. Junction Temperature

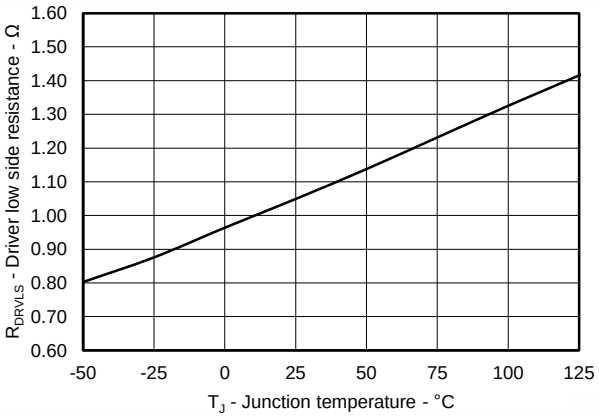


Figure 10. Driver Pull Down Resistance vs. Junction Temperature

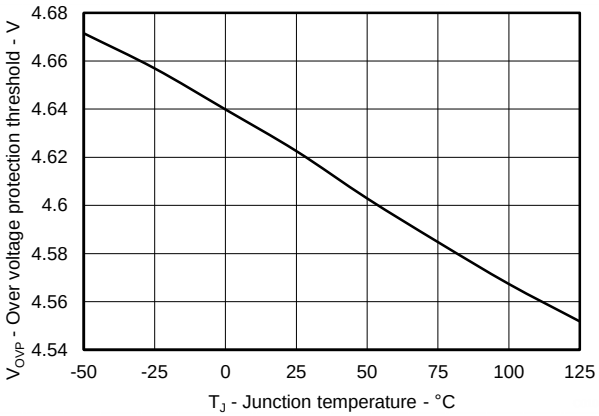


Figure 11. Over Voltage Protection Threshold vs. Junction Temperature

FUNCTIONAL DESCRIPTION

The UCC28722 is a flyback power supply controller which provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The control law provides a wide-dynamic operating range of output power which allows the power designer to achieve less than 75-mW of stand-by power.

During low-power operating ranges the device has power management features to reduce the device operating current at operating frequencies below 28 kHz. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost and low component count.

Primary-Side Voltage Regulation

Figure 12 illustrates a simplified flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.

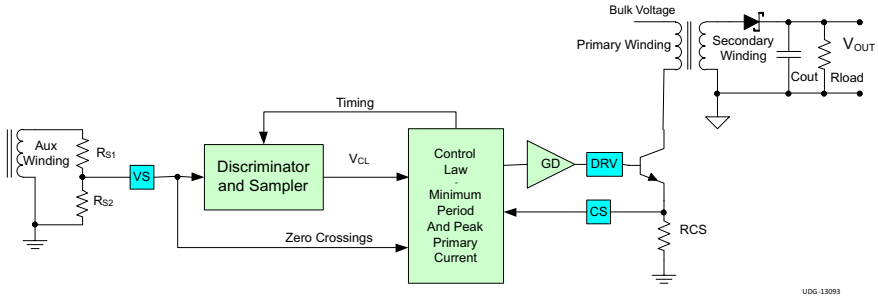


Figure 12. Simplified Flyback Convertor (with the main voltage regulation blocks)

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in Figure 13 it is clear there is a down slope representing a decreasing total rectifier V_F and resistance voltage drop ($I_S R_S$) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably recognizes the leakage inductance reset and ringing and ingores it, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V. Temperature compensation on the VS reference voltage of -0.8-mV/°C offsets the change in the output rectifier forward voltage with temperature. The resistor divider is selected as outlined in the VS pin description.

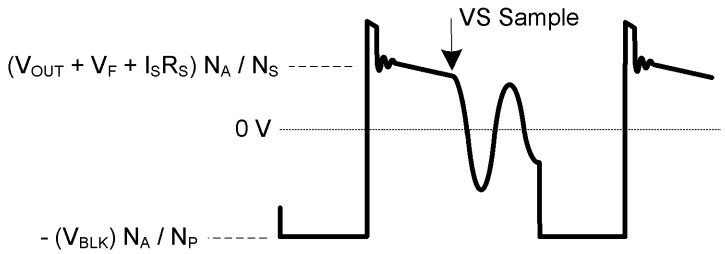


Figure 13. Auxiliary Winding Voltage

The UCC28722 includes a VS signal sampler that uses discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are some conditions that must be met on the auxiliary winding signal to ensure reliable operation. These conditions are the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 14 below for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET} in Figure 14. Because this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time less than 600 ns for I_{PRI} minimum, and less than 2.2 µs for I_{PRI} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DM}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS scales up when measured at the auxiliary winding by R_{S1} and R_{S2}, and is equal to 100 mV x (R_{S1} + R_{S2}) / R_{S2} when measured directly at the auxilliary winding.

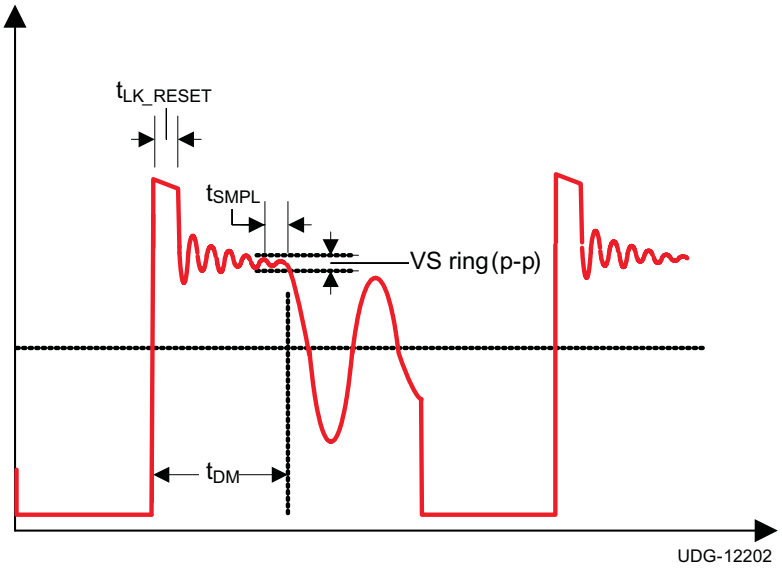


Figure 14. Auxiliary Waveform Details

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode as illustrated in Figure 15 below. The internal operating frequency limits of the device are 80 kHz, $f_{SW(max)}$ and 650 Hz, $f_{SW(min)}$. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no stability compensation required for the UCC28722.

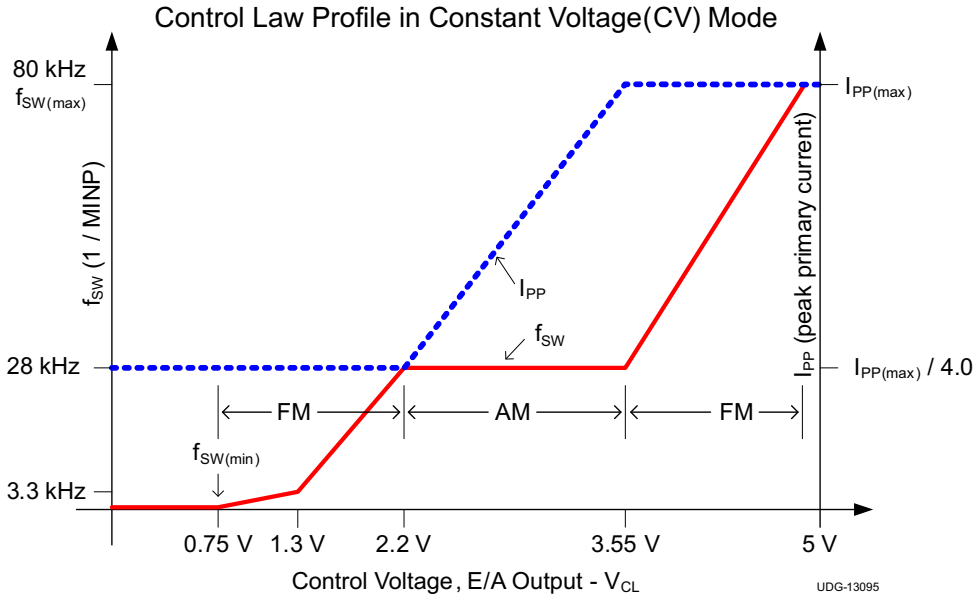


Figure 15. Frequency and Amplitude Modulation Modes (during voltage regulation)

Primary-Side Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{PP(max)}$. Referring to Figure 16 below, the primary-peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by Equation 6. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

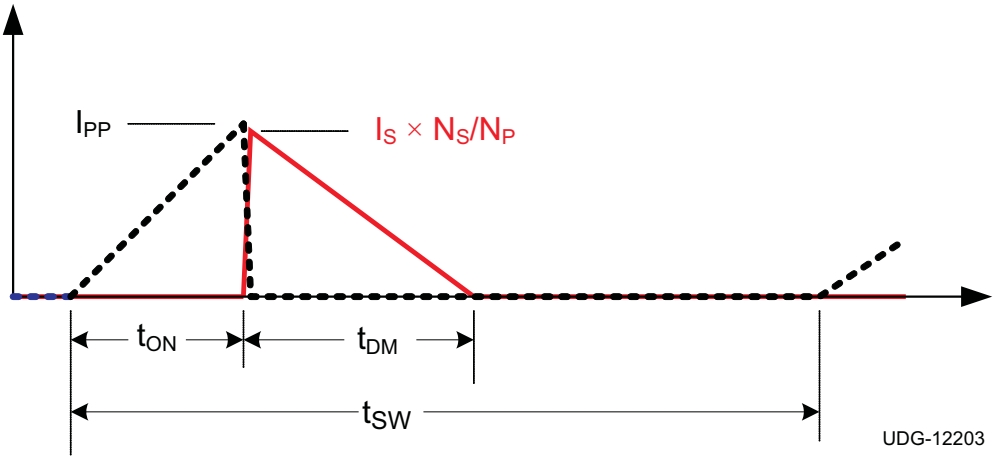


Figure 16. Transformer Currents

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (6)$$

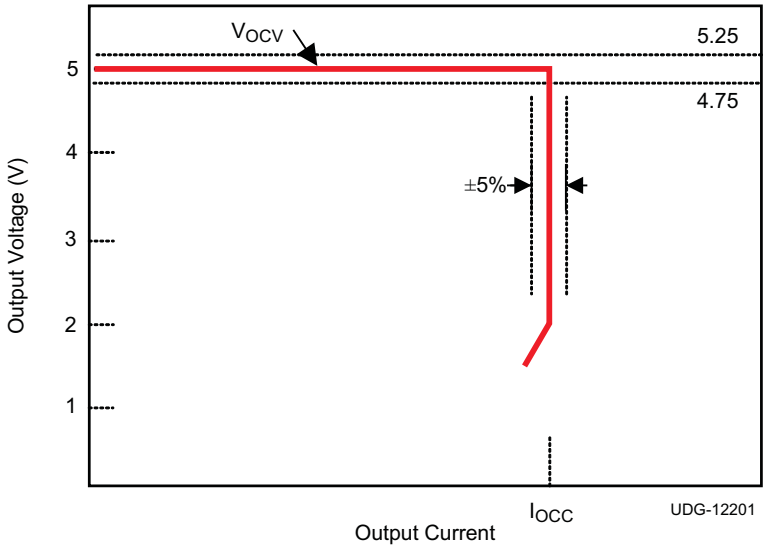


Figure 17. Typical Target Output V-I Characteristic

Valley Switching

The UCC28722 utilizes valley switching to reduce switching losses in the transistor, to reduce induced-EMI, and to minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the collector voltage (V_C) ringing has subsided.

Referring to Figure 18 below, the UCC28722 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_C.

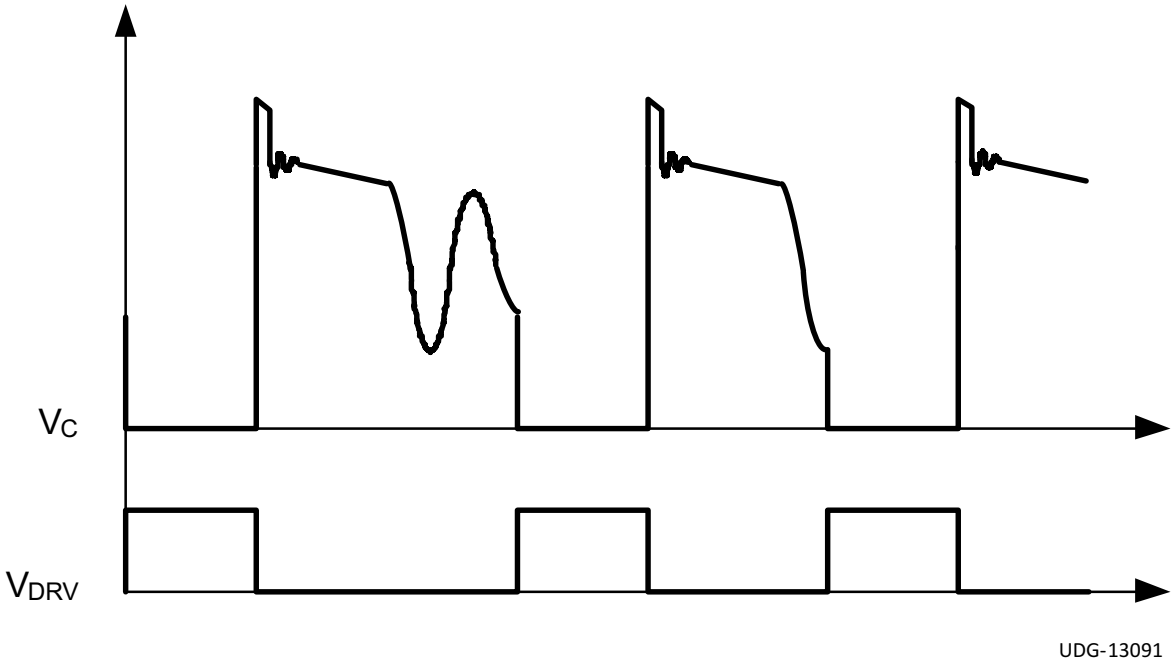


Figure 18. Valley-Skipping Mode

Start-Up Operation

An external resistor connected from the bulk capacitor voltage (V_{BLK}) to the VDD pin charges the VDD capacitor. The amount of startup current that is available to charge the VDD aapacitor is dependent on the value of this external startup resistor. Larger values supply less current and increase startup time but at the expense of increasing standby power and decreasing efficiency paeritularly at high input voltage and light loading. When VDD reaches the 21-V UVLO turn-on threshold, the controller is enabled, the converter starts switching. The initial three cycles are limited to $I_{PP(min)}$. After the initial three cycles at minimum $I_{PP(min)}$, the controller responds to the condition dictated by the control law. The converter will remain in discontinuous mode during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

Note that it is possible for the startup resistor to supply more current to the VDD node than the IC will comsume at higher bulk input voltages. A zener diode clamp will be required on the VDD pin to keep the VDD pin voltage within limits if this is the case.

Fault Protection

The UCC28722 provides comprehensive fault protection. Protection functions include:

- Output over-voltage fault
- Input under-voltage fault
- Internal over-temperature fault
- Primary over-current fault
- CS pin fault
- VS pin fault

A UVLO reset and restart sequence applies for all fault protection events.

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal V_{OUT}, the device stops switching and the internal current consumption is I_{FAULT} which discharges the VDD capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

The UCC28722 always operates with cycle-by-cycle primary peak current control. The normal operating range of the CS pin is 0.78 V to 0.195 V. There is additional protection if the CS pin reaches 1.5 V. This results in a UVLO reset and restart sequence.

The line input run and stop thresholds are determined by current information at the VS pin during the transistor on-time. While the VS pin is clamped close to GND during the transistor on-time, the current through R_{S1} is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. The run current threshold is 225 µA and the stop current threshold is 80 µA.

The internal over-temperature protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

Layout Considerations

As with all switching power supplies, attention to detail in the layout can save much troubleshooting later on.

- Minimizing the loop area and trace length on the power path circuits on both the primary and secondary sides of the converter will help with both EMI and converter overall performance, as will close coupling the storage capacitors associated with both circuits.
- Keep traces with high dV/dt potential away from or shielded from sensitive signal traces. Two prime examples of this would be the transistor collector circuit and the output of the AUX winding.
- Do not run traces with high dI/dt capability next to signal level traces. One place that this might not be apparent initially is on the common side of the AUX winding. The trace between the AUX winding common and the VDD capacitor is subject to high dI/dt when the transistor is turned off. If this connection is run parallel to a signal trace, it can couple into that circuit and cause issues. If this trace must cross a signal line, such as CS, keep them as separate as possible and cross at right angles.

At the controller:

- The VDD capacitor should be as close as physically possible to the VDD and GND pins. the most critical pins after that are the VS pin and the CS pin. These sense current and voltage in the converter and control output regulation an current limit respectively.
- The VS pin should be connected to the voltage divider on the AUX winding with as short a trace as practical. This node can be relatively high impedance and susceptible to noise pickup. Minimimize this possibility with short connections. between the AUX winding divider resistors, the bottom of the divider and GND of the conroller as well as from the VS pin to the center of the divider.
- The CS pin in addition to functionaing as the current sense pin also serves as the compensation for transistor turn off delay. Using this requires a compensation resistor placed between the CS pin and the current sense resistor. To minimize the possibility of noise pickup, place the compensation resistor close to the CS pin, minimizing the higher impedance connection length.

DESIGN PROCEDURE

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28722 controller. Refer to the Figure 19 for component names and network locations. The design procedure equations use terms that are defined below.

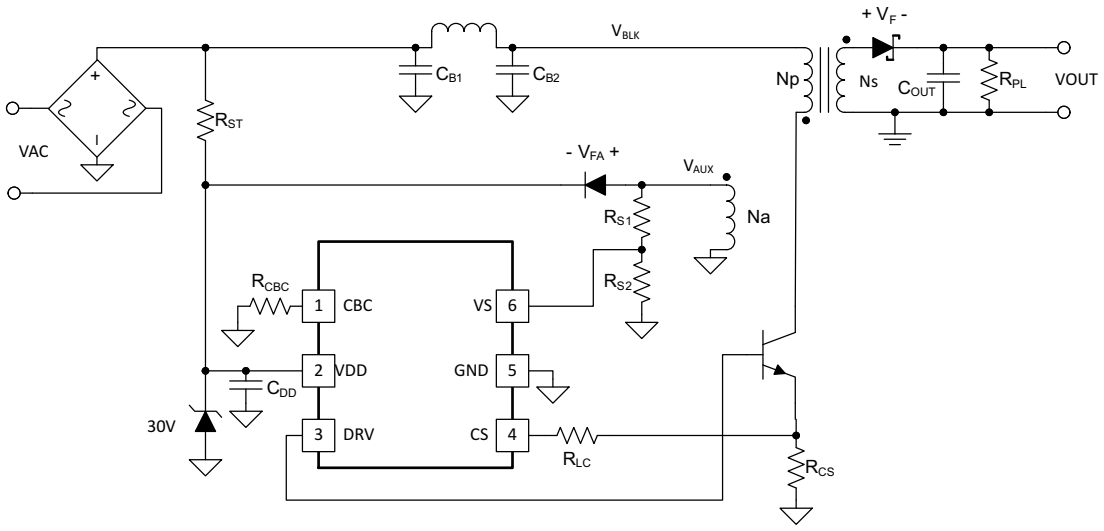


Figure 19. Design Procedure Application Example

Definition of Terms

Capacitance Terms in Farads

- **C_{BULK}:** total input capacitance of C_{B1} and C_{B2}.
- **C_{DD}:** minimum required capacitance on the VDD pin.
- **C_{OUT}:** minimum output capacitance required.

Duty Cycle Terms

- **D_{MAGCC}:** secondary diode conduction duty cycle in CC, 0.425.
- **D_{MAX}:** transistor on-time duty cycle.

Frequency Terms in Hertz

- **f_{LINE}:** minimum line frequency.
- **f_{MAX}:** target full-load maximum switching frequency of the converter.
- **f_{MIN}:** minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device.
- **$f_{SW(min)}$:** minimum switching frequency (see ELECTRICAL CHARACTERISTICS).

Current Terms in Amperes

- **I_{OCC}:** converter output constant-current target.
- **$I_{PP(max)}$:** maximum transformer primary current.
- **I_{START}:** start-up bias supply current (see ELECTRICAL CHARACTERISTICS).
- **I_{TRAN}** : required positive load-step current.
- **$I_{VSL(run)}$:** VS pin run current (see ELECTRICAL CHARACTERISTICS).
- **I_{DRS}:** Driver source current (see ELECTRICAL CHARACTERISTICS).

Current and Voltage Scaling Terms

- **K_{AM}:** maximum-to-minimum peak primary current ratio (see ELECTRICAL CHARACTERISTICS).
- **K_{LC}:** current-scaling constant (see ELECTRICAL CHARACTERISTICS).

Transformer Terms

- **L_P:** transformer primary inductance.
- **N_{AS}:** transformer auxiliary-to-secondary turns ratio.
- **N_{PA}:** transformer primary-to-auxiliary turns ratio.
- **N_{PS}:** transformer primary-to-secondary turns ratio.

Power Terms in Watts

- **P_{IN}:** converter maximum input power.
- **P_{OUT}:** full-load output power of the converter.
- **P_{RSTR}:** VDD start-up resistor power dissipation.
- **P_{SB}:** total stand-by power.
- **P_{SB_CONV}:** P_{SB} minus start-up resistor and snubber losses.

Resistance Terms in Ω

- **R_{CS}:** primary current programming resistance.
- **R_{ESR}:** total ESR of the output capacitor(s).
- **R_{PL}:** preload resistance on the output of the converter.
- **R_{S1}:** high-side VS pin resistance.
- **R_{S2}:** low-side VS pin resistance.
- **R_{STR}** : startup resistance.

Timing Terms in Seconds

- **t_D:** current-sense delay including transistor turn-off delay; add 50 ns to transistor delay.
- **$t_{DMAG(min)}$:** minimum secondary rectifier conduction time.
- **$t_{ON(min)}$:** minimum transistor on time.
- **t_R:** resonant frequency during the DCM (discontinuous conduction mode) time.
- **t_{ST}:** startup time

Voltage Terms in Volts

- **V_{BLK}:** highest bulk capacitor voltage for stand-by power measurement.
- **$V_{BULK(min)}$:** minimum voltage on C_{B1} and C_{B2} at full power.
- **V_{OCBC}:** target cable compensation voltage at the output terminals.
- **$V_{CBC(max)}$:** maximum voltage at the CBC pin at the maximum converter output current (see ELECTRICAL CHARACTERISTICS).
- **V_{CCR}:** constant-current regulating voltage (see ELECTRICAL CHARACTERISTICS).
- **$V_{CST(max)}$:** CS pin maximum current-sense threshold (see ELECTRICAL CHARACTERISTICS).
- **$V_{CST(min)}$:** CS pin minimum current-sense threshold (see ELECTRICAL CHARACTERISTICS).
- **$V_{DD(off)}$:** UVLO turn-off voltage (see ELECTRICAL CHARACTERISTICS).
- **$V_{DD(on)}$:** UVLO turn-on voltage (see ELECTRICAL CHARACTERISTICS).
- **$V_{O\Delta}$:** output voltage drop allowed during the load-step transient.
- **V_{CPK}:** peak transistor collector to emitter voltage at high line.
- **V_F:** secondary rectifier forward voltage drop at near-zero current.
- **V_{FA}:** auxiliary rectifier forward voltage drop.
- **V_{LK}:** estimated leakage inductance energy reset voltage.
- **V_{OCV}:** regulated output voltage of the converter.
- **V_{OCC}:** target lowest converter output voltage in constant-current regulation.
- **V_{REV}:** peak reverse voltage on the secondary rectifier.
- **V_{RIPPLE}:** output peak-to-peak ripple voltage at full-load.
- **V_{VSR}:** CV regulating level at the VS input (see ELECTRICAL CHARACTERISTICS).

AC Voltage Terms in V_{RMS}

- **$V_{IN(max)}$:** maximum input voltage to the converter.
- **$V_{IN(min)}$:** minimum input voltage to the converter.
- **$V_{IN(run)}$:** converter input start-up (run) voltage.

Efficiency Terms

- **η_{SB}:** estimated efficiency of the converter at no-load condition, not including start-up resistance or bias losses. For a 5-V USB charger application, 60% to 65% is a good initial estimate.
- **η:** converter overall efficiency.
- **η_{XFMR}:** transformer primary-to-secondary power transfer efficiency.

Stand-by Power Estimate

Assuming no-load stand-by power is a critical design parameter, determine estimated no-load power based on target converter maximum switching frequency and output power rating.

The following equation estimates the stand-by power of the converter.

$$P_{SB\_CONV} = \frac{P_{OUT} \times f_{MIN}}{\eta_{SB} \times K_{AM}^{2} \times f_{MAX}} \tag{7}$$

For a typical USB charger application, the bias power during no-load is approximately 2.5 mW. This is based on 25-V VDD and 100-µA bias current. The output preload resistor can be estimated by V_{OCV} and the difference in the converter stand-by power and the bias power. The equation for output preload resistance accounts for bias power estimated at 2.5 mW.

$$R_{PL} = \frac{V_{OCV}^{2}}{P_{SB\_CONV} - 2.5\,mW} \tag{8}$$

Typical startup resistance values for R_{STR} range from 1 MΩ to 5MΩ to achieve 2 s startup time The capacitor bulk voltage for the loss estimation is the highest voltage for the stand-by power measurement, typically 325 V_{DC}.

$$P_{RSTR} = \frac{V_{BLK}^{2}}{R_{STR}} \tag{9}$$

For the total stand-by power estimation add an estimated 2.5 mW for snubber loss to the converter stand-by power loss.

$$P_{SB} = P_{SB\_CONV} + 2.5\,mW \tag{10}$$

$$P_{SB} = P_{SB\_CONV} + P_{RSTR} + 2.5\,mW \tag{11}$$

Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np to Ns turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{12}$$

The below equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{2} - V_{BULK(min)}^{2}\right) \times f_{LINE}} \tag{13}$$

Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{CE} voltage is ½ of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX} \right) - D_{MAGCC} \tag{14}$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the UCC28722 at 0.425. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV}, the secondary rectifier V_F, and the cable compensation voltage (V_{OCBC}). For the 5-V USB charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \tag{15}$$

Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28722 constant-current regulation is achieved by maintaining a maximum D_{MAG} duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a 5-V, 1-A charger example, bias power of 1.5% is a good estimate. An overall transformer efficiency of 0.9 is a good estimate to include 3.5% leakage inductance, 5% core and winding loss, and 1.5% bias power.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{16}$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in the equation below. Initially determine transformer primary current.

Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{17}$$

$$L_P = \frac{2(V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{18}$$

The secondary winding to auxiliary winding transformer turns ratio (N_{AS}) is determined by the lowest target operating output voltage in constant-current regulation and the VDD UVLO of the UCC28722. There is additional energy supplied to VDD from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{19}$$

Transformer Parameter Verification

The transformer turns ratio selected affects the transistor V_C and secondary rectifier reverse voltage so these should be reviewed. The UCC28722 does require a minimum on time of the transistor (t_{ON}) and minimum D_{MAG} time (t_{DMAG}) of the secondary rectifier in the high line, minimum load condition. The selection of f_{MAX}, L_P and R_{CS} affects the minimum t_{ON} and t_{DMAG}.

The secondary rectifier and transistor voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{20}$$

For the transistor V_C voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{CPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \tag{21}$$

Equation 22 and Equation 23 are used to determine if the minimum t_{ON} target of 300 ns and minimum t_{DMAG} target of 1.2 µs is achieved.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}} \tag{22}$$

$$t_{DMAG(min)} = \frac{t_{ON} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \tag{23}$$

Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in some USB charger applications there is a requirement to maintain a minimum V_O of 4.1 V with a load-step transient of 0 mA to 500 mA . The equation below assumes that the switching frequency can be at the UCC28722 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}\left(\frac{1}{f_{SW(min)}} + 150\ \mu s\right)}{V_{O\Delta}} \tag{24}$$

Another consideration of the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} = \frac{V_{RIPPLE} \times 0.8}{I_{PP(max)} \times N_{PS}} \tag{25}$$

VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the voltage to the UCC28722. The total output current available to the load and to charge the output capacitors is the constant-current regulation target, I_{OCC}. The equation below assumes all the output current of the flyback is available to charge the output capacitance from 0 V to V_{OCC}. If the converter is going to be loaded during the time the output is ramping from 0 V to V_{OCC}, that load current must be subtracted for the available output current limit value, I_{OCC}. There is 1 V of margin added to VDD in the calculation.

$$C_{DD} = \frac{\left(I_{RUN} + I_{DRS(max)} \times \left(1 - D_{magcc}\right)\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{\left(V_{DD(on)} - V_{DD(off)}\right) - 1\ V} \quad (26)$$

Note that the typical ceramic capacitor of sufficient ratings for use here varies considerably in effective capacitance as the voltage across the capacitor changes. As the capacitor voltage increases beyond 25% of its rated voltage, the effective capacitance can become significantly less than the nominal capacitance at zero bias. This equation calculated the effective capacitance needed over the 8V to 21V range, not the nominal zero bias capacitance required. Evaluation of the particular capacitor chosen for this function is strongly recommended to ensure adequate capacitance over the 8V to 21V range.

VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (27)$$

The low-side VS pin resistor is selected based on desired V_O regulation voltage.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times \left(V_{OCV} + V_F\right) - V_{VSR}} \quad (28)$$

The UCC28722 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected base drive and transistor turn-off delay. Assume a 50-ns internal delay in the UCC28722.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (29)$$

The UCC28722 has adjustable cable drop compensation. The resistance for the desired compensation level at the output terminals can be determined using Equation 30.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\ k\Omega \times \left(V_{OCV} + V_F\right)}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega \quad (30)$$

Startup Resistance and Startup Time

Once the VDD capacitor is known, there is a tradeoff to be made between startup time and overall standby input power to the converter. Faster startup time requires a smaller startup resistance, which results in higher standby input power.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{T_{STR}}} \quad (31)$$

REVISION HISTORY

Changes from Original (December 2013) to Revision A **Page**

- Changed Marketing status from Product Preview to Active. 1
- Changed Simplified Application Diagram. 1
- Changed Supply current, fault values from 95 µA and 170 µA to 2.00 mA and 2.65 mA. 4
- Changed Functional Block Diagram. 6
- Changed Bias Supply Current vs. VDD Voltage image. 10
- Changed Operating Current vs. Junction Temperature image. 10
- Changed Simplified Flyback Convertor image. 12
- Changed C_{DD} equation. 24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28722DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	U722	Samples
UCC28722DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	U722	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

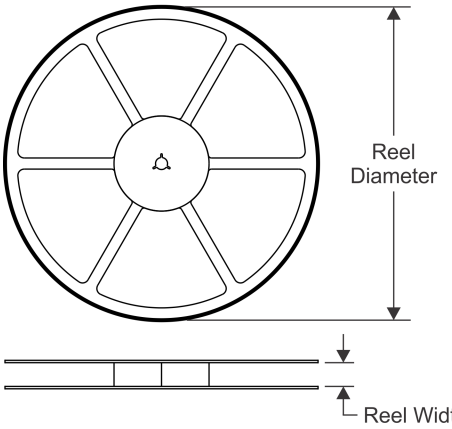
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

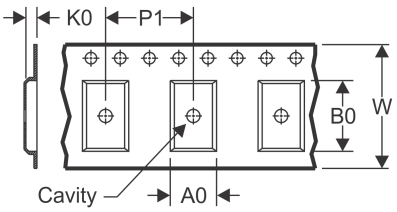
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

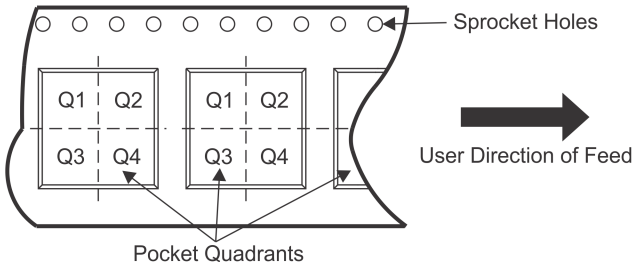


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

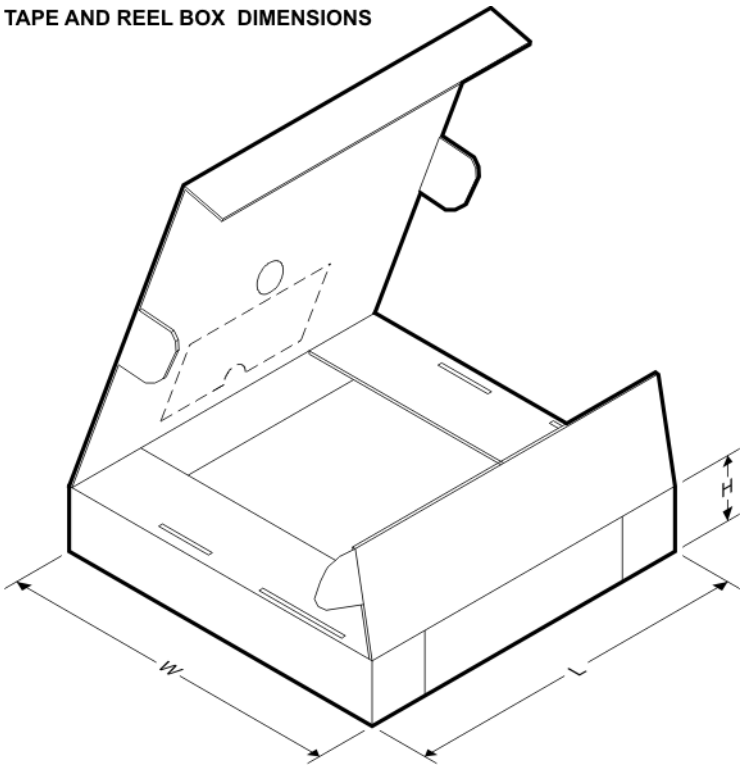
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28722DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC28722DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

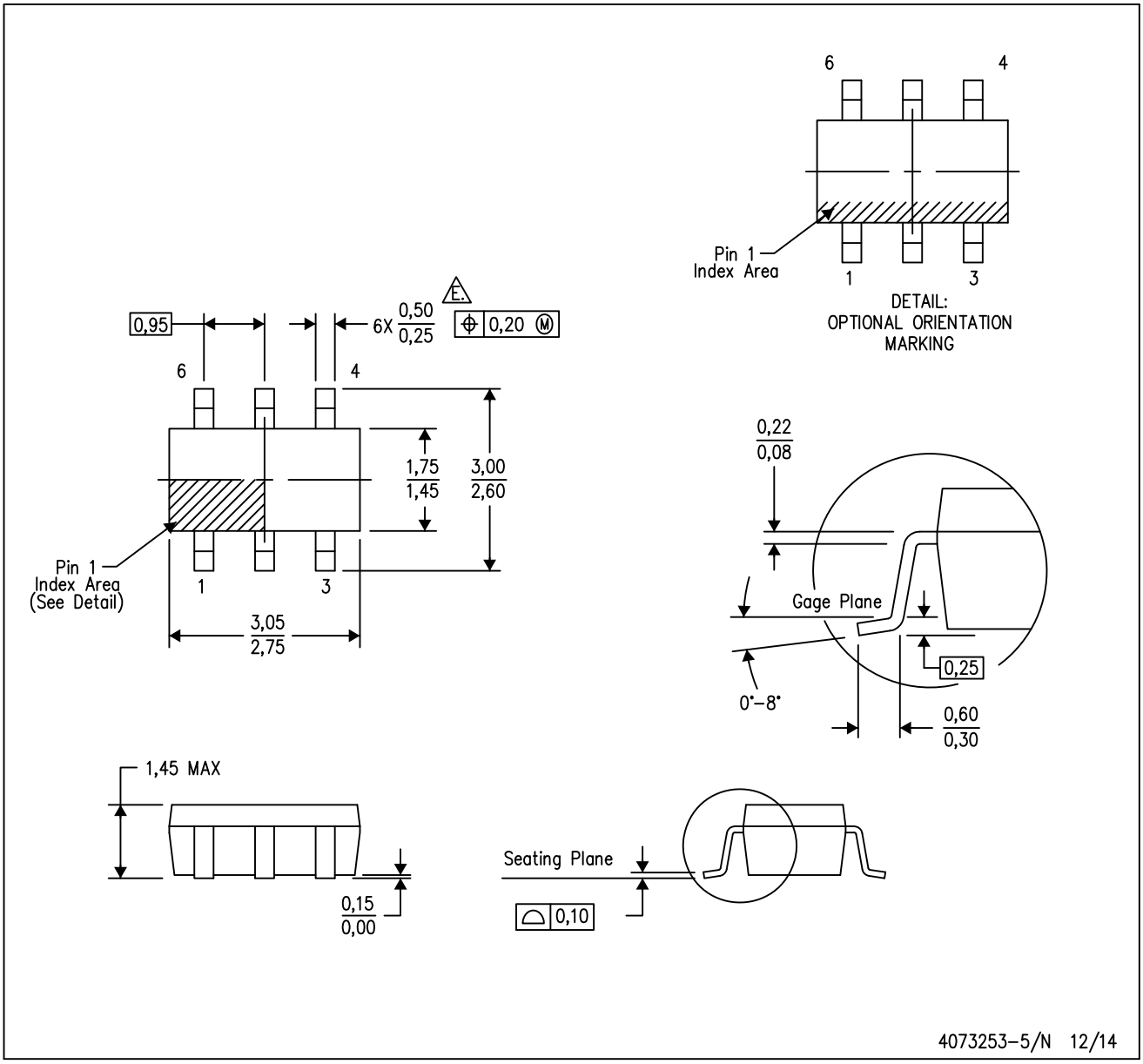
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

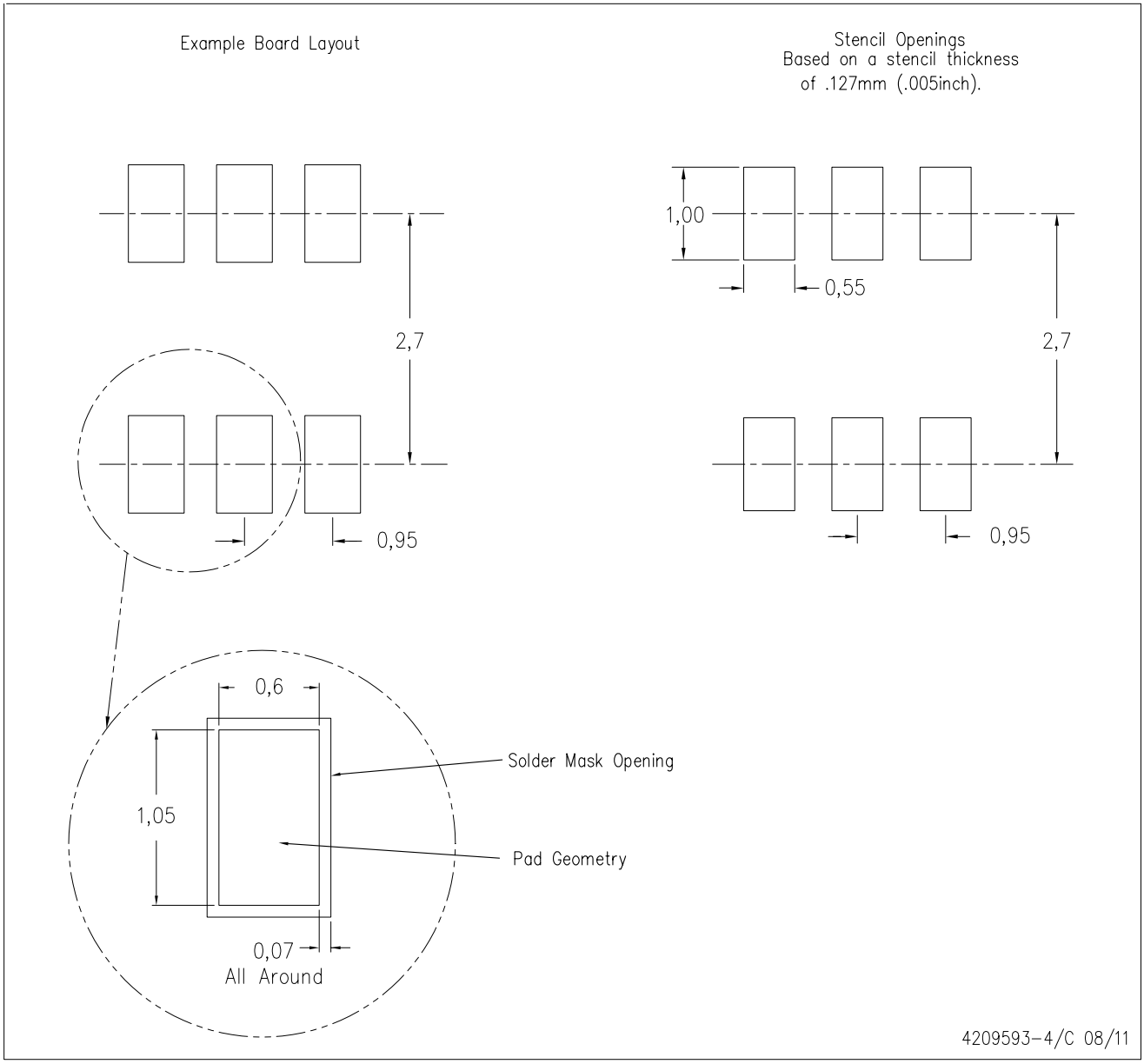
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28722DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC28722DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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